The MIT Virtual Source (MVS) Model: from device science to circuits and systems

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Background

The MIT Virtual Source (MVS) model for nanotransistors was first published in 2009 by the Antoniadis group at MIT [1], and it has provided a sound, physics-based approach to modeling near-ballistic Si MOSFETs anchored in the Landauer transmission approach as elaborated by Lundstrom and his collaborators over several years. With simple analytical expressions, it captures the FET terminal current and charge dependencies on physical quantities such as the apparent carrier mobility and injection velocity. The model was used to characterize those parameters in Si CMOS devices, and with simple extensions, in advanced InGaAs HEMTs fabricated by the del Alamo group at MIT [2]. As such it became an important tool for projecting performance of FETs with advanced channel materials along the Technology Roadmap. The MVS model was first demonstrated to work in simple circuit simulations based on a primitive Verilog A implementation in 2012 [3], but it had remained largely in its analytical MATLAB implementation.

What were the goals?

With the launch of the NEEDS initiative (needs.nanoHUB.org) on September 1, 2012, the MVS model was selected to drive the specification of a NEEDS compact model release package and to define NEEDS compact model publication processes. A robust Verilog A version of MVS became the first compact model published under the NEEDS program [4]. Subsequently, the MVS FET model became the backbone of several compact models that have been developed and deployed with support from the NEEDS program. It also proved useful in probing the physics of carrier transport in nanoscale FETs. This work is described below.

What was accomplished?

The very first significant extension of MVS made possible by the NEEDS program was to model ambipolar transport in MOSFETs fabricated on graphene [5,6]. This work proved the soundness of the virtual source concept in capturing the behavior of near-ballistic (nanoscale) device even when two virtual sources of carrier injection exist at opposite ends of the channel, one for electrons and the other for holes, as in the case of the bandgap-less graphene. Excellent reproduction by the AVS model of experimental I-V behaviors of several devices fabricated in different labs and with a broad range of channel lengths was demonstrated buttressing the physical soundness of the model. Furthermore, with robust implementation in Verilog A, and properly modeling the terminal charges as well as current the AVS was used in circuit simulations to study the efficiency of frequency doubling circuits vs. frequency and was the base for proposing a novel differential circuit implementation of the doubler with significantly improved efficiency (increased first harmonic to fundamental and second harmonic ratios compared to the original single-ended circuit) [7]. This model is currently being used by the Pop group at Stanford to explore the use of graphene transistors to implement dot product functions.

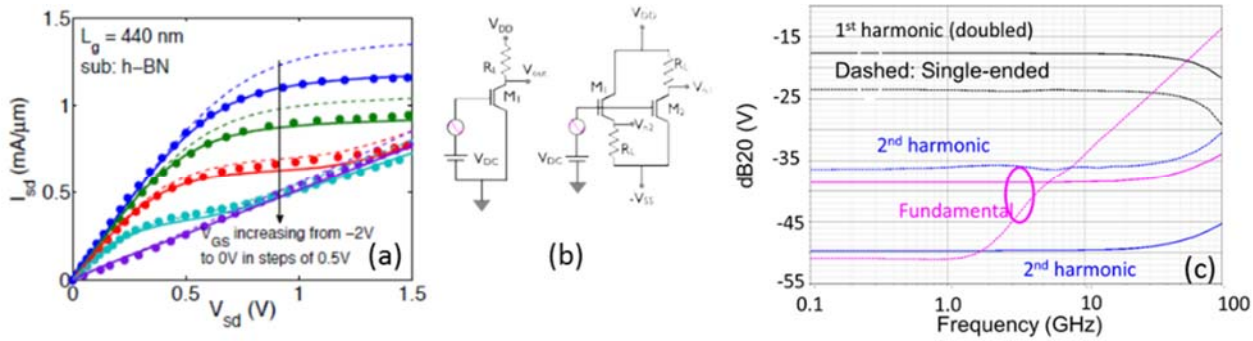

Figure 1. (a) Output curves at various VGS for a 440 nm exfoliated GFET on hexagonal boron nitride (h-BN) substrates. Model - solid lines, symbols - experimental data. Dashed lines are produced using the model but without considering the degradation in injection velocity due to carrier-scattering effects. (b) Single-ended and differential GFET frequency doubler circuits. (c) Simulated output voltage vs. frequency for the two circuit configurations demonstrating clearly superior efficiency of the differential topology by suppressed fundamental and 2nd harmonic components.

Another significant extension of MVS was the adaptation of the model to novel GaN-channel FETs [8,9], which became the PhD thesis topic of Ujwal Radhakrishna. This model is at this point in use in (at least) two companies and has been adopted by the Compact Model Coalition (CMC) for industry standardization in a robust Verilog A implementation that is expected to run efficiently over multiple circuit simulation platforms. The model has been verified against both individual devices and full circuit measurements in both the RF (up to 5 GHz) and the High Voltage operation regimes and has demonstrated excellent results. Once again the breadth of the technologies, the fitting to measurements with a small number of physically sensible fitting parameters, and the excellent prediction of circuit hardware performance, are testimony to the soundness of the physics-based core of the model.

The development of both the AVS and MVSG models entailed significant modification of the original MVS model. However, the basic MVS model has also proven to be an excellent tool for the characterization and the prediction of device performance with very early stage technologies where straightforward test structure characterization is not possible. One of those applications was in the evaluation of 2D-channel FET (MoS_2) operation in the sub-10 nm channel length regime. In this case experimental sub-10-nm devices could only fabricated in groups of several in series via an ingenious transformation of single and few-layer MoS_2 films in alternating segments of semiconducting and metallic phases [10]. This was accomplished with chemical exposure of the films through a nano-scale pattern with sub-10-nm period achieved via directed self-assembly of a block co-polymer resist. Simulating the structure as a series combination of FETs, and interpreting the measured I-V results as such, it was possible to extract the carrier apparent mobility, velocity, and importantly, the remarkably low contact resistance between semiconducting and metallic MoS_2 phases.

Another example of the use of MVS in the exploration of early stage technologies is a recent extension of the MVS model to the modeling of MOSFETs incorporating a negative capacitance (ferroelectric) dielectric in the gate stack NCFETs [11, 12]. While many aspects of this technology are still in very early phase of investigation, one of the NCFET model implementations, the recently released MVSNC in Verilog A, has allowed the exploration of the

detrimental influence of current leakage through the FE dielectric on the expected benefits for the NC gate stack and has helped identify work-function engineering as a mitigation approach [13]. This would not have been possible without the full, circuit simulation capabilities of the MVSNC.

Finally, the MVS model has proven to be a good tool for elucidating the physics of carrier transport at the nanoscale. Work done in collaboration with IBM on electron transport in nanoscale Extremely Thin SOI MOSFETs is one example [13]. Another is recent work that suggests that backscattering from the drain can be important in certain MOSFETs [14]. These and other studies have not only shed light on the physics of nanoscale MOSFET, they have also led to refinements in the MVS model resulting in a version of the model with a much more sophisticated treatment of transport physics [15, 16].

Why was it important?

The MVS model introduced in 2009 has proven to be a useful tool for exploring device physics and for assessing the potential of early stage technologies. Eleven compact models published on needs.nanoHUB.org are MVS models or incorporate the MVS model. These models have been downloaded almost 5000 times. The first MVS model also played an important role in helping NEEDS define compact model publication standards and processes. Finally, the use of the model in analyzing experimental data from a variety of devices and materials has significantly increased our understanding of electron transport in nanotransistors. While much of the research has been forward looking, MVS was also used to develop a new, industry-standard compact model for GaN FETs. The published compact models and the concepts underlying the MVS model [17] are likely to continue to be useful in advancing the science and applications of nanotransistors.

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