From Science to Nanofunctions with 2D Transistors

NEEDS 2012-2017 (needs.nanohub.org)
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What were the goals?

The goals of our NEEDS project were to encapsulate the emerging device and materials science of two-dimensional (2D) materials (like graphene and MoS_2) into compact circuit models that could be made widely available (on the nanoHUB) and into simple nanofunctions, demonstrating system-level functionality. There were actually two separate goals, at different levels of maturity when NEEDS started. The first one was to implement and develop "from scratch" a complete device-to-circuit model of monolayer semiconductor devices (based on MoS_2 and WSe_2). The second goal was to take a more mature device model (the MIT Virtual Source graphene model) and use it to optimize graphene-based dot product nanofunctions which we were experimentally building within another project (StarNET SONIC).

What was accomplished?

The Stanford 2D semiconductor (S2DS) transistor model for 2D field-effect transistors (FETs) was developed from scratch by Saurabh Suryavanshi within the Pop group at Stanford. This model is presently available at https://nanohub.org/publications/18/2 where it was viewed by 2400 users, had 450 downloads, and 2 citations (as of April 2017). A schematic of the 2D FET with the parasitic is shown in Fig. 1(a).

A semi-classical transport approach is appropriate for the 2D channel, enabling simplified analytical expressions for the drain current. In addition to intrinsic FET behavior, the model includes contact resistance, traps and impurities, quantum capacitance, fringing fields, high-field velocity saturation and self-heating, the latter being found to play a strong role. The model is calibrated with state-of-the-art experimental data for n- and p-type 2D-FETs, and it can be used to analyze device properties for sub-100 nm gate lengths. Using the experimental fit, we demonstrate feasibility of circuit simulations using properly scaled devices. The model is implemented in SPICE-compatible Verilog-A, and a downloadable version is freely available on the nanoHUB.org.

We have also used S2DS to predict the impact of 2D material *variation* on device and circuit performance and variability. We performed Monte Carlo simulations of standard cells for different technology nodes with channel length L = 16 nm to 500 nm. The S2DS model was fitted to our experimental devices [Fig. 1(b)], but otherwise assumed contact resistance and EOT (for top-gate oxide) based on ITRS specifications, with I_{OFF} = 100 nA/μm for high-performance applications. For each technology (channel lengths from 16 to 500 nm), we simulated 600 standard cells to obtain statistically significant data. In our analysis, the Monte Carlo engine assigns the device mobility with a Gaussian distribution mimicking the experimentally measured data. The measured mobility of these transistors is plotted as a histogram in Fig. 1(c). In Fig. 1(d), we show 10 simulations of rising output in 2-input NAND gate with 65 nm transistors. For the same standard cell, rise and fall times are extracted from 600 Monte Carlo and shown in Fig. 1(e). We further quantify the standard cell variation in terms of coefficient of variation (CV) rise and fall times, calculated as the mean divided by the standard deviation. As shown in Fig. 1(f),

the delay CV < 0.1 for channel length down to 16 nm for 2-input NAND gates. This contrasts with the observation from other nanotechnologies such as carbon nanotubes, where the variation is significant for scaled devices and requires special processing steps to make useable systems.

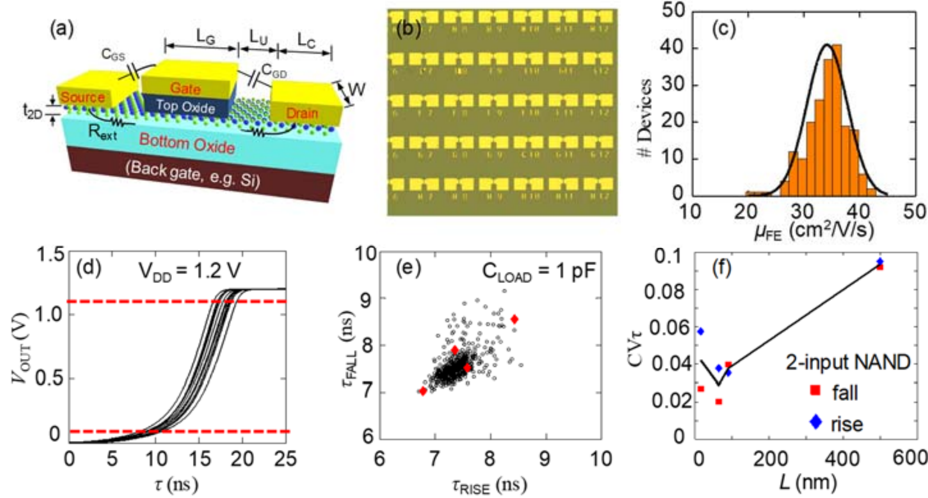

Figure 1 S2DS: (a) Schematic of 2D semiconductor FET, including parasitic elements [1]. (b) Optical image of a portion of the chip with over 200 finished devices. (c) Extracted field effect mobility (μ_{FE}) from the experimental devices. Black line shows the Gaussian fit to experimental data. (d) Simulated output demonstrating the rise time in 2-input NAND gates. (e) Extracted rise times (τ_{RISE}) and fall times (τ_{FALL}) for 600 NAND gates are shown by black symbols. The performance corners simulated for $\mu_{mean} \pm 2\sigma_{std\text{-}dev}$ are shown in red diamonds. (f) Shows variation (CV) in rise times and fall times for NAND. The variation in average delay is shown by black lines.

Our second NEEDS-related project involved fabricating a graphene analog dot-product nanofunction (GDOT). To achieve this, we fabricated a 4-input GDOT using wafer-scale graphene grown by chemical vapor deposition (CVD) [Fig. 2(a)]. Fig. 2(b) shows a schematic of our top-gated graphene transistors used in GDOT. We used the MIT-VS graphene compact model to fit the experimental measurements as shown in Fig. 2(c). The extracted parameters are then used to design, optimize, and benchmark the GDOT. The output of a GDOT using 2-inputs is shown in Fig. 2(d). Additional details can be found in refs. [3,4].

Why was it important?

We aim to unravel potential applications of low-dimensional materials such as MoS_2 and graphene. Both of our NEEDS projects involved working with these materials, which are in early stages of development. The properties of these lab-grown nanofabrics is far from ideal. In order to model, design, optimize, and eventually benchmark these nanomaterials, it is necessary to understand the non-idealities. Along the way, such physics-based modeling approaches also help to provide valuable feedback and direction to the experimental work. Working at the intersection of experiment and modeling allows students to learn beyond the *ideal* characteristics of

semiconductors. The robust physics-based models help the community as well as industry to develop realistic benchmark for these nanomaterials.

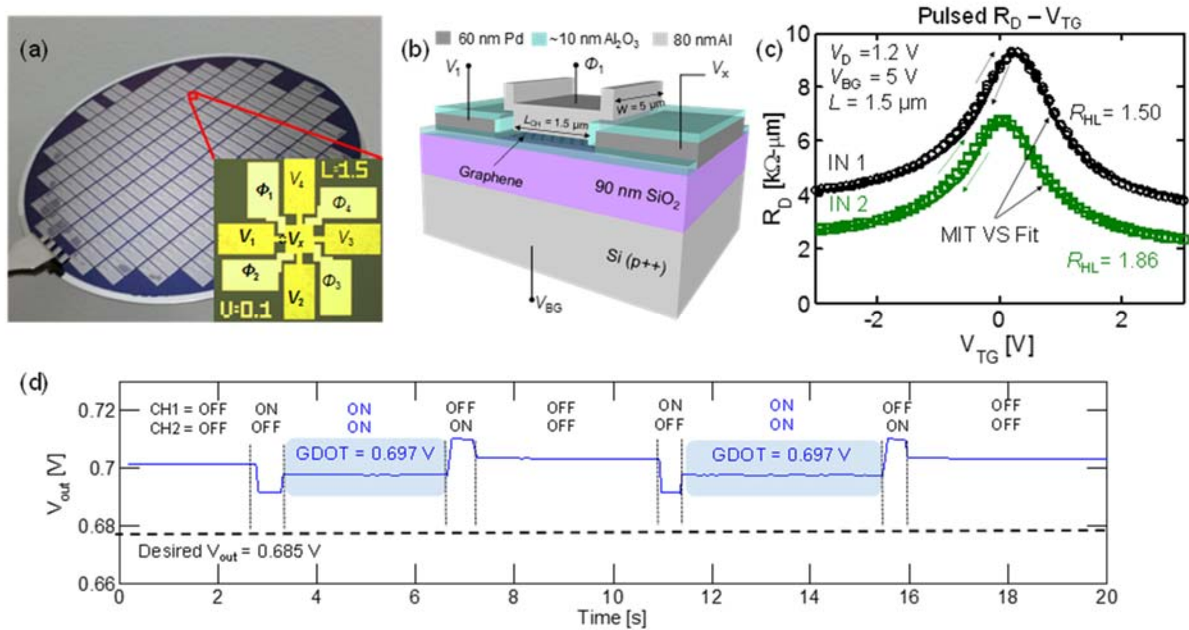

Figure 2 GDOT: (a) Wafer-scale (4”) GDOT fabrication. (Inset) Optical image of prototype 4-input L = 1 μm GDOT. (b) Representative GFET cross section. (c) Pulsed device resistance [R_D] vs top-gate bias [V_{TG}] (symbols) and MIT-VS model fit (lines) for fabricated GFETs. (d) Measured V_{out} vs. time (V_1 = 0.665 V, p_1 = 0.7, V_2 = 0.7321 V, p_2 = 0.3). CH1 and CH2 refer to manually triggered pulse generator outputs.

References (* denotes work supported or partially supported by NEEDS)

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3) N.C. Wang, S.K. Gonugondla, I. Nahlus, N.R. Shanbhag, E. Pop, "GDOT: A Graphene-Based Nanofunction for Dot-Product Computation" *IEEE VLSI Tech. Symp.*, Jun 2016, Honolulu HI (*)

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