Carbon Nanotubes Enable Highly Energy-Efficient sub-10 nm Node Digital VLSI Systems

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Background

While scaling of silicon-based field-effect transistors (FETs) has significantly improved digital logic circuit speed and energy efficiency for decades, continued miniaturization yields diminishing returns. How can we then achieve the next order of magnitude improvement in energy efficiency of digital logic technologies? To address this outstanding question, a variety of technology options are currently being explored for future sub-10 nm nodes (e.g., the 7 nm node). These options include silicon-based evolutionary developments – such as silicon-germanium (SiGe) channels, or progressing from FinFETs to nanowires (NWs) – as well as replacing silicon with nanotechnologies such as carbon nanotube (CNT) FETs (CNFETs). To effectively guide the exploration of such options, the following question must also be answered: how do we accurately compare the energy efficiency benefits of these technology options for realistic very-large-scale integrated (VLSI) logic circuits? Importantly, performance projections for CNFET digital VLSI circuits must account for significant CNT-specific process variations, which can significantly degrade their projected energy and speed benefits 0.

What were the goals?

Our goals were to answer the two key questions:

1) How can we achieve the next order of magnitude improvement in energy efficiency of digital logic technologies?

2) How do we accurately compare the energy efficiency benefits of various technology options for realistic very-large-scale integrated (VLSI) logic circuits?

Due in large part to the NEEDS initiative, including support from the NEEDS program as well as our contributions to needs.nanohub.org, we can now answer both questions; in particular, using tools we've developed for designing VLSI systems using emerging technologies (available at https://nanohub.org/resources/22582) 0, which leverage compact models developed for NEEDS (e.g., the Virtual Source CNFET compact model: https://nanohub.org/publications/42) 0, we have shown the following.

1) We quantify and compare the VLSI circuit-level energy efficiency benefits (quantified by the energy-delay-product: EDP) for future technology options, using industry-standard physical designs of sub-10 nm node digital VLSI processors, and using technology parameters extracted from experimental data 0.

2) We demonstrate that compared with sub-10 nm FinFETs, evolutionary silicon-based technologies offer only marginal (<30%) EDP benefits. In contrast, CNFETs drastically improve EDP of VLSI digital logic circuits by an order of magnitude (9.0X), while maintaining the same off-state leakage current density (≤100 nA per micron of FET width) and total chip power density (≤100 W per cm^2 of chip area). This is shown using physical

designs of the processor core of the OpenSparc T2 system-on-chip (SoC) 0.

3) We show that by co-optimizing CNT process improvements, together with CNFET circuit design, that the overall CNFET circuit speed degradation can be limited to 5%, with 5% energy cost, while simultaneously meeting circuit-level noise margin and yield constraints. Furthermore, our framework runs over 100X faster than existing approaches, and automatically explores the large space of CNT processing options to derive optimized CNT processing and CNFET circuit design guidelines (e.g., for CNFET sizing and standard cell layouts). Thus, CNFETs can maintain >90% of their projected EDP benefits, even in the presence of CNT variations 000.

What was accomplished?

Even while multiple potential options are being explored for future transistor channels by many research groups, prior to NEEDS, there had previously lacked a rigorous comparison of their energy efficiency benefits for realistic sub-10 nm node VLSI-scale digital integrated circuits (ICs), e.g., ICs consisting of millions or billions of transistors. Previous comparisons are inadequate as they rely on at least one of the following: simplified transistor models (e.g., with fixed on- and off-current for fixed technology parameters such as fixed gate length), simplified circuit models (e.g., ignoring parasitics from physical layouts), and/or small circuit benchmarks (e.g., extrapolating VLSI circuit performance from only inverter chains or adders). Such simplified analyses ignore effects present in realistic VLSI circuits, ranging from physical placement and routing congestion, to wire parasitics, to buffers inserted to meet circuit-level timing constraints, and thus ignoring these effects can lead to highly inaccurate EDP results. To address this outstanding challenge, with support from NEEDS, we have released the first tools for full physical design-based VLSI circuit-level comparison for a sub-10 nm technology node using emerging technologies, leveraging compact models calibrated to experimental data 00, physical layouts of standard cells, and industry-standard tools for synthesis, placement, routing, and power/timing analysis of VLSI circuits in the presence of significant process variations.

As a demonstration of how these tools are useful, Fig. 1 illustrates the energy and clock frequency of the processor core of the processor core of OpenSparc T2 system-on-chip, designed using multiple technology candidates for sub-10 nm nodes, demonstrating: 1) evolving from FinFETs to NWs offers only marginal (<30%) EDP benefits, 2) CNFETs offer 9.0X EDP benefit, and 3) through co-optimized CNT processing and CNFET circuit design, the overall CNFET circuit speed degradation due to CNT variations can be limited to 5% with 5% energy cost.

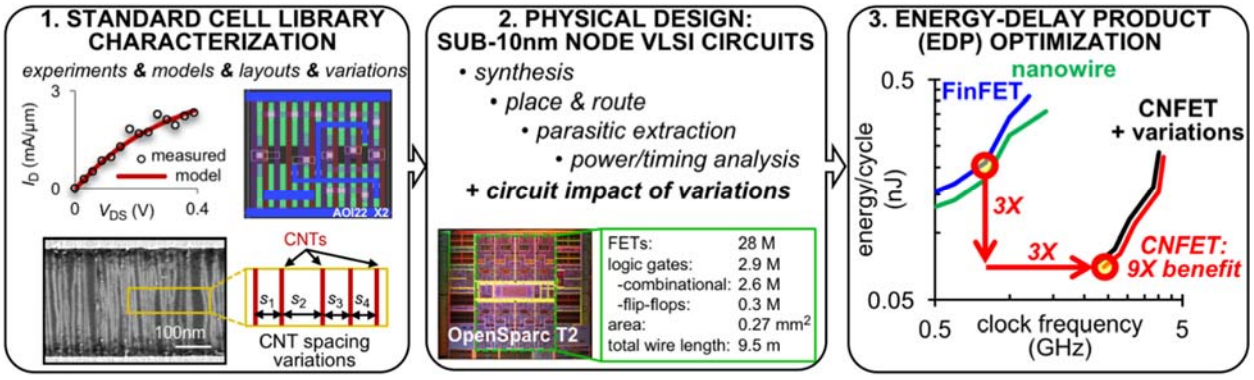

Figure 1. Summary of model-driven approach for designing VLSI systems. 1) Standard cell library characterization, incorporating parasitics extracted from full layouts of standard library cells. 2) Variation-aware physical design methodology including synthesis, place & route, parasitic extraction, and power/timing analysis, e.g., for the processor core of OpenSparc T2. 3) Pareto-optimal energy vs. delay curves for the processor cores of OpenSparc T2 illustrating that CNFET enables VLSI circuits to run 3X faster than FinFET while simultaneously consuming 3X less energy. Additionally, CNFETs can maintain >90% of their projected EDP benefits even in the presence of significant CNT variations.

What was it important?

We have answered an important question in both the research and industrial communities; namely, the tools we have released at https://nanohub.org/resources/22582 provide a methodology to accurately compare the energy efficiency benefits of these technology options for realistic very-large-scale integrated (VLSI) logic circuits using emerging technologies such as CNFETs, accounting for effects present in realistic VLSI circuits such as wire parasitics and process variations 000. Not only can users can reproduce our results for CNFET circuits, but also these tools can be adapted to analyze the energy efficiency benefits of alternative technologies (e.g., FETs based on 2D materials), leveraging alternative compact models developed as part of the NEEDS initiative. Furthermore, our tools for quantifying CNFET circuit performance in the presence of CNT variations have been used to explore other research opportunities as well, including (but not limited to) the design of CNFET-based SRAM cells 0, power delivery networks using CNTs 0, new logic synthesis techniques 0, and monolithic 3D integrated systems leveraging multiple layers of computation and memory integrated over the same starting substrate enabling 1,000X energy efficiency benefit for VLSI systems 0.

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