A New Non-linear Noise model for scaled CMOS Transistors

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Background

Most existing MOSFET noise models are based completely upon thermal noise, assuming that the noise originates from several thermal noise sources including a finite channel conductance, induced gate noise correlated to the channel noise, and various parasitic resistances. To help explain the noise behavior (and also high frequency and high power behavior), a distributed gate resistance effect has been introduced for multi-finger transistors. Due to difficulty in its implementation, instead of using a lumped RC model, this effect has been most commonly modeled by a lumped gate resistor with a modified empirical resistance value. Despite various modifications to capture the noise of nanoscale transistors, the classical long-channel thermal noise model requires geometry and bias dependent empirical parameters, especially when the channel length scales down below 100 nm.

A shot noise model has been proposed for ultra short-channel MOS transistors with ballistic transport, where the shot noise is due to electron injection from the source region through the potential barrier and into the channel [1]. In such ballistic transistors, the channel thermal noise can be ignored. While this shot noise model fits the noise behavior of ultra short-channel transistors investigated by device simulation, the model is not experimentally verified as no comparison to measured noise data has been reported. Additionally, current sub-100 nm MOS transistors are still semi-ballistic transport devices and the aforementioned shot noise model is not expected to completely capture their noise behavior.

What were the goals?

The goal of this work was to develop a nonlinear and scalable model suitable for predicting high frequency noise of N-type Metal Oxide Semiconductor (NMOS) transistors. The model was developed for a commercial 45 nm CMOS SOI technology and its accuracy was validated through comparison with measured performance of a microwave low noise amplifier. The model employs the virtual source nonlinear core (from MIT) and adds parasitic elements to accurately simulate the RF behavior of multi-finger NMOS transistors up to 40 GHz. For the first time, the traditional long-channel thermal noise model is supplemented with an injection noise model to accurately represent the noise behavior of these short-channel transistors up to 40 GHz. The developed model is simple and easy to extract, yet very accurate.

What was accomplished?

A simple equivalent circuit based MOSFET RF model has been developed for NMOS transistors in this technology. The RF model is built on top of the MIT virtual source DC non-linear model, which accurately predicts the DC performance of NMOS transistors studied in this project. The RF model also includes intrinsic parasitic capacitances and extrinsic parasitic elements originated from interconnections, vertical interconnects (VIAs), RF pads and transistor layout parasitics. All these parasitic elements have been extracted from the measured S-parameter data.

The existing long-channel noise model has been adopted by most model developers through assigning a larger and non-constant channel noise parameter that changes with both bias and

device dimensions to accommodate larger than expected noise of short-channel MOS transistors. While such a modification is convenient, it does not capture the noise of short-channel devices accurately, especially as the drain-source voltage or the lattice temperature of the device changes. Extraction of the empirical channel noise parameter to fit to all measured noise data is also very cumbersome. In [1], the channel noise of ballistic NMOS transistors has been attributed to the shot noise induced by random injections of electrons from the source to the channel, whereas the thermal noise in the channel has been completely eliminated.

For the semi-ballistic NMOS devices studied here, noise contributions from both thermal and shot noise must be considered, as depicted in Fig. 1, leading to the effective channel noise spectral density given by

$$\overline{i_{Ch}^2} = \overline{i_{sh}^2} \cdot \left(\frac{1 + g_m R_{DS}}{1 + g_m R_{DS} + g_D R_{DS}}\right)^2 + \overline{i_{th}^2} \cdot \left(\frac{g_D R_{DS}}{1 + g_m R_{DS} + g_D R_{DS}}\right)^2$$

where R_{DS} is the output resistance, g_m is the device transconductance and g_D is the N/N+ junction diode (channel to source) forward bias conductance. This N/N+ junction diode at the virtual source is a non-ideal diode, leading to the introduction of a fitting noise parameter $\zeta = \frac{g_D R_{DS}}{1+g_m R_{DS}+g_D R_{DS}}$ in the following equation.

$$\overline{i_{Ch}^2} = \overline{i_{sh}^2} \cdot (1-\zeta)^2 + \overline{i_{th}^2} \cdot \zeta^2$$

In the above equations, i_{sh} *and* i_{th} are ideal shot and thermal noise sources. The correlation between the two noise sources is ignored as the two noise mechanisms are spatially separated. The noise equivalent circuit model is depicted in the schematic shown in Fig. 1(a). Figs. 1 (b) and (c) depict the noise mechanism in the device. The combination of the shot and thermal noise models not only predicts the drain current noise accurately, but also captures the undying physics very well. Fig. 1 (d) and (e) show measured and simulated noise parameters NF_{min}, R_n, and Γ_{opt} by three different models, namely the one developed in this work with the noise parameter ζ= 0.3, the classical ideal long-channel thermal noise model with γ of 2/3, and the post-layout foundry model with a bias and size dependent γ compared to the measured data. As shown, the developed noise model is more accurate that the classical model and the one developed by the Foundry.

In order to further verify the model accuracy, a two-stage microwave low noise amplifier (LNA) shown in Fig. 2(a) has been implemented in the same technology and the measured performance is compared with the simulation result based on this model. The gain and noise figure at 50 Ω input impedance has been measured and the results are compared with the model developed here and the one provided by the foundry-supported process design kit (PDK) as shown in Fig. 2(b). A close agreement between the measured data and simulated data based on this model is observed.

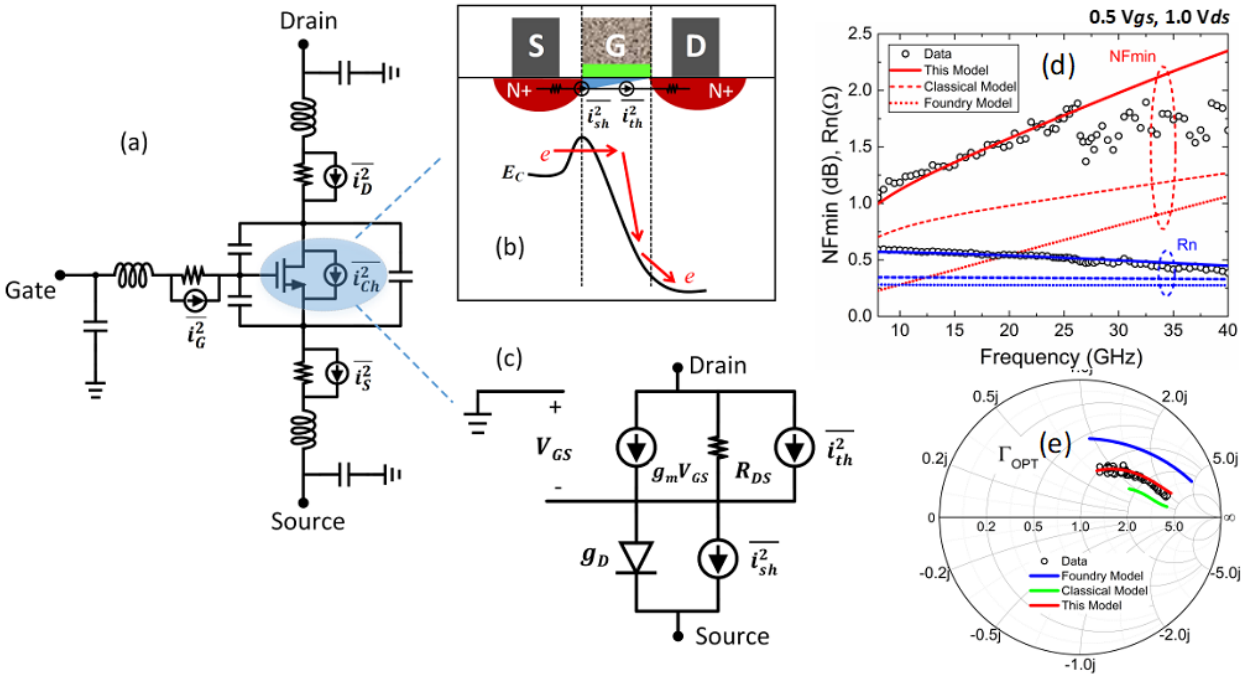

Fig. 1. (a) Equivalent noise circuit model of a MOSFET with various noise sources; (b) The inset depicts the noise mechanisms in the channel for short-channel MOSFETs; (c) Circuit representation of the two noise sources inside the intrinsic transistor transport region; Measured (open symbols) and simulated (lines) noise parameters with three different noise models (d) NF_{min} and R_n as functions of frequency at bias V_{gs} = 0.5 V and V_{ds} = 1 V, (e) Γ_{OPT} plotted on a Smith impedance chart for an NMOS transistor with a width of 84 µm.

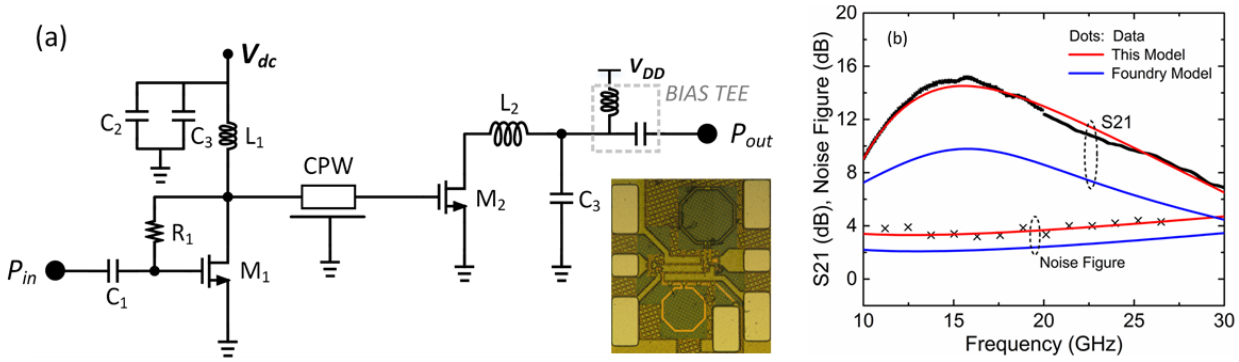

Fig. 2. (a) The circuit schematic of a two-stage microwave LNA. The first stage uses a 126 µm wide transistor while the second stage has an 84 µm wide transistor. (b) The comparison between measured and simulated S_{21} and Noise Figure of the LNA (50 Ω source impedance) vs. frequency. Noise data was only available up to 26.5 GHz.

Why was it important?

A new combined shot-thermal channel noise model that predicts the high frequency noise behavior of NMOS transistors has been developed. The developed noise model uses only one fitting parameter, which is not geometry, bias or frequency dependent. The model overcomes the

limitations of most existing thermal noise based models, which use bias, geometry and sometimes frequency dependent parameters in predicting the noise of sub-100 nm channel length transistors.

The developed model is a complete scalable non-linear model that has been recently published [2][3]. Further work is underway to release a process design kit (PDK) based on this model. The new PDK will be utilized in ECE 60420 (Radio Frequency Integrated Circuits) in Fall 2017.

References (* denotes supported by NEEDS)

[1] R. Navid, C. Jungemann, T. H. Lee, and R. W. Dutton, "High-frequency noise in nanoscale metal oxide semiconductor field effect transistors" *J. Appl. Phys.*, vol. 101, no. 12, 2007.

[2] Y. Shen, J. Cui and S. Mohammadi, "An Accurate Model for Predicting High Frequency Noise of Nanoscale NMOS SOI Transistors" to appear in *Journal of Solid-State Electronics*. (*)

[3] 45 nm NMOS SOI compact model available from https://nanohub.org/groups/needs/compact_models (*)