Scalable SOI transistor models and process design kits (PDKs)

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What were the goals?

Scalable transistor models and process design kits (PDKs) developed by microelectronic industry are considered intellectual properties and are not readily available to educational community. Developing the models that typically require more than 100 physical and empirical parameters is very challenging and time consuming. On the other hand, device models and PDKs available to educational institutions are often not verified with any specific technology, and therefore lack the accuracy for any meaningful circuit implementation. Moreover most such models lack device noise characteristics. The goal of this activity was to develop scalable models for NMOS and PMOS transistors, passive components and a PDK for a scaled CMOS technology with high degree of accuracy. Students who use such models and PDKs can achieve accurate simulation of their circuits and will be able to easily go to circuit implementation if they choose to.

The activity was focused on developing an accurate scalable model for NMOS transistors fabricated in GlobalFoundries 45nm CMOS SOI technology. The model employs the virtual source nonlinear core (from MIT) and adds parasitic elements to accurately simulate the RF behavior of multi-finger NMOS transistors up to 40 GHz. For the first time, the traditional long-channel thermal noise model is supplemented with an injection noise model to accurately represent the noise behavior of these short-channel semi-ballistic transistors up to 40 GHz. The developed model is simple and easy to extract, yet very accurate. It only uses one empirical parameter for noise, which is independent of device size, bias and operating frequency.

What was accomplished?

To construct the scalable nonlinear model, first the virtual source model with only 10 parameters was extracted from various dc measurements. Parasitic capacitance, inductance and resistance were added to the virtual source core and their values were extracted from various ac measurements of the device using standard techniques available in the literature. To capture the noise behavior of the transistor, the standard technique is to utilize the long-channel noise model with variable and empirical channel noise parameters that change with both bias and device dimensions to accommodate larger than expected noise of short- channel MOS transistors. While such approach is convenient, it does not capture the noise of short-channel devices accurately, especially as the drain-source voltage or the lattice temperature of the device change. Extraction of the empirical channel noise parameter to fit to all measured noise data is also very cumbersome.

For the semi-ballistic NMOS devices studied here, noise contributions from both thermal and shot noise must be considered, as depicted in Fig. 1. There is only one empirical parameter, namely the ratio of the shot noise to thermal noise spectral power densities, which is constant and independent of device dimensions, bias and operating frequency. The noise model is depicted in Fig. 1(a). Figs. 1 (b) and (c) depict the noise mechanism in the device. The combination of the shot and thermal noise models not only predicts the drain current noise

accurately, but also captures the underlying physics very well. Fig. 1 (d) and (e) show measured and simulated noise parameters NF_{min}, R_n, and Γ_{opt} by three different models, namely the one developed in this work, the classical ideal long-channel thermal noise model, and the post-layout foundry model with a bias and size dependent noise parameter. As shown, the developed noise model is more accurate than the classical model and the one developed by the foundry.

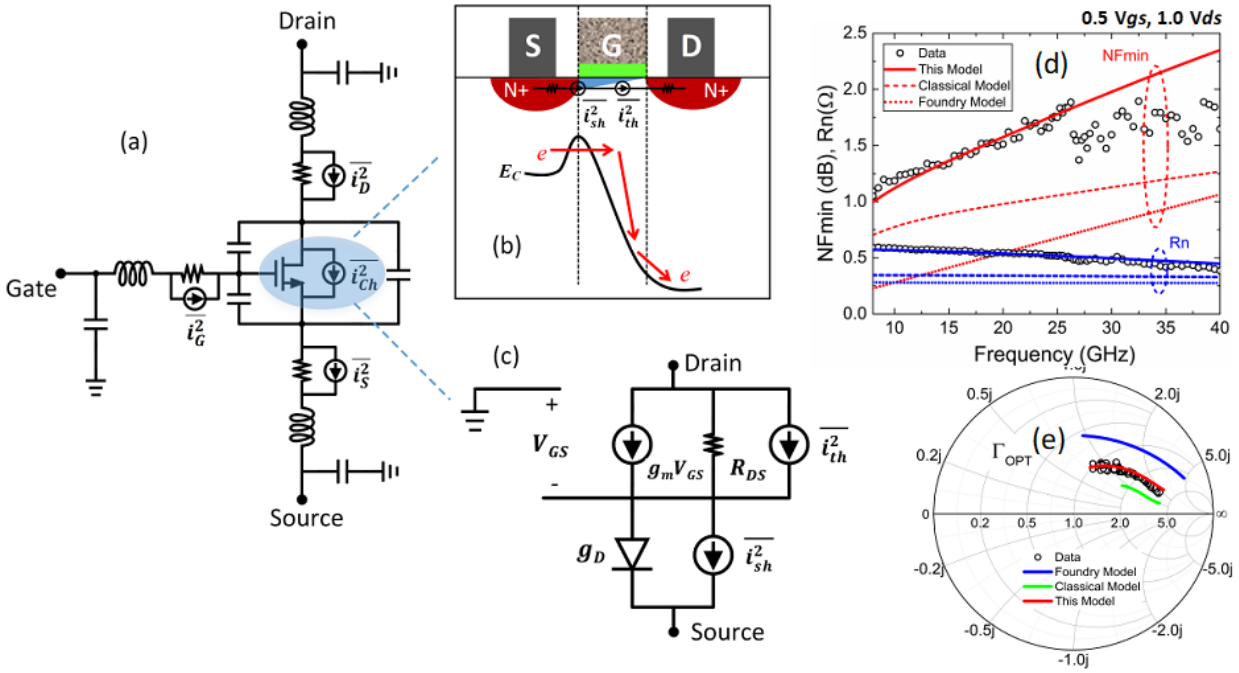

Fig. 1. (a) Equivalent noise circuit model of a MOSFET with various noise sources; (b) The inset depicts the noise mechanisms in the channel for short-channel MOSFETs; (c) Circuit representation of the two noise sources inside the intrinsic transistor transport region; Measured (open symbols) and simulated (lines) noise parameters with three different noise models (d) NF_{min} and R_n as functions of frequency at bias V_{gs} = 0.5 V and V_{ds} = 1 V, (e) Γ_{OPT} plotted on a Smith impedance chart for an NMOS transistor with a width of 84 µm.

The scalable nonlinear model developed for NMOS transistor is very accurate yet easy to extract [1-2]. The NMOS model when supplemented with PMOS model, passive components model and layout parasitic models can be easily turned into a PDK. Such PDK will be developed in collaboration with Dr. Matthew Swabey and will not rely on any intellectual properties from third parties. Hence, it can be shared with graduate and undergrad students who take circuit design courses not only in the US but also in other parts of the world. In the emerging era of the Internet of Things, students who are equipped with such advanced and accurate circuit design tool can use their imagination and creativity to develop novel concepts from ideas to market. With the accuracy, simplicity and availability of these PDKS to a broad enthusiastic student population, the turnaround time for many new IoT products is expected to be very short.

Why was it important?

Several graduate and undergraduate students benefited from this project. Two PhD students who graduated in 2016 were partially supported by this project. One of them pursued a carrier in device and circuit modeling at Cadence design Software, which is one of the suppliers of circuit design suits. A Masters student is currently working on the project to complete the modeling for semi-ballistic PMOS transistors in GlobalFoundries 45 nm technology and near-ballistic NMOS and PMOS devices in GlobalFoundries 22 nm technology. Three undergraduate students have been involved in this research with one who developed models for passive components as a SURF student and two how will be developing models for PMOS transistors and PDK. GlobalFoundries and Murray Microwave has contributed to this research. GlobalFoundries has provided access to their technology at no cost, while Murray Microwave has performed noise measurements on these devices at microwave frequency at no cost.

References:

[1] Y. Shen, J. Cui and S. Mohammadi, "An Accurate Model for Predicting High Frequency Noise of Nanoscale NMOS SOI Transistors" *Solid-State Electronics,* Vol. 131, pp. 45-52, (May 2017), http://doi.org/10.1016/j.sse.2017.02.005 (*)

[2] Verilog-A model package for RF CMOS SOI transistors available at https://nanohub.org/groups/needs/compact_models (*)