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Penn State III-V Tunnel FET Model Manual
Version 1.0.1

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1 Introduction

We presented look-up table based Verilog-A models for III-V interband Tunnel Field Effect Transistors (TFETs) based on the calibrated TCAD Sentaurus [1] device simulations. The Verilog-A models can be further implemented to Spectre [2] circuit simulators. The calibrated TFET TCAD models serve as an approximation of full-band atomistic calculation of TFET band diagram and band-to-band tunneling current to generate the DC characteristics [3]. The gate-source and gate-drain capacitance characteristics obtained from the TCAD small-signal simulation has recently been validated with the measured transient characteristics of TFET [4, 5], which are employed for circuit-level transient analysis.

To improve the tunneling current, low bandgap materials (e.g. SiGe, Ge, InGaAs, InAs) have been widely explored for TFET prototype device design. The demonstrated double-gate III-V heterojunction TFET exhibits MOSFET-like on-current [6, 7, 8]. The improved gate-electrostatic control can further reduce the sub-threshold slope [9, 10]. Two types of III-V TFETs are considered for model development based on double-gate, ultra-thin body structure: InAs homojunction TFET and GaSb-InAs near-brokengap heterojunction TFET. Our Veriog-A models can capture TFET DC and transient operation for a wide range of operating voltages, which are suitable for various small-scale circuit designs and performance benchmarking (e.g. power consumption, energy-delay). Details of device calibration, look-up table generation and Verilog-A model implementation for circuit analysis are described in this manual.

2 III-V Tunnel FET (TFET) Device Simulation and Model Calibration

2.1 Tunnel FET Device Design and Simulation

TFETs have asymmetrical source/drain doping which operates as reverse-biased, gated p-i-n tunnel diodes. In TFETs, the on-off switching is enabled by the gate-voltage induced band-to-band tunneling (BTBT) at the source-channel tunnel junction. In conventional MOSFETs, only the carriers with energy exceeding the source-channel thermal barrier contribute to the on-state current. These carriers follow the Fermi-Dirac distribution with an energy slope of kT (where k is the Boltzmann constant, T is the absolute temperature), which induces a thermal limited sub-threshold slope of 60 mV/decade (~2.3kT/q at 300K, where q is the unite charge). In TFETs, the high energy carriers are filtered by the gate-controlled tunneling window. As a result, a sub-60 mV/decade SS, in principle, can be achieved in TFETs at the room temperature (300K) [11].

High on-state current (I_{on}), high on-off ratio and steep SS are critical aspects in TFET design, which allow the further scaling of the supply voltage (V_{DD}) for power consumption reduction without jeopardizing the performance. Tremendous progress has been made in TFET prototype demonstration with significant improvement of the tunneling limited I_{on} and reduction of SS. The design of TFET involves the tunneling barrier reduction (e.g.

low bandgap materials, hetero-band-alignment), gate electrostatics improvement (e.g. multi-gate or gate-all-around, ultra-thin body, effective oxide thickness (EOT) reduction), and low interface states to suppress the trap-assisted tunneling (TAT) [6-10]. III-V semiconductors are attractive for TFET fabrication due to their direct band-gaps and wide range of compositionally tunable band-alignment for tunnel barrier reduction. Previous work in [6, 7, 8] demonstrated III-V heterojunction TFET (HTFET) with MOSFET-like on-current through the reduction of effective tunneling barrier width while preserving the band-gap of the channel material to achieve a simultaneous enhancement of the on-off ratio. Benchmarking on beyond CMOS logic devices in [12] shows significant energy efficiency advantages in HTFET, where over 10^{15} Integer Ops/s/cm^2 with power consumption less that 1W/cm^2 can be achieved.
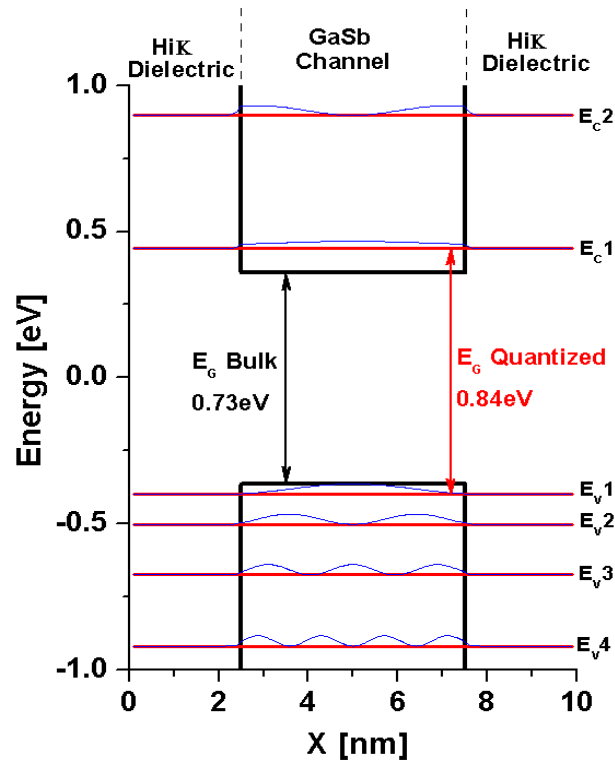
Figure 1. Example of the effective bandgap of GaSb due to quantization obtained from nextnano [14] simulation.

For TFET device simulation, the full-band atomistic simulation provides an accurate calculation of the band-to-band tunneling (BTBT) [13] for ideal device performance evaluation (e.g. defect free case). TCAD simulation serves as an approximation for the BTBT generation calculation based on the dynamic non-local tunneling model, which requires calibration with atomistic full-band simulation. Figure 1 shows an example to obtain material characteristics from nextnano simulation [14] as parameter input for TCAD Sentaurus to account for the quantization effect. This section will be focusing on the TCAD simulation for InAs homojunction TFET and GaSb-InAs heterojunction TFET, which are used to generate the look-up tables in Verilog-A models.

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2.2 InAs Homojunction TFET Model Calibration

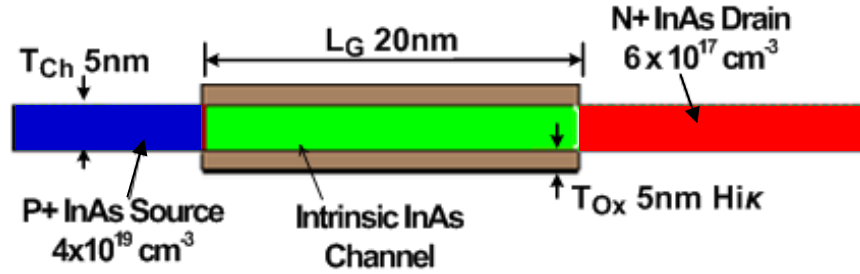**Double-gate InAs Homojunction Tunnel FET**

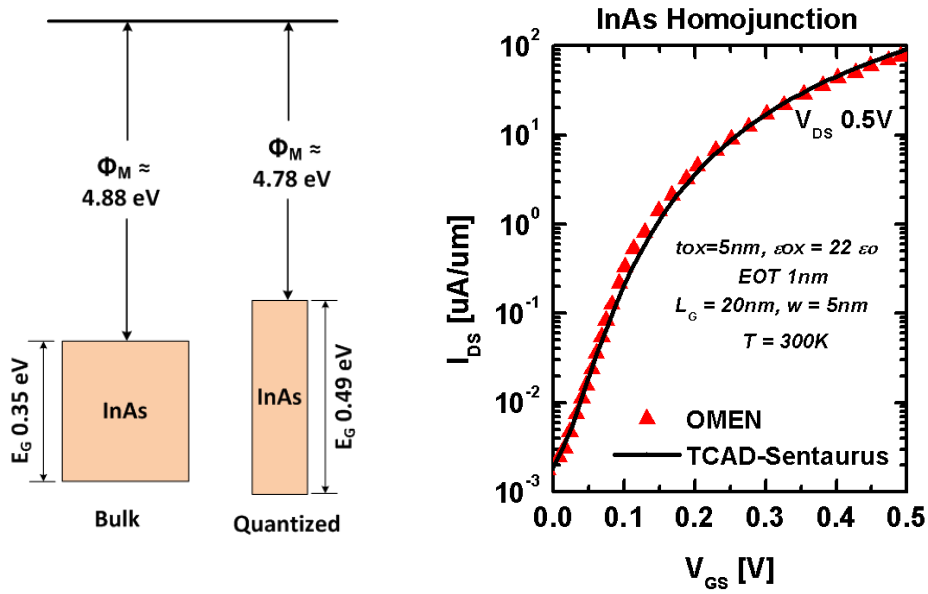**Figure 2.** InAs Homojunction Tunnel FET schematic.

Figure 3. InAs homojunction Tunnel FET DC characteristics calibration.

The double-gate InAs homojunction TFET schematic is shown in Figure 2 corresponding to the simulation structure in [22], which has a gate length (L_G) of 20 nm, ultra-thin body (T_{Ch}) of 5 nm, high-k dielectric thickness (HfO_2) of 5 nm at EOT of 1 nm with the source/drain doping of 4×10^{19} cm^{-3} (p+) and 6×10^{17} cm^{-3} (n+), respectively. The quantization induced bandgap broaden was obtained through nextnano simulation as described above in Figure 3. The calibrated DC characteristics show good agreement with the atomistic full-band simulation results [3].

2.3 GaSb-InAs Heterojunction TFET Model Calibration.

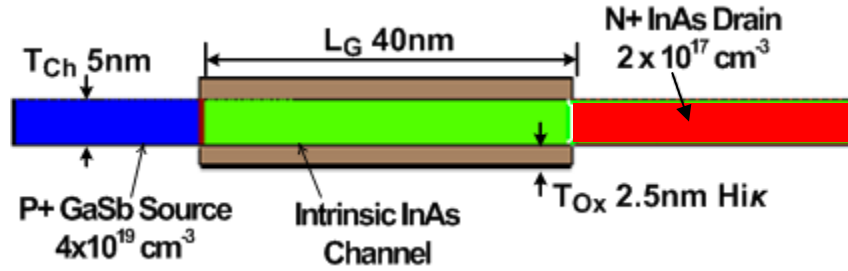**Double-gate GaSb-InAs Heterojunction Tunnel FET**

Figure 4. GaSb-InAs heterojunction Tunnel FET schematic.

Figure 4 shows the GaSb-InAs heterojunction FET schematic, which is calibrated with simulated structure in [3] with a gate length (L_G) of 40 nm, ultra-thin body (T_{Ch}) of 5 nm, high-k dielectric thickness (HfO_2) of 5 nm at EOT of 1 nm with the source/drain doping of $4x10^{19}$ cm^{-3} (p+) and $2x10^{17}$ cm^{-3} (n+) respectively. The quantized bandgap are shown in Figure 5 which agrees well with the OMEN simulation in [13]. The effective barrier height (E_{beff}) is 0.065 eV.
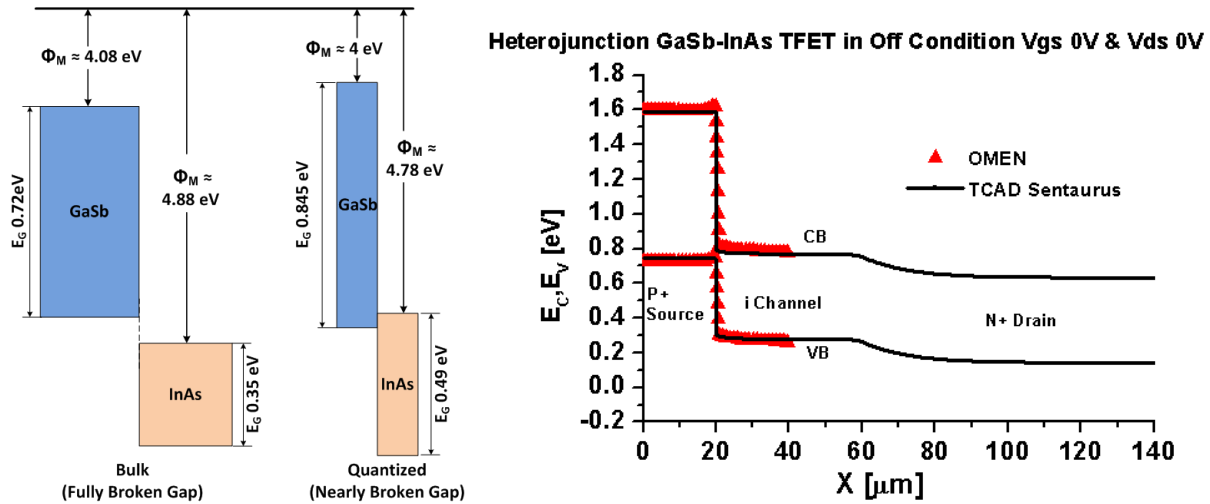
Figure 5. GaSb-InAs Heterojunction Tunnel FET D band diagram calibration. Omen simulation results are obtained from [13].

Figure 5 shows the calibration of DC characteristics obtained from TCAD simulation with OMEN simulation results. The current at 0.5 V V_{ds} shows good match at sub-threshold region and super-threshold region. Note that leakage current from TCAD simulation was 1 order lower. The Verilog-A model of GaSb-InAs HTFET uses 20 nm gate-length derived from this calibrated model.

Figure 6. GaSb-InAs heterojunction TFET DC characteristics calibration.

2.4 Capacitance Characteristics

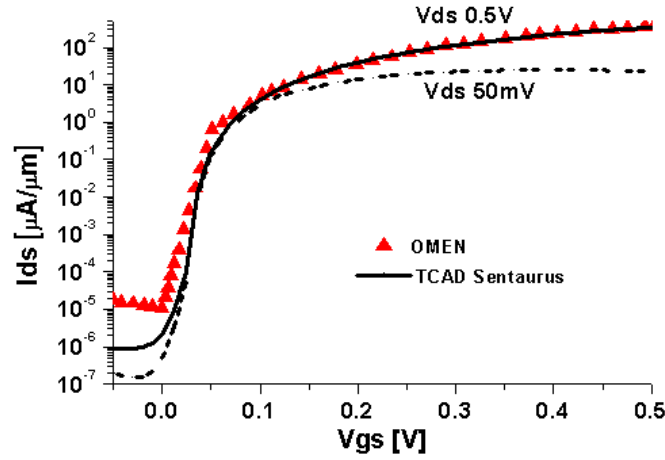Capacitance characteristics are critical for accurate device modeling. Due to the semi-classical simulation nature of TCAD, TFET gate-source C_{gs} and gate-drain capacitance C_{gd} characteristics obtained from the small signal simulation requires validation from transient measurements. [15] first reported the unique capacitance characteristics of TFET, which is known as enhanced on-state Miller capacitance effect, showing a dominant C_{gd} among the total capacitance C_{gg} at the device on-state ($V_{gs}=V_{DD}$). Such characteristics rises from the un-equal charge sharing between source and drain due to the tunnel-barrier, which results in a large "voltage spike" during transient analysis in TFET based inverter as compared to MOSFET case. Furthermore, Zhang et al [16] reported a Si TFET compact model based on the surface potential calculation, which shows the same observation (enhanced Miller capacitance effect) during transient analysis. Knoll et, al in [4] first reported the transient measurements of a Si nanowire TFET inverter, which further validates the effect of enhanced C_{gd} contribution to overall C_{gg}. Recently, Bijesh et al in [7] reported the first measured RF characteristics of fabricated near-broken gap III-V HTFET, showing a good match of the capacitance characteristics from TCAD with the extracted capacitance values, transconductance (g_m) and cut-off frequency (f_T) from S parameter measurements. More works [17, 18] have recently explored this unique capacitance characteristic of TFET. Based on the experiment validation, we obtain the capacitance characteristics of C_{gs} and C_{gd} using calibrated TCAD model to construct the TFET Verilog-A model. The capacitance characteristics of InAs TFET and GaSb-InAs HTFET are shown in Figure 7 and Figure 8.
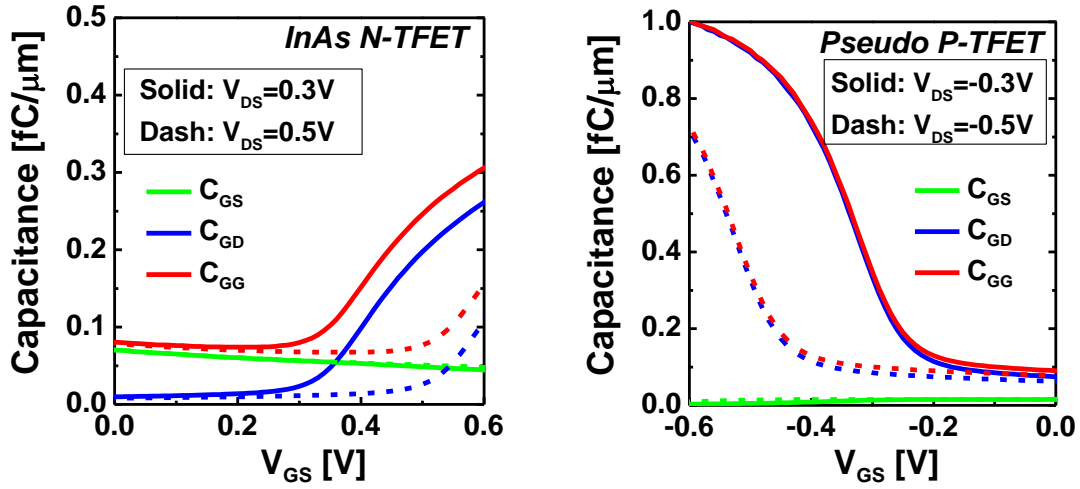
Figure 7. C_{gs}, C_{gd} vs V_{gs} characteristics for InAs homojunction TFET
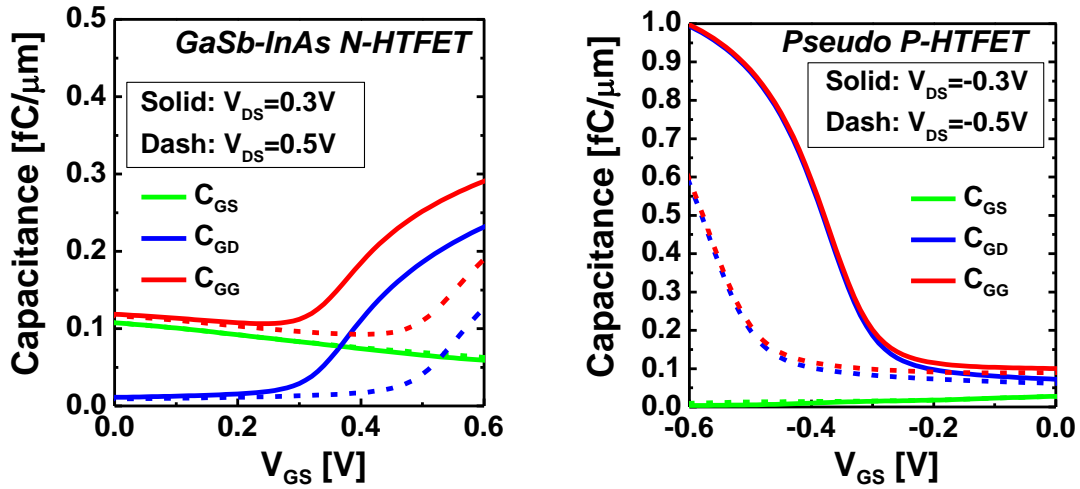

Figure 8. C_{gs}, C_{gd} vs V_{gs} characteristics for GaSb-InAs heterojunction TFET

2.5 Experimental Data Reference

Due to the lack of experimental data, the simulation model validation of the 20 nm GaSb-InAs heterojunction Tunnel FET remains challenging. Here, we present the validation of our simulation models at a channel length of 200 nm with the fabricated near-broken gap heterojunction TFET from [7]. Figure 9 shows the $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ material system and the vertical Tunnel FET schematic [7]. The device TEM cross-section is shown in Figure 10(a). Benefited from the near broken gap induced high band-to-band tunneling current density, a high drive current of 740 µA/µm is achieved at $V_{DS} = 0.5$ V (Figure 10(b-c)). The numerical simulation model has shown a good agreement with the measured I_{DS}-V_{GS} characteristics at T = 300 K, $V_{DS} = 0.5$ V using interface states density (D_{it}) of $5 \times 10^{12} \text{cm}^{-2}\text{eV}^{-1}$ as shown in Figure 11(a-b).
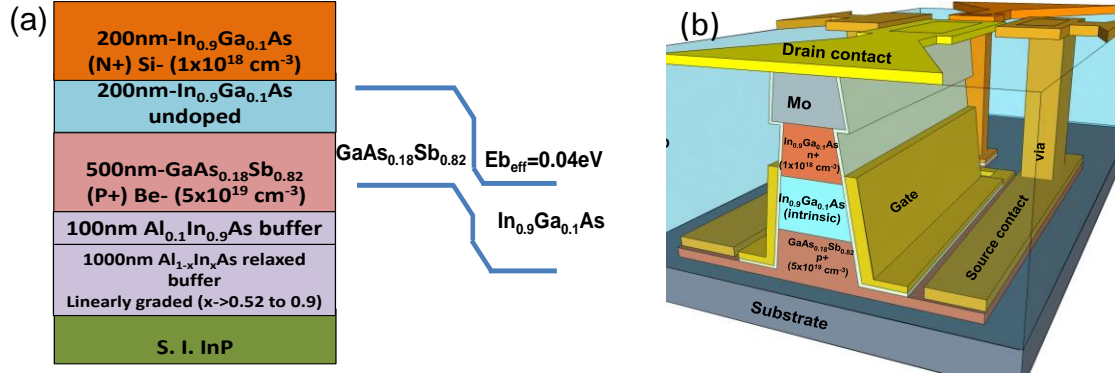
Figure 9. The near-broken gap In$_{0.9}$Ga$_{0.1}$As/GaAs$_{0.18}$Sb$_{0.82}$ heterojunction n-type Tunnel FET (a) material system and device schematic [7].
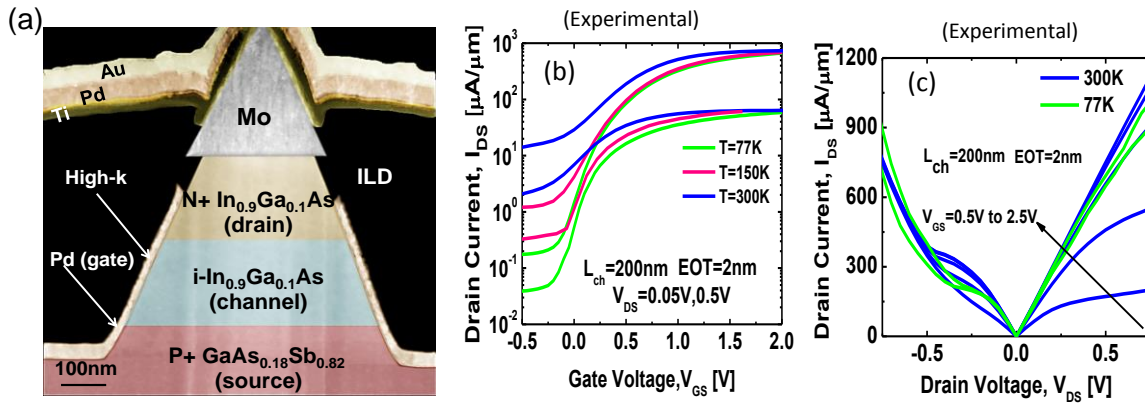
Figure 10. (a) Cross-section TEM image of the fabricated HTFET showing angled sidewall and gate-drain overlap. (b) Temperature dependent transfer characteristics of HTFET showing improved I$_{ON}$/I$_{OFF}$ at low temperature (c) Output characteristics of HTFET at T=300K and T=77K [7].

To validate the capacitance characteristics of the TCAD models, the RF measurement has been carried out with a coplanar ground-signal-ground (GSG) waveguide structure. Figure 12(a-c) shows the measured and modeled scattering parameters (S-parameters) to extract the cut-off frequency (F$_T$) and capacitance values. The 200 nm HTFET exhibits a measured F$_T$ of 10 GHz and 19 GHz at V$_{DS}$=0.3V and 0.5V respectively. TCAD simulation of the HTFET device structure matched to the TEM image has been used taking into account parasitic capacitances and resistances. The capacitance characteristics and F$_T$ of the TCAD models are obtained from the small signal simulation. The simulated C$_{gs,extrinsic}$, C$_{gd,extrinsic}$ values, as well as the F$_T$ are in agreement with the measured values from RF measurements, as shown in Figure 13 [7]. The measured I$_{DS}$-V$_{GS}$ characteristics and simulation results are available in the experiment data folder.

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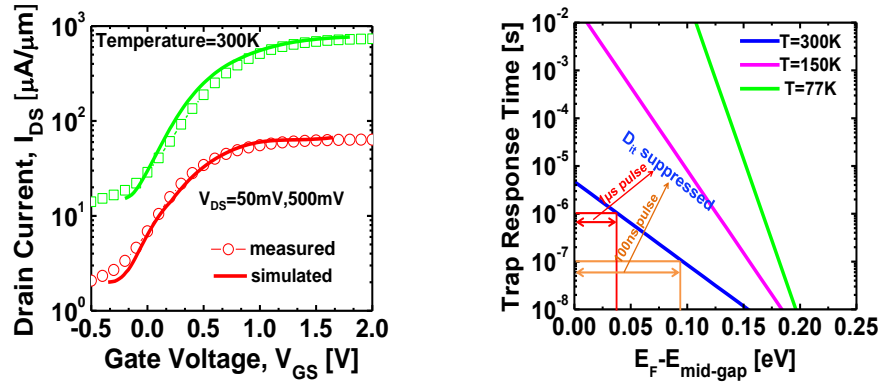
Figure 11. (a) TCAD simulation and measured characteristics at T=300K. (b) Simulated electron trap response time in $In_{0.9}Ga_{0.1}As$ is used to estimate gate voltage pulse width required to suppress D_{it}.
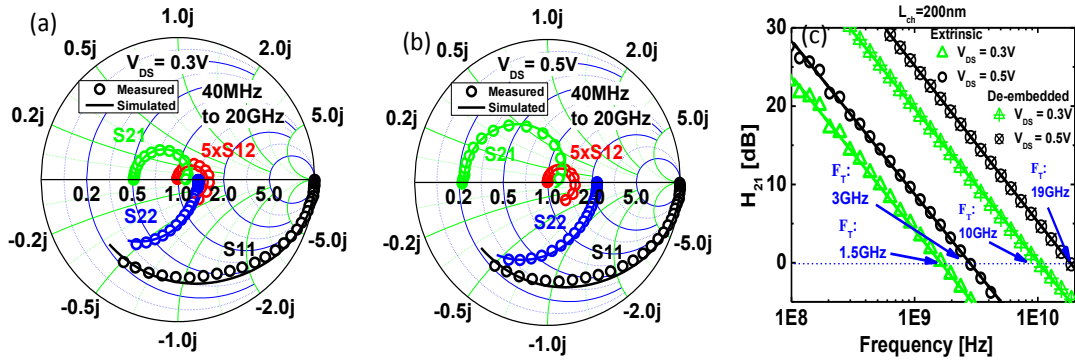
Figure 12. (a-b) Modeled and measured s-parameters at V_{DS} = 0.3 V and 0.5 V respectively (c) Measured and modeled H_{21} parameter at V_{DS} = 0.5 V and 0.3 V. After de-embedding, F_T of 10GHz and 19 GHz are measured at V_{DS}=0.3 V and 0.5V respectively [7].
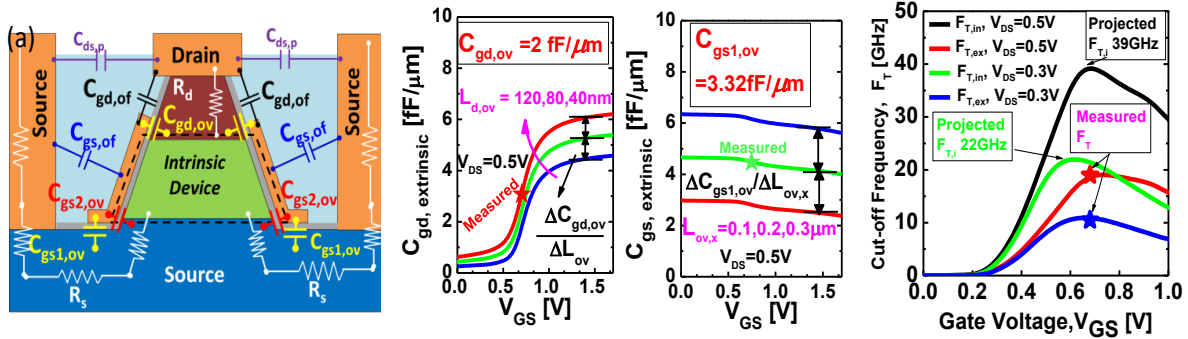
Figure 13. (a) 2D schematic of the simulated HTFET with dimensions calculated from the TEM with parasitic capacitances and resistance illustration. Extraction of (b) gate-drain overlap capacitance $C_{gd,ov}$ (c) lateral gate-source overlap capacitance $C_{gs1,ov.}$ (d) Measured F_T is in agreement with the simulations. After de-embedding the overlap capacitances, HTFET with L_{ch}=200nm is expected to achieve F_T of 22GHz and 39GHz at V_{DS}=0.3V and 0.5V respectively.

3 TFET Verilog-A Models

3.1 Look-up Table based Verilog-A Model

Lookup table-based Verilog-A model has been employed for TFET-based circuit designs in many literatures [3, 19, 20, 21]. Here we show the schematic of the Verilog-A transistor model in Figure 9 from [3]. It is a lookup table-based model composed of two-dimentional tables: the transfer characteristics $I_{ds}(V_{ds}, V_{gs})$, the gate-source capacitance $C_{gs}(V_{gs}, V_{ds})$ and the gate-drain capacitance $C_{gd}(V_{gs}, V_{ds})$ across a range of fine-step drain-source voltage bias V_{ds} and gate-source voltage bias V_{gs}. The TCAD models used for lookup table generation are the same as those shown in the previous Section 2, except that the gate lengths are all set to $L_G = 20$ nm. The parasitic series resistance and parasitic external capacitance are not included in the TCAD model, which can be added at the circuit level as shown in the schematic above.
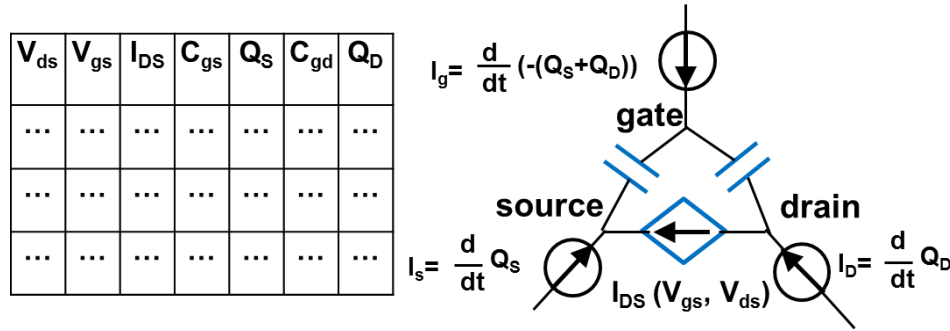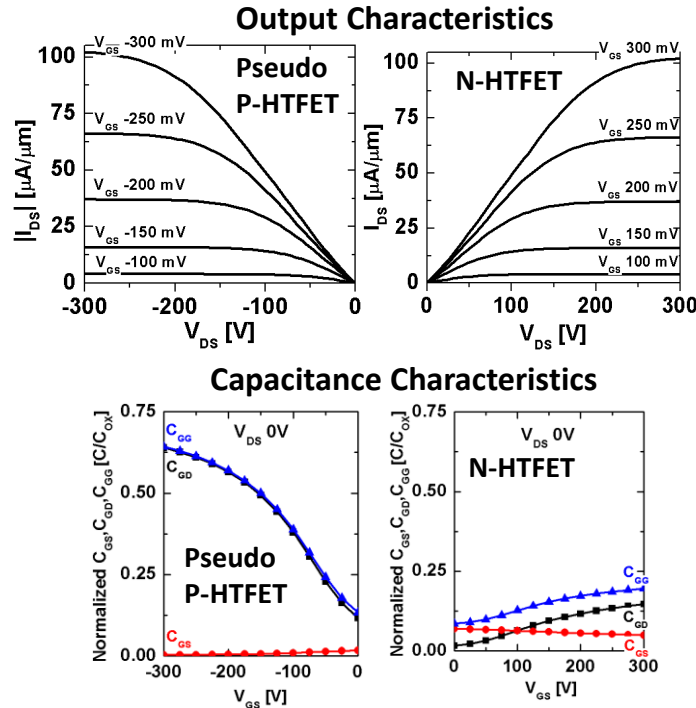

Figure 9. Verilog-A model schematic.

Figure 10. Device characteristics comparison.

Due to the ongoing efforts of p-type Tunnel FET development, we assume identical drive-currents for the n-channel and p-channel transistors in TFET Verilog-A models for the optimal circuit performance. We should notice that the Density-of-States (DoS) of electrons and holes can be quite different in III-V materials, such that the gate-capacitance characteristics need to be obtained from TCAD simulation for n-type and p-type TFET, respectively, to accurate modeling the circuit performance. We develop a symmetrical device structure as n-type TFET to obtain the capacitance characteristics for pseudo p-type TFET. The p-type and n-type device characteristics of GaSb-InAs TFET are shown in Figure 10.

3.2 Model Description (Ver. 1.0.1)

The Verilog-A model is coded in ".va" file, which contains the following files:

Wrapper File		homotfet.va (for InAs Homojunction TFET); heterotfet.va (for GaSb-InAs Heterojunction TFET)
Master Model File		tfet_master.va
Look-up Tables	InAs Homojuntion TFET	IdVg-InAs-NTFET-Lg-20nm.tbl, CGS-InAs-NTFET-Lg-20nm.tbl, CGS-InAs-PTFET-Lg-20nm.tbl, CGD-InAs-NTFET-Lg-20nm.tbl, CGD-InAs-PTFET-Lg-20nm.tbl;
	GaSb-InAs Heterojunction TFET	IdVg-GaSb-InAs-HNTFET-Lg-20nm.tbl, CGS-GaSb-InAs-HNTFET-Lg-20nm.tbl, CGS-GaSb-InAs-HPTFET-Lg-20nm.tbl, CGD-GaSb-InAs-HNTFET-Lg-20nm.tbl, CGD-GaSb-InAs-HPTFET-Lg-20nm.tbl;

The key features of this model bundle are:
(1) "tfet_master.va" combined all the model features for n-type and p-type homojunction and heterojunction TFETs. 'ifdef has been used to enable HOMOJUNCTION and HETEROJUNCTION features.
(2) "homotfet.va" and "heterotfet.va" recall "tfet_master.va" to enable different types of TFETs (e.g. "homotfet.va" enables "_HOMOJUNCTION_" for InAs Homojunction TFET in "tfet_master.va", while "heterotfet.va" enables "_HETEROJUNCTION_" for GaSb-InAs Heterojunction TFET in "tfet_master.va".
(3) In "tfet_master.va", a parameter, "type", has used to define n-type and p-type transistors, which needs to be specify in the circuit netlist.

The master model file "tfet_master.va" is as follows:

****

```
`include "constants.vams"
`include "disciplines.vams" // Header files, using Verilog-A language to describe a module
function

module TFET(d,g,s);
inout d,g,s;
electrical g,d,s; // Device module name and terminal definition

real Ids, Cgs, Cgd,Qg, Qs, Qd; // Variables used in modeling.
parameter real W=1 from (0:inf); //Device width "W", in micrometer unit.
parameter string type = "n" from '{"n", "p"}; // Parameter "type" to specify n-type or
p-type TFET.
integer direction; // Variable to specify the current direction in n-type or p-type TFET.

//Verilog-A model main body
analog begin

`ifdef _HETEROJUNCTION_  // GaSb-InAs Heterojunction TFET
//n-type TFET, reading current Ids, capacitance Cgs and Cgd values from look-up tables
(tables are generated from Sentaurus TCAD simulation), current direction is 1. Variable
values assigned from the lookup tables in ".tbl" are according to terminal voltage
condition. In each table, the 1st column is Vds, 2nd column is Vgs, 3rd column is the
current or capacitance value.
if (type == "n") begin
Ids=$table_model(V(d,s), (V(g,s)), "IdVg-GaSb-InAs-HNTFET-Lg-20nm.tbl","1LL,1LL");
Cgd=$table_model(V(d,s), (V(g,s)), "CGD-GaSb-InAs-HNTFET-Lg-20nm.tbl","1LL,1LL");
Cgs=$table_model(V(d,s), (V(g,s)), "CGS-GaSb-InAs-HNTFET-Lg-20nm.tbl","1LL,1LL");
direction =1;
end

//p-type TFET, reading current Ids, capacitance Cgs and Cgd values from look-up tables
(tables are generated from Sentaurus TCAD simulation), current direction is -1.
else if (type == "p") begin

// We assume that the PTFET and NTFET drive currents are similar
Ids=$table_model(-V(d,s), (-V(g,s)), "IdVg-GaSb-InAs-HNTFET-Lg-20nm.tbl","1LL,1LL");
```

// We do not assume that the PTFET and NTFET gate capacitances are similar because the hole and electon DoS in InAs are significantly different

```
Cgd=$table_model(V(d,s), (V(g,s)), "CGD-GaSb-InAs-HPTFET-Lg-20nm.tbl","1LL,1LL");
Cgs=$table_model(V(d,s), (V(g,s)), "CGS-GaSb-InAs-HPTFET-Lg-20nm.tbl","1LL,1LL");
direction = -1;
end

`else `ifdef _HOMOJUNCTION_ // InAs Homojunction TFET
```

//Similarly, reading variable values from look-up tables, specify the current direction according to the "type".

```
if (type == "n") begin
Ids=$table_model(V(d,s), (V(g,s)), "IdVg-InAs-NTFET-Lg-20nm.tbl","1LL,1LL");
Cgd=$table_model(V(d,s), (V(g,s)), "CGD-InAs-NTFET-Lg-20nm.tbl","1LL,1LL");
Cgs=$table_model(V(d,s), (V(g,s)), "CGS-InAs-NTFET-Lg-20nm.tbl","1LL,1LL");
direction =1;
end

else if (type == "p") begin
Ids=$table_model(-V(d,s), (-V(g,s)), "IdVg-InAs-NTFET-Lg-20nm.tbl","1LL,1LL");
Cgd=$table_model(V(d,s), (V(g,s)), "CGD-InAs-PTFET-Lg-20nm.tbl","1LL,1LL");
Cgs=$table_model(V(d,s), (V(g,s)), "CGS-InAs-PTFET-Lg-20nm.tbl","1LL,1LL");
direction = -1;
end
`endif
```

//Calculate the charge Qgd, Qgs and Qg according to the capacitances, device width and the terminal voltages. Calculate the terminal current with respect to the charge.

```
    Qd = (W*-1*Cgd)*(V(g,d));
    Qs = (W*-1*Cgs)*(V(g,s));
    Qg=-1*(Qd+Qs);
    I(d,s) <+ direction*Ids*W ;
    I(g) <+ ddt(Qg);
    I(s) <+ ddt(Qs);
    I(d) <+ ddt(Qd);

end
endmodule
```

3.3 Terminal and Voltage Definition for Intrinsic Device

N-TFET   **P-TFET**
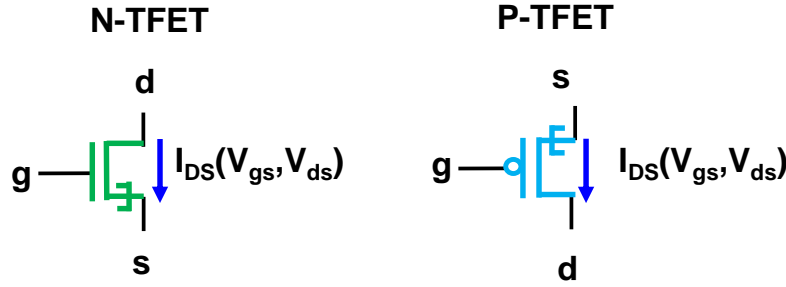
Figure 11. Terminal definition N-type TFET and p-type TFET and direction.

As shown in Figure 11, the intrinsic Tunnel FET (as shown in the dashed box in Figure 9) has 3 terminals: source (**s**), gate (**g**) and drain (**d**). No body terminal in this model due to the double-gate, ultra-thin-body device structure. The terminal voltage V(g,s) and V(d,s) identify the device operation and determine I_{ds}, C_{gs} and C_{gd} at such V_{gs} and V_{ds} bias through the look-up tables:

```
****************************************************************************************
    module TFET(d,g,s);
    inout d,g,s;
    electrical g,d,s;
    real Ids, Cgs, Cgd, Qs, Qd, Qg;
        Ids=$table_model(V(d,s), (V(g,s)), "IdVg-NTFET_Lg20nm.tbl","1LL,1LL");
        Cgd=$table_model(V(d,s), (V(g,s)), "CGD-NTFET_Lg20nm.tbl","1LL,1LL");
        Cgs=$table_model(V(d,s), (V(g,s)), "CGS-NTFET_Lg20nm.tbl","1LL,1LL");
****************************************************************************************
```

3.4 DC Characteristics

The device DC current is directly obtained from the table value and device width (W**)** definition, and current direction (direction):

```
****************************************************************************************
    parameter real W=1;
    integer direction;
    direction=1;
      I(d,s) <+ direction*Ids*W;
****************************************************************************************
```

3.5 Transient Characteristics

The device transient characteristics are obtained through charge models. Terminal charge of Q_{gd} (drain charge) and Q_{gs} (source charge) are calculated using C_{gd} and C_{gs} obtained from lookup tables and terminal voltages V_{gd} and V_{gs}, respectively. Since the

DC component of I_{gd} and I_{gs} are negligible, the transient current I_{gd} and I_{gs} are calculated according to the time evolution of the terminal charges:

```
************************************************************************************
Qd = (-1*W*Cgd)*(V(g,d));
Qs = (-1*W*Cgs)*(V(g,s));
Qg=-1*(Qd+Qs);
I(d,s) <+ direction*Ids*W ;
I(d) <+ ddt(Qd);
I(s) <+ ddt(Qs);
I(g)<+ddt(Qg);
************************************************************************************
```

3.6 Pseudo P-TFET

The pseudo P-TFET model uses the Ids table of NTFET with P-TFET Capacitance characteristics:

```
************************************************************************************
if (type == "p") begin
Ids=$table_model(-V(d,s), (-V(g,s)), "IdVg-NTFET-Lg-20nm.tbl","1LL,1LL");
Cgd=$table_model(V(d,s), (V(g,s)), "CGD- PTFET-Lg-20nm.tbl","1LL,1LL");
Cgs=$table_model(V(d,s), (V(g,s)), "CGS- PTFET-Lg-20nm.tbl","1LL,1LL");
direction = -1;
end
************************************************************************************
```

4   Example Circuits and Spectre Simulation Results

The TFET Verilog-A device model can be implemented in Spectre simulation. In order to execute the circuit simulations you need to have Virtuoso Spectre Circuit Simulator [2] installed. We present the following examples of using TFET Verilog-A model to obtain device Id-Vg characteristics, TFET based FO1 Inverter and Ring Oscillator simulation. The simulation projects are available with the model download as ".scs" files.

4.1 Id-Vg simulation: DC Analysis Example

The Id-Vg simulation for NTFET is in ntfet_idvg.scs. Run by:
>spectre ntfet_idvg.scs
Note that, for InAs Homojunction TFET, use ahdl_include "homotfet.va"; for GaSb-Heterojunction TFET, use ahdl_include "heterotfet.va".

```
************************************************************************************
// Simulation language is Spectre.
simulator lang=spectre
global 0
```

//Terminal voltages of VG and VD are defined as parameters. Device width is defined Width=1 um. Series resistance R_{Series} of 55 Ohm-um is used as parameter

parameters VG=0.0

parameters VD=0.3

parameters Width=1

parameters RSeries=55

//3 dc voltage sources V1, V2 and V3 are defined and connected to source, gate, and drain node.

V1 (source 0) vsource type=dc dc=0

V2 (gate 0) vsource type=dc dc=VG

V3 (drain 0) vsource type=dc dc=VD

// R1 and R2 are the parasitic resistances I1 is the instance of an intrinsic NTFET with a width W=Width, where nodes d1, gate and s1 are connected to the device d, g, s terminals respectively. Parasitic resistance R1 and R2 are connected to NTFET's s and d, respectively.

R1 (source s1) resistor r=RSeries/Width

//Specify type=n for NTFET

I1 (d1 gate s1) TFET type=n W=Width

R2 (drain d1) resistor r=RSeries/Width

dc dc param=VG start=0 stop=0.3 lin=100 oppoint=rawfile maxiters=150 \

maxsteps=10000 annotate=status

// Divide by two in order to report the current per micrometer. Since the simulator gives the double gate current

//print gate*1000, -I(V3)*1e6/2, name=dc addto="idvg_heterotfet.out"

print gate*1000, -I(V3)*1e6/2, name=dc addto="idvg_homotfet.out" //Print to file

//ahdl_include "heterotfet.va" //Using ahdl to compile Verilog-A model

ahdl_include "homotfet.va" //Using ahdl to compile Verilog-A model

****

The simulation results of InAs Homojunction TFET are plotted in Figure 12.

InAs NTFET I_d-V_g simulation
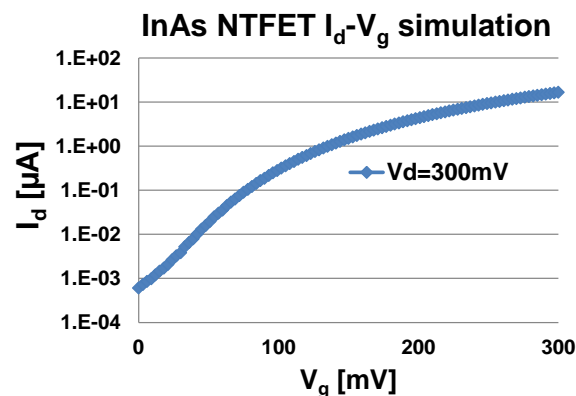
Figure 12. Id-Vg of InAs N-TFET with source/drain series resistance of 55 ohm at V_{DS}=0.3V.

4.2 TFET based Inverter: Transient Analysis Example

The 5-stage FO1 inverter chain simulation using InAs TFET is in inverter_InAs_tfet_FO1.scs. Run by:

>spectre inverter_ tfet_FO1.scs

Note that, for InAs Homojunction TFET, use ahdl_include "homotfet.va"; for GaSb-Heterojunction TFET, use ahdl_include "heterotfet.va".

****

// Series resistance of 55 ohm-um and output parasitic capacitance 0.1 fF/um are included. Minimum device width W_{Min}=20 nm is used for simulation at V_{DD}=0.3V.

parameters VSUPPLY=0.3 INPUT=0

parameters RSeries=55

parameters CParasitic=100e-18

parameters WMin=0.02

V1 (supply1 0) vsource type=dc dc=VSUPPLY

V2 (gnd 0) vsource type=dc dc=0

V3 (in1   0) vsource type=pwl wave=[0 0 1n 0 1.05n VSUPPLY 3n VSUPPLY 3.5n 0 5n 0]

//5-stage FO1 inverter chain

X1   (out1 in1 supply1 gnd) inv

X2   (out2 out1 supply1 gnd) inv

X3   (out3 out2 supply1 gnd) inv

X4   (out4 out3 supply1 gnd) inv

X5   (out5 out4 supply1 gnd) inv

// Sub-circuit definition for TFET inverter which has 4 terminals: out, in, supply, gnd. Series resistance is added to PTFET and NTFET. Parasitic capacitance is added to the inverter output.

subckt inv out in supply gnd

17

```
// R1 R2 R3 and R4 are the parasitic resistances
R1  (o1 out) resistor r=RSeries/WMin
I1  (o1  in s1) TFET type=p W=1*WMin
R2  (s1 supply) resistor r=RSeries/WMin
R3  (o2 out) resistor r=RSeries/WMin
I2  (o2  in gnd2) TFET type=n W=1*WMin
R4  (gnd2 gnd) resistor r=RSeries/WMin


// C1 is the parasitic output capacitance
C1 (out 0) capacitor c=CParasitic*WMin
ends
// Initial condition is given to inverter chain internal nodes.
ic out1=VSUPPLY out2=0 out3=VSUPPLY

tran  tran  stop=5n  write="spectre.ic"  writefinal="spectre.fc"  annotate=status\
maxiters=5 autostop=yes
print        in1*1000,out1*1000,out2*1000,out3*1000,out4*1000,          name=tran\
addto="inv_tran.out"

//ahdl_include "heterotfet.va" //switch to heterotfet
ahdl_include "homotfet.va" //switch to homotfet
*********************************************************************************
```
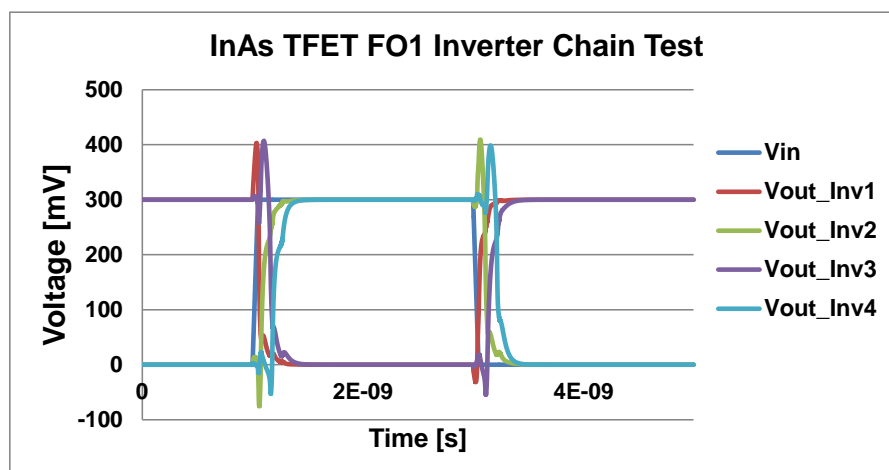
The simulation results are plotted in Figure 13.

Figure 13. Input and Output Waveforms of InAs TFET inverter with minimum sizing at V_{DS}=0.3V.

The measurement simulation to obtain fall-delay, fall-energy, rise-delay and rise-energy for signal-stage inverter can be obtained by running:

>spectremdl –b inverter_ tfet_FO1.mdl –d inverter_ tfet_FO1.scs –measure inverter_ tfet_FO1.measure

The output results (energy vs V$_{DD}$, delay vs V$_{DD}$) of InAs Homojunction TFET are shown in Figure 14.
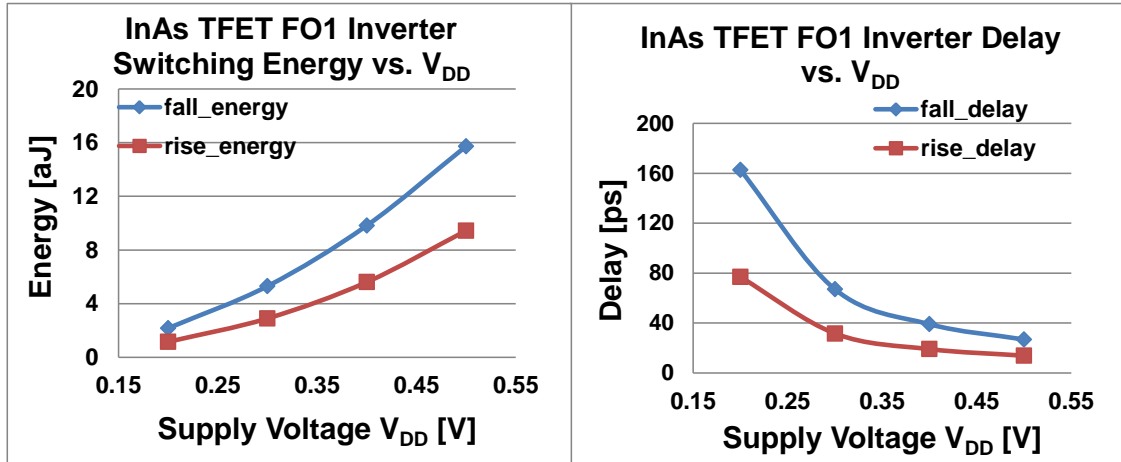

Figure 14. InAs TFET FO1 Inverter Switching Energy and delay vs. supply voltage V$_{DD}$.

4.3 HTFET based Ring Oscillator: Transient Analysis Example

Similarly, the 15-stage FO1 inverter chain simulation using GaSb-InAs HTFET is in ring_oscillator.scs. Run by:

>spectre ring_oscillator.scs

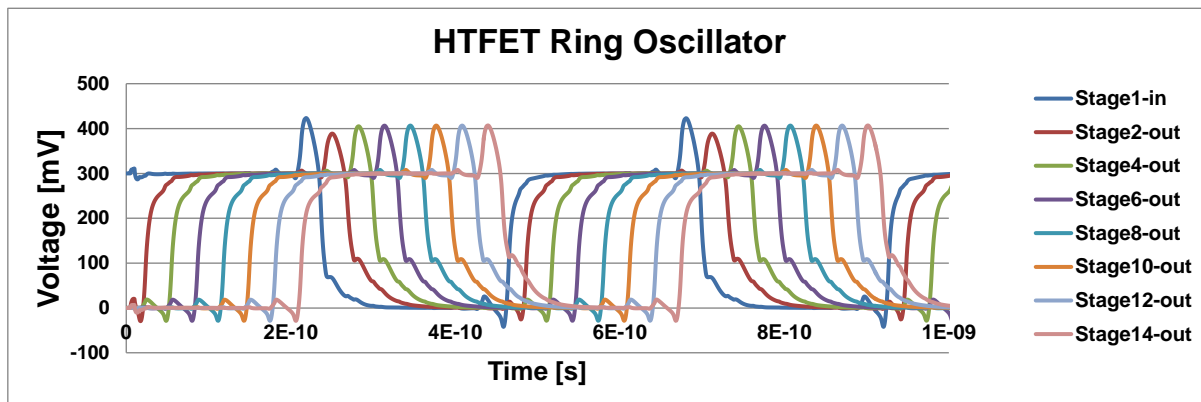The simulation results are plotted in Figure 15.

Figure 15. Input and output waveforms of GaSb-InAs HTFET NAND based ring oscillator at V$_{DS}$=0.3V.

The measurement simulation to obtain fall-delay, fall-energy, rise-delay and rise-energy for signal-stage inverter can be obtained by running:

>spectremdl   –b   ring_oscillator.mdl   –d   ring_oscillator.scs   –measure ring_oscillator.measure

The simulation results are plotted in Figure 16:
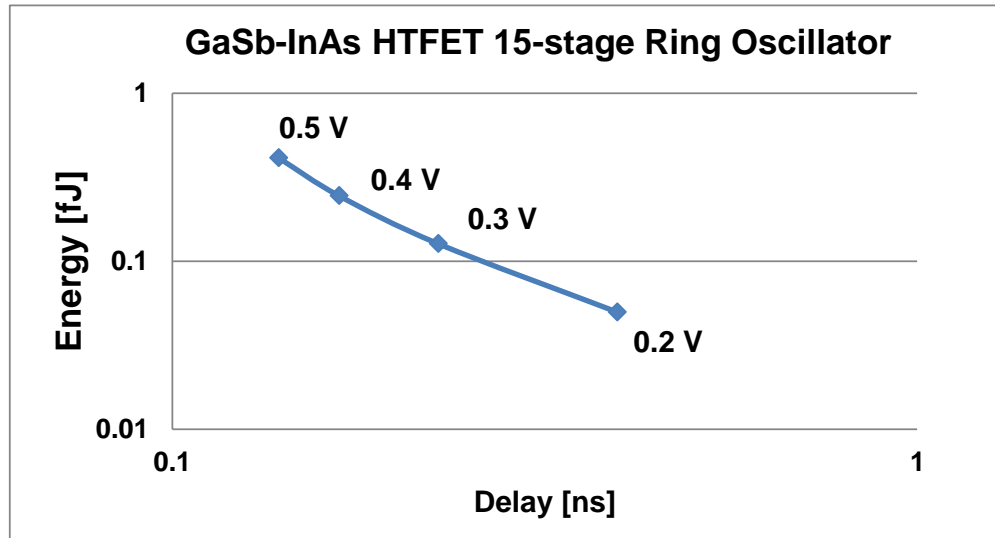
Figure 16. Energy vs delay of the GaSb-InAs HTFET NAND based ring oscillator at different supply voltage V_{DD}.

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