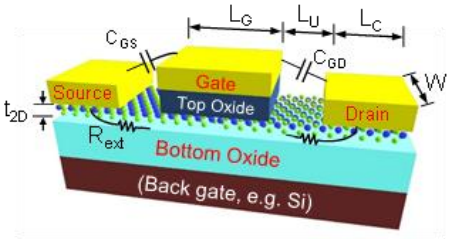
Stanford 2D Semiconductor (S2DS) model

Version: 1.2.0



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Introduction

Extended derivation and model implementation are discussed in Ref. [1].

We present a physics-based compact model for two-dimensional (2D) field-effect transistors (FETs) based on monolayer semiconductors such as MoS_2. A semi-classical transport approach is appropriate for the 2D channel, enabling simplified analytical expressions for the drain current. In addition to intrinsic FET behaviour, the model includes contact resistance, traps and impurities, quantum capacitance, fringing fields, high-field velocity saturation and self-heating, the latter being found to play a strong role. The model is calibrated with state-of-the-art experimental data for n- and p-type 2D-FETs, and it can be used to analyse device properties for sub-100 nm gate lengths. Using the experimental fit, we demonstrate feasibility of circuit simulations using properly scaled devices. The complete model is implemented in SPICE-compatible Verilog-A, and a downloadable version is freely available on the nanoHUB.org.

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Voltage definitions

The voltage definitions are like MVS model [2]. To account for the direction of the current flow, we are using a variable '*dir*'. Under normal operation, the '*dir*' is equal to 1.

For the terminal characteristics, gate (*g*), source(*s*) and drain (*d*) are the output nodes with bidirectional properties. Though the device has an additional back-gate, we have not included it in the list of the nodes. The back gate is accounted for by a variable V_{BS} . *si and di* are internal nodes for the FET. We have defined nodes *a1*, *a2* and *gnd* as internal nodes for calculation of surface potential at drain and source end. The thermal calculations are taken care by a thermal node *dt.* The branch definitions are given as follows.

```
Vgsraw      =   type * ( V(g , si) );
Vgdraw      =   type * ( V(g , di) );
if (Vgsraw >= Vgdraw) begin
    Vds     =   type * ( V(d , s) );
    Vgs     =   type * ( V(g , s) );
    Vdsi    =   type * ( V(di , si) );
    Vgsi    =   Vgsraw;
    Vgdi    =   Vgdraw;
    dir     =   1;
end
else begin
    Vds     =   type * ( V(s , d) );
    Vgs     =   type * ( V(g , d) );
    Vdsi    =   type * ( V(si , di) );
    Vgsi    =   Vgdraw;
    Vgdi    =   Vgsraw;
    dir     =   -1;
end
```

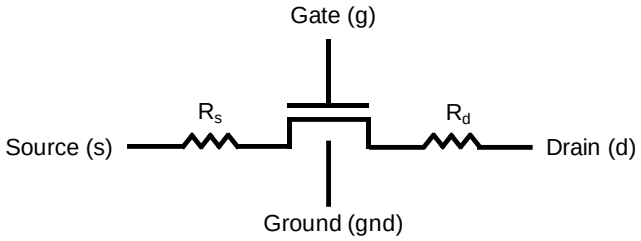

Figure 1: Schematic showing the nodes definition in the model

List of the key parameters:

Parameter	**Default value**	**Definition**
W	1e-6 m	Width of transistor
LG	9.4e-6 m	Gate length
LOV	0 m	Overlap length
L	9.4e-6 m	Effective gate length
TS	0.65e-9 m	Semiconductor thickness
TTOP	17.5e-9 m	Thickness of top oxide
TBOX	270e-9 m	Thickness of bottom oxide
tp	40e-9 m	Thickness of gate metal
NSUB	1e12 cm^{-2}	Impurity density
Dit	1e10 cm^{-2}	Trap density at semiconductor-oxide interface
Vgs0_e, Vgs0_h	0.6	Flatband voltage for top metal
me_e, me_h	$0.45m_O$, $0.64m_O$	Effective mass for electron and hole in 'K' valley
Rce, Rch	5000 Ω·μm	Contact resistance
eps_t	12.5	Relative permittivity of top gate dielectric
eps_b	3.9	Relative permittivity of bottom gate dielectric
Cif, Cof	1e-12	Inner and outer fringe capacitance
kox	1.4	Thermal conductivity of bottom oxide (SiO_2)
ksi	100	Thermal conductivity of substrate (Si)
Rcox	1.2e-8	Thermal resistance of semiconductor and bottom oxide contact
lambda	0.2	Adjust for output resistance

Flags

Name	Function
str	The structure of the device (1 = double-gate)
type	Type of device 1 = nFET, -1 = pFET
SELFHEAT	'1' will include the self-heating effect
HIFIELD	Will include high drain field effect in mobility
GATEFIELD	'1' will include the gate field effect on mobility

Key parameter definition

The important parameters and nuances have been explained below.

Dimensions and material properties: The dimensions for the device are available from the foundry or laboratory experimental studies. The devices produced in university fabs may not have well defined rectangular dimensions. In such cases, we choose effective width and effective lengths for these devices. The material properties like dielectric constant, effective masses are taken from the available (theory) publications. However, care should be taken in choosing these values.

Mobility: Mobility has a strong relation to various factors including dielectric constant of the gate oxide, the gate voltage, and electric field. S2DS model uses effective mobility and incorporates effect of temperature, high field, and gate dependence.

Band-structure: For MoS_2, S2DS assumes a two-valley conduction band. This may not be universally true for other 2D materials. So, care should be taken while using this model to model other 2D materials.

The model has been developed for monolayer semiconductor with direct band gap. But it should be easily extended to few layered materials as well.

Effective mass: The density of state calculation depends strongly on the effective masses of the materials. We chose to use the most accepted effective masses $0.45m_o$ for electrons MoS_2 and $0.64m_o$ for holes in WSe_2. However, due to uncertainty in extracting in these value, effective mass can also be treated as fit-parameters.

Modeling details

(*The text for this section is taken from Ref.* [1])

S2DS models a FET shown in Fig. For the sake of concreteness, a typical device structure considered in this work includes the 1L material on an insulator (e.g. the bottom oxide shown in Fig. 1), a top-gate oxide and gate metal stack on top. A finite underlap distance (L_U) appears between the edge of the top-gate and the source and drain contacts, respectively. The contacts themselves have a finite length L_C, which can play a role when this becomes comparable to the current transfer length [3]. Beneath the bottom oxide, the substrate can be conductive as a doped Si wafer (which is often used as a back-gate in experiments), or insulating like glass, quartz, or a flexible polymer.

To simplify the analysis, we present equations for n-type transistors (n-FET),

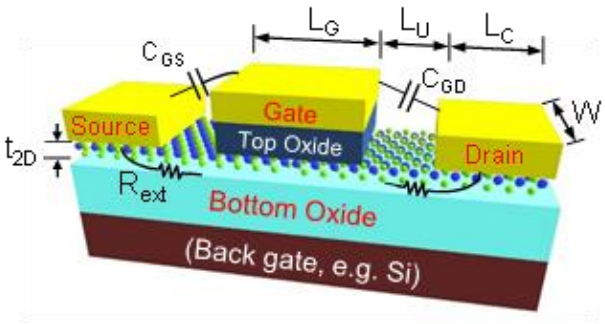

Figure 2: Schematic of a representative 2D semiconductor FET, including its parasitic elements. Here, the channel is a monolayer semiconductor such as MoS_2. The channel thickness and the width are represented by t_{2D} and W respectively. L_G is the gate length, L_U is the underlap length, and L_C is the length of the source and drain contacts. C_{GS} and C_{GD} are the capacitances from gate to source and to drain, respectively. R_{ext} is the total external resistance that includes the contact resistance (R_C) and the resistance of the underlap region (R_U). The substrate can be doped Si, functioning as a back-gate, or it could be an electrically insulating polymeric flexible substrate. For a 2D material, integrating the available state over an energy for a applied voltage, we can get the total amount of charge store in the channel.

considering electron transport in the channel and positive voltages (V_{GS}, $V_{DS} > 0$). Of course, these can be easily modified to simulate p-type transistors (p-FET), as is done for inverter simulations in the latter part of this study. We build on the model developed by Jiménez to derive the current-voltage (*I*-*V*) characteristics, with several extensions described below, particularly with respect to "extrinsic" transistor aspects, including self-heating, velocity saturation, and fringing fields.[4], [5]

First, we include the effect of the band structure for charge calculation. For example, in most TMDs (including MoS_2) two conduction band valleys may participate in transport, one at the K point and the other halfway along the K and Γ points of the Brillouin zone, sometimes labelled the Q valley.[6]–[8] Figure 2a shows the schematic of this band structure, where ΔE_{KQ} is the energy separation between the K and Q conduction band valleys. We calculate the charge density as

$$n_{2D} = \int_0^{\infty} DOS_{2D}(E) \cdot f(E) dE \,, \tag{1}$$

where $f(E)$ is the Fermi-Dirac distribution and $DOS_{2D}(E)$ is the 2D density of states corresponding to the lowest band. The Fermi energy $E_F = qV_C$, where V_C is the voltage across the quantum capacitance for the 2D channel and q is the elementary charge. Simplifying the charge density expression, we obtain $n_{2D} = N_{2D} \ln(1 + \alpha)$ where $\alpha = \exp[(qV_C - E_0)/(k_B T)]$, $E_0 = E_G/2$, and

$$N_{2D} = \frac{k_B T g_K m_{effK}}{\pi \hbar^2} + \frac{k_B T g_Q m_{effQ}}{\pi \hbar^2} \exp\left(-\frac{\Delta E_{KQ}}{k_B T}\right) \tag{2}$$

where, k_B is the Boltzmann constant, and T is the average device temperature. We use the semiconductor mid-gap as our energy reference ($E = 0$) such that the conduction band energy is E_0 and the valence band energy is $-E_0$. g_K and g_Q are the degeneracy of the K and Q conduction valleys, respectively, and m_{effK} and m_{effQ} are their respective DOS effective masses. For MoS_2 $g_K = 2$, $g_Q = 6$,[9] $m_{effK} = 0.48m_0$, and $m_{effQ} = 0.57m_0$.[10] ΔE_{KQ} is the energy separation between K and Q conduction valleys (~0.11 eV for monolayer MoS_2).[6]–[8] For the sake of simplicity, we take the band gap (E_G) to be the same as the photoluminescence (PL) gap, which is ~1.85 eV for MoS_2 and ~1.65 eV for WSe_2. However, we note that the true electronic band gap can be affected by the dielectric screening environment, by strain, and proximity to grain boundaries.[7], [11]

Along with the free charge carriers, impurities (N_{Dop}) and traps (N_{it}) also contribute to the total channel charge (Q_{ch}) as:

$$Q_{ch} = -q[N_{Dop} + N_{it} + n_{2D}]. \tag{3}$$

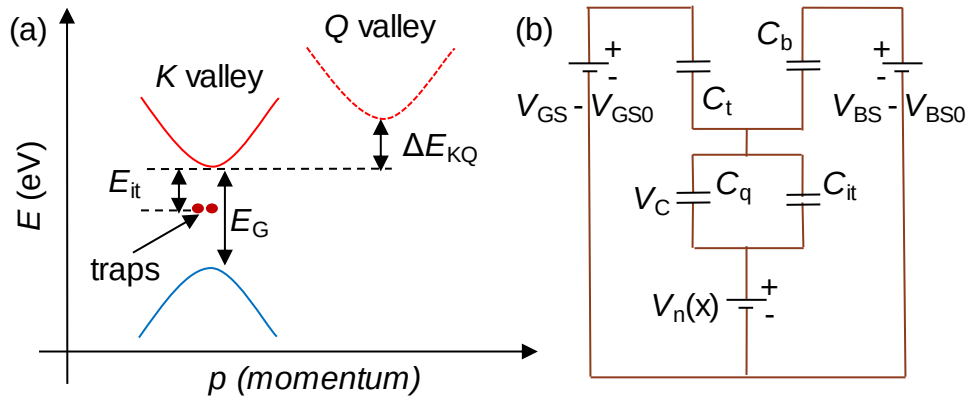

Figure 3: (a) Schematic of band structure of a 2D material with the K and the Q conduction band valleys. The energy separation between two valleys, ΔE_{KQ}, is of the order of few $k_B T$. (b) Schematic used to calculate the channel charge. V_{GS} and V_{BS} are the voltages of the top- and back-gate, respectively. V_{GS0} and V_{BS0} are respective flat band voltages. C_t and C_b are the top and bottom oxide capacitances, respectively. C_q is the quantum capacitance of the 2D monolayer channel and C_{it} is the capacitance due to traps at the oxide-channel interface(s).

As shown in Fig. 3a, we model the interface traps as acceptors, situated at an effective energy E_{it} below the conduction band, with an effective trap density D_{it}. To simplify the model, D_{it} is assumed here to be a delta function in energy, but this approach could be generalized. At a bias, the number of trapped carriers (N_{it}) is given by,

$$N_{it} = \int_{-E_0}^{E_0} D_{it} f(E) dE = \frac{D_{it}}{1+\exp(\frac{E_0 - E_{it} - qV_C}{k_B T})} \ . \quad (4)$$

The device electrostatics are guided by the distributed capacitive circuit model shown in Fig. 2(b).[4], [12] The top and the back oxide capacitance are C_t (= ε_{OX}/t_{OX}) and C_b (= $\varepsilon_{BOX}/t_{BOX}$) respectively. ε_{OX} and ε_{BOX} are the dielectric constants, and t_{OX} and t_{BOX} are the oxide thicknesses of the top and bottom oxide, respectively. C_q is the quantum capacitance and C_{it} is the capacitance due to traps at the oxide-semiconductor interface, taken as a combination from both interfaces of the ultra-thin 2D channel. The quantum capacitance C_q and the trap capacitance C_{it} are given by

$$C_q = q\frac{dn_{2D}}{dV_C} = \frac{q^2 N_{2D}\alpha}{(1+\alpha)k_B T} \quad (5a)$$

$$C_{it} = -q\frac{dN_{it}}{dV_C} = \frac{D_{it} q^2 \alpha\beta}{k_B T(\alpha+\beta)} \quad (5b)$$

where $\beta = \exp[-E_{it}/(k_B T)]$.

V_{GS}-V_{GS0} and V_{BS}-V_{BS0} are internal voltages from the top- and the back-gate respectively. V_{GS0} and V_{BS0} are flatband voltages of the top- and back-gate, treated as fit parameters to the experimental data. (For example, if the top-gate metal workfunction is increased, V_{GS0} will be higher, etc.) The total charge in the 2D channel (Q_{ch}, eq. 3), and the quantum potentials at the source (V_{Cs}) and the drain (V_{Cd}) are calculated iteratively as discussed in the Appendix A of Ref. [1], including doping and trapped charges. We neglect the channel depletion capacitance because the channel thickness is less than 1 nm. We note that the effect of the fringing field from the drain through the BOX can also be incorporated in our model by including an additional capacitance between the drain node and the channel in the circuit shown in Fig. 3(b).[13] In thicker multi-layer channels, the depletion capacitance should be accounted for, in a similar manner as it is done for silicon-on-insulator (SOI) transistors.[14]

We solve for semi-classical drift transport to obtain an expression for the drain current (I_D = -I_S) for all transistor operating regions. The semi-classical approach is appropriate even for 2D FETs near 10 nm channel length, as the present-day experimental mean free path in monolayer 2D semiconductors like MoS_2 is ~2 to 3 nm (see Fig. S10 in Supplement of Ref. 3). Similarly, our approach should hold for channel widths greater than 10-20 nm, for which edge scattering effects can be safely ignored. (And all experimental data for 2D semiconductors is typically taken on micron-width devices, to obtain larger current drives.) Thus:

$$I_D = \frac{\mu W}{L_G}\left[N_{2D}k_BT\alpha + q^2\ln^2(1+\alpha) - \frac{N_{2D}q^2D_{it}\beta}{(C_t+C_b)(\beta-1)}\left(\frac{(1+\alpha)\ln(1+\alpha)}{\alpha+\beta} - \ln(\alpha+\beta)\right)\right]_{V_{Cd}}^{V_{Cs}} . \quad (6)$$

Here μ is the carrier mobility, C_t and C_b are the top and the bottom oxide capacitances per unit area, and other variables are defined earlier. We recall that α is a function of V_C, and thus I_D is calculated as the difference of eq. 6 evaluated at V_{Cs} and V_{Cd}. (The complete derivation is given in Appendix A. of Ref. [1]) Gate and diffusion currents are not included in the present version of the S2DS model, thus leakage power will be underestimated. Nevertheless, this could be a reduced component in TMD FETs, which have larger band gaps than semiconductors like Si and Ge.

When fitting to some (but not all) experimental data, we need to introduce a finite output resistance modeled by a fit parameter λ as $I_{D,eff} = I_D(1 + \lambda V_{DS})$. However, sometimes λ is not needed, especially when fitting the model against long channel back-gated MoS_2 FETs.[15] For fitting the model with experimental data on top-gate transistors, we used a finite value $0 < \lambda < 0.1$.[16], [17] We note that the current saturation region is also influenced by device self-heating, which is taken into account self-consistently, as we will discuss below.

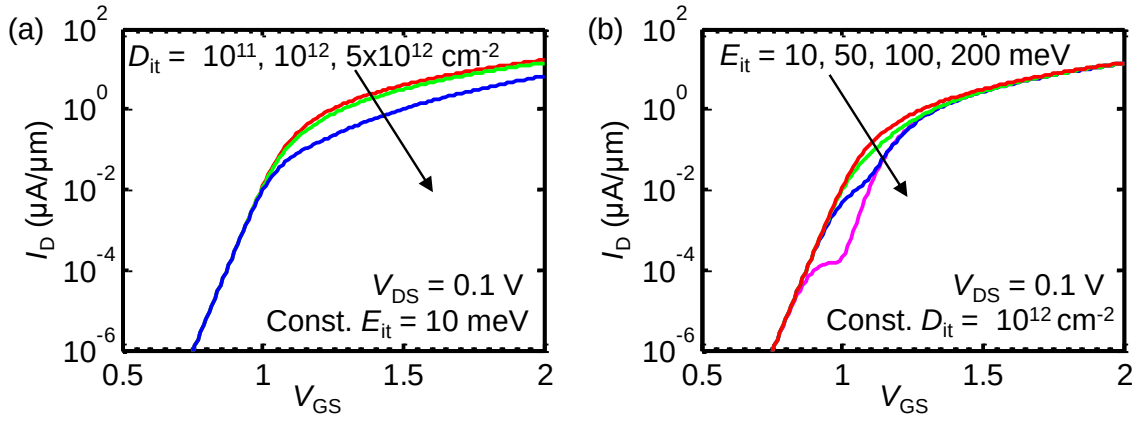

Figure 4: Simulated drain current vs. top-gate voltage ($I_D - V_{GS}$) curves for a 1L top-gate MoS_2 n-FET ($V_{BS} = 0$) with L_G = 1.0 µm, effective oxide thickness (EOT) = 2 nm, R_{ext} = 1 kΩ·µm and μ_0 = 80 cm^{2}V^{-1}s^{-1} with (a) varying trap density (D_{it}); here E_{it} = 10 meV and (b) varying trap depths (E_{it}); here $D_{it} = 10^{12}$ cm^{-2}. For larger gate bias all traps are charged, and we see that the current is the same irrespective of E_{it}.

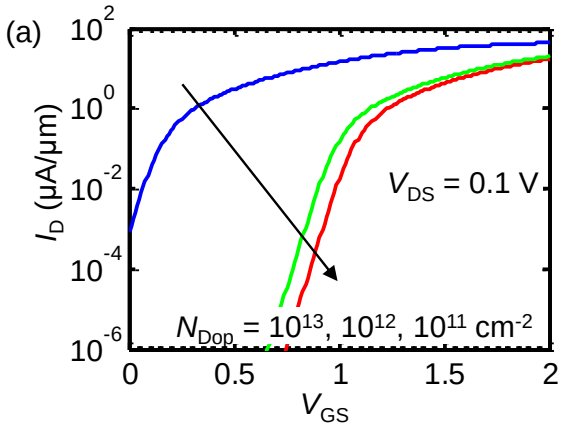

Figure 5: Simulated $I_D - V_{GS}$ of a 1L single-gate MoS_2 n-FET with the same characteristics as in Fig. 3, but with varying doping density and $D_{it} = 0$. Channel doping changes the flatband (and consequently the threshold) voltage of the device.

With these considerations, Fig. 4 displays the I_D vs. V_{GS} curve for a few trap densities and trap energies. For large trap densities, a part of the gate voltage is used to charge the traps. As a result, less voltage is available to induce mobile charges in the channel, leading to smaller drain currents [Fig. 4(a)]. In Fig. 4(b), the V_{GS} at the kink in the I_D vs. V_{GS} curve is the voltage at which the Fermi energy is closest to the trap energy, and charges a significant amount of traps. For large $V_{GS,}$ all traps are charged, and the drain current remains constant for different trap energies. Similarly, Fig. 5 shows the impact of doping the channel material for an n-type 2D FET. Large doping shifts the flatband voltage in the negative direction, increasing the current.

Non-ideal effects

Besides the current-voltage relations derived above, we have listed other effects which have been included in the model.

Extrinsic resistance:

Generally speaking, the total extrinsic resistance $R_{ext} = R_U + R_C$ of the intrinsic device includes resistance due to the underlap region (R_U) and the contact resistance between metal and semiconductor (R_C). The underlap R_U can be reduced by adjusting the back-gate voltage (i.e. "electrostatic doping" using a back-gate plane under the entire device), or by chemical doping, the latter being preferred in realistic devices. The impact of both adjustments is shown in Fig. 6(a) and Fig. 6(b) for different underlap lengths. In addition, the underlap resistance can also be reduced by increasing the mobility of the 2D channel material.

The contact resistance (R_C) for 2D devices can display non-linear behavior with respect to drain and gate voltages due to the Schottky barrier at the metal-semiconductor interface.[3] For simplicity, here we assume that R_C is optimized in the fabrication and is Ohmic, which is a good approximation at higher lateral field and high V_{DS}. Nonetheless, following work on organic TFTs,[18], [19] it is possible to model each contact with a pair of anti-parallel Schottky diodes.

Thermal heating:

Considering that 2D devices can carry high current densities,[15], [20], [21] unlike their organic counterparts in flexible and transparent electronics,[22] such transistors can generate significant heat. We can model the FET self-heating by including a thermal resistance (R_{TH}) such that the average device temperature rise is $\Delta T = T - T_0 = P R_{TH}$, where $P = I_D(V_{DS} - 2I_D R_C)$ is the power input of the device without the contacts. As illustrated in the inset of Fig. 5(a), the total thermal resistance has three components: the thermal boundary resistance (TBR) between the channel and the bottom oxide ($R_B = R_{TBR}/A$), the spreading resistance of the bottom oxide (R_{BOX}), and the spreading thermal resistance into the substrate (R_{Si}).[23], [24] The thermal resistance per unit length is given as

$$g^{-1} = \frac{R_{Cox}}{W} + \left\{ \frac{\pi k_{ox}}{\ln\left[6\left(\frac{t_{ox}}{W}+1\right)\right]} + \frac{k_{ox}}{t_{ox}} W \right\}^{-1} + \frac{1}{2k_{sub}} \left(\frac{L_G + 2L_U}{W_{eff}} \right) \qquad (9)$$

Here k_{BOX} and t_{BOX} are the thermal conductivity and thickness of the bottom oxide (BOX), respectively, and k_{sub} is the thermal conductivity of the substrate. The TBR per unit area is $R_{TBR} \approx 10^{-7}\ m^2KW^{-1}$ for monolayer MoS_2 on SiO_2[25] and the "thermal area" of the device is $A \approx W(L_G + 2L_U)$. Due to heat spreading effects in the SiO_2, the effective thermal width at the SiO_2/Si interface can be approximated as $W_{eff} \approx W + 2t_{BOX}$.

T he thermal expression in eq. 9 strictly only applies to "longer" channel devices, at least three times longer than the lateral thermal healing length (L_H) along the channel. For 1L MoS_2 on 90 nm SiO_2 on Si substrate, $L_H = [k_{2D}t_{2D}(W/g + R_{TBR})]^{1/2} \approx 100$ nm, if we take $k_{2D} \approx 80\ Wm^{-1}K^{-1}$ as the in-plane thermal conductivity of MoS_2 at room temperature. (k_{2D} could become a function of length in shorter devices.[26]) For "longer" devices (with $L_G + 2L_U > 3L_H$), the thermal resistance is given simply by $R_{th} \approx 1/[g(L_G + 2L_U)]$. For "shorter" channel length devices ($L_G + 2L_U < 3L_H$), heat flow into the metal contacts becomes non-negligible and can be taken into account as described in Ref. [24]. We note that heat flow into a top metal gate can, in general, be neglected, partly due to TBR at the two top oxide interfaces, but mainly due to the presence of the larger heat sink (i.e. Si substrate) at the back-side.[27]

To quantify the impact of device self-heating, we simulate a typical 1L MoS_2 transistor ($L_G = 1$ μm) in Fig. 5(b) under four circumstances: without self-heating (solid line, top curve), with self-heating on 90 nm SiO_2 / Si substrate (dashed), with self-heating on 300 nm SiO_2 / Si substrate (dotted), and finally on a poor thermal substrate where the Si was replaced by a plastic like polyethylene naphthalate (PEN) or acrylic (dash-dotted). We observe reduction in saturation current of approximately 20, 26, and 70%, respectively from the "ideal" scenario without any self-heating. Thus, self-heating becomes crucial for devices on substrates with poor thermal conductivity, especially when the FET channel is a high-quality 2D material which has large current-carrying capability.

Note that S2DS does not yet consider the transient thermal behaviour. This will probably be added in the future versions.

Mobility

The electron mobility in 2D materials depends on the vertical and the lateral electric field, as well as on the temperature. The dependence on *vertical* (gate) field comes in through the dependence on carrier density. Higher carrier density can partially screen scattering with ionized impurities and remote polar phonons,[28] and higher carrier density also raises the Fermi level, which changes the effective density of states for scattering. Classical "sixth-power law of thickness" surface roughness scattering present in ultra-thin (<3 nm) bulk semiconductors like Si[29] should not, in principle, affect 2D semiconductors without dangling bonds.[28] However, the vertical field could affect scattering with microscopic roughness of the gate dielectric, including the remote phonons mentioned above. The mobility dependence on *lateral* field mostly comprises high-field effects, i.e. drift velocity saturation. The temperature dependence of mobility comes in through scattering with intrinsic phonons (of the 2D material) and remote dielectric phonons.

Keeping the above considerations in mind, we fit the mobility behavior (at low lateral field) with the following semi-empirical relationship:

$$\mu_{eff} = \frac{\mu_0}{\left(1+\frac{F_V}{F_C}\right)^{\eta}\left(\frac{T}{T_0}\right)^{\gamma}}, \tag{7}$$

where μ_0 is the effective mobility at zero field and room temperature (T_0), T is the average device temperature, F_V is the vertical electric field, γ is a positive constant that depends on dominant phonons, and fitting parameters η and F_C depend on the material and the quality of the interface. Figure 4(b) compares this model with experimental data for 1L WSe_2 (Ref. [17]) and the fit provides η = 6.8 and F_C = 305 V/μm. Previous studies on 1L MoS_2 have observed η = 1.45 and F_C = 90 V/μm.[9] The value of γ is also obtained by fitting the model to experimental data, yielding γ (bulk) = 2.6 (Ref. [30]) and γ (1L) = 1 to 1.6 for electron mobility in MoS_2.[15], [31]

At high lateral field, the carrier drift velocity begins to saturate and the effective mobility decreases. We include this effect using a semi-empirical relation

$$\mu = \frac{\mu_{eff}}{\left[1+\left(\frac{\mu_{eff}F}{v_{sat}}\right)^{\xi}\right]^{1/\xi}} \tag{8}$$

where ξ is a fitting parameter with typical value around 2 to 4, F is the lateral electric field and v_{sat} is the saturation velocity. Note it is this μ which is then used when calculating the current in eq. 6. The temperature dependence of the saturation velocity is incorporated similarly to models for graphene and Si,[32], [33] as $v_{sat} = v_0/(1 + N_{OP})$ where the OP (optical phonon) occupation is $N_{OP} = 1/[\exp(\hbar\omega_{OP}/(k_B T)) - 1]$. Here $\hbar\omega_{OP}$ is the OP energy and v_0 can be interpreted as the saturation velocity extrapolated to zero Kelvin. For MoS_2 the best fit against experimental high-field data (on monolayer MoS_2 grown by chemical vapor deposition on SiO_2) is obtained with $\hbar\omega_{OP} \approx 30$ to 40 meV and $v_0 \approx 2$ to 3×10^6 cm/s.[34] However, when modeling *I-V* curves of different devices in the literature, we must treat v_0 and $\hbar\omega_{OP}$ as fitting parameters.

Parasitic capacitance modelling

We now discuss the key parasitic capacitances that contribute to C_{GS} (gate to source) and C_{GD} (gate to drain). The total parasitic capacitance between the gate and the channel nodes (source and drain) is due to internal fields through the channel (C_{if}), outer fringing fields through the surrounding region (C_{of}) and normal fringing fields between the gate, and the source or the drain (C_{nf}). We display these fields in the schematic shown in inset of Fig. 5(a). The S2DS model does not include the capacitance between the gate and metal plugs at the drain or the source, but such capacitance can easily be included following Ref. [35].

The capacitance C_{nf} is obtained by mapping the perpendicular surfaces of the gate sidewall and the top surface of contact metal to equivalent parallel surfaces using conformal mapping.[36] We modify C_{nf} from Ref. [36] to only include the part of the gate sidewall ($t_G + t_{OX} - t_C$) which is higher than the contact metal as shown in the Fig. 5(a) inset. We assume that the contact length (L_C) is larger than the underlap length (L_U). C_{of} includes the fringing fields from the horizontal edges of the gate metal to the horizontal edges of the contact metal.[36] In addition, C_{of} includes the parallel capacitance between vertical sidewalls of the gate and the source or drain, approximated with an average distance $(L_U^2 + t_{OX}^2)^{1/2}$ between sidewalls. By solving for the specific geometry in Fig. 5(a), we obtain the analytical form of the total fringing capacitance as:

$$C_{nf} = \frac{2W\varepsilon_{sp}}{\pi}\ln\left[\frac{1.3(t_G + t_{OX} - t_C) + \sqrt{L_U^2 + 1.3^2(t_G + t_{OX} - t_C)^2}}{L_U}\right] \quad (10a)$$

$$C_{of} = \frac{0.2W\varepsilon_{sp}}{\pi}\ln\left[\frac{\pi W}{\sqrt{L_U^2 + t_{OX}^2}}\right]\exp\left(-\left|\frac{L_U - t_{OX}}{L_U + t_{OX}}\right|\right) + \frac{W(t_G + t_C)\varepsilon_{sp}}{2\sqrt{L_U^2 + t_{OX}^2}} \quad (10b)$$

where ε_{sp} is the dielectric constant of the surrounding spacer region, and the other quantities are defined in Fig. 1 and Fig. 5(a).

To obtain C_{if}, we separate the contribution of the channel charge between the source and the drain terminals by using the Ward-Dutton charge partition scheme.[37]

$$Q_D = W\int_0^{L_G}\frac{x}{L_G}Q_n(x)dx \quad (11a)$$

$$Q_S = W\int_0^{L_G}\left(1 - \frac{x}{L_G}\right)Q_n(x)dx \quad (11b)$$

Here the charge at the source (Q_S) and the drain (Q_D) are written in terms of the position dependent channel charge $Q_n(x) = -qn_{2D}(x)$. We note, as described in section II-A, that $n_{2D}(x) = N_{2D}\ln(1 + \alpha)$ where $\alpha = \exp[(qV_C(x) - E_0)/(k_BT)]$, and additional details are discussed in Appendix B of Ref. [1]. Using nodal charges, we calculate the internal field capacitances between node m and node j as $C_{if} = -\partial Q_m/\partial V_j$ ($m \neq j$) where m and j are the transistor nodes (gate, source or drain).

We also consider the impact of the fringing field from the top-gate on the carriers in the underlap region by including an effective fringing capacitor (C_{tf}) from the gate metal sidewall to the underlap region. The analytical expression for C_{tf} is obtained similar to eq. 10 using conformal mapping:[36]

$$C_{tf} = \frac{2W\varepsilon_{sp}}{\pi} \ln\left[\frac{\phi t_G + t_{OX} + \sqrt{\phi^2 t_G^2 + 2\phi t_G t_{OX}}}{t_{OX}}\right] \quad (12a)$$

$$\phi = \exp\left(\frac{L_U - \sqrt{t_G^2 + 2t_{OX}t_G}}{3.7L_U}\right) \quad (12b)$$

We note that when $t_{OX} \ll t_G \approx L_U$, then $\phi \approx 1$.

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