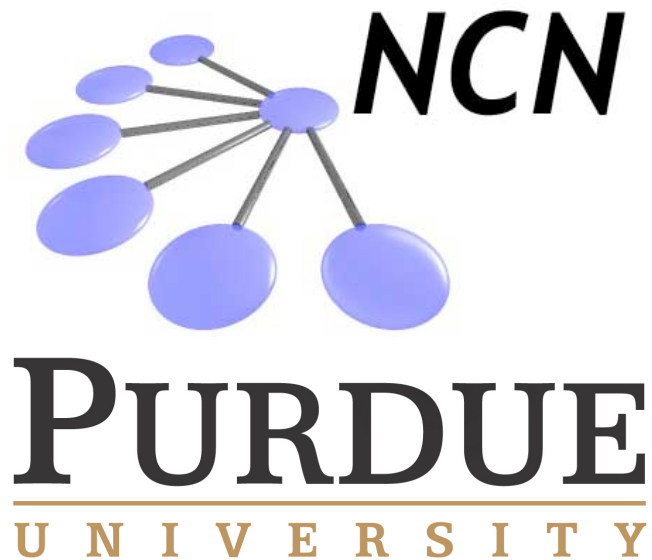


Network for Computational Nanotechnology (NCN)

UC Berkeley, Univ. of Illinois, Norfolk State, Northwestern, Purdue, UTEP

First-Time User Guide to MOSFET V1.2.2



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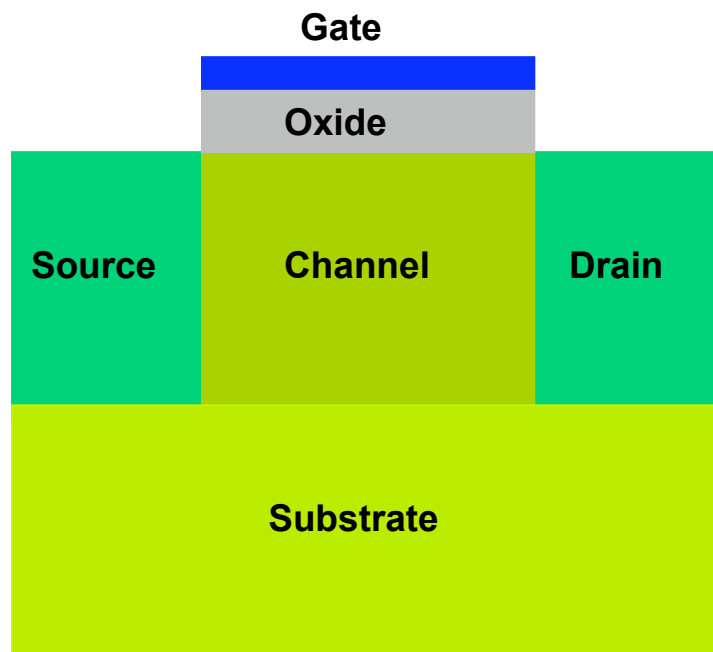
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What is a MOSFET?

metal–oxide–semiconductor field-effect transistor:

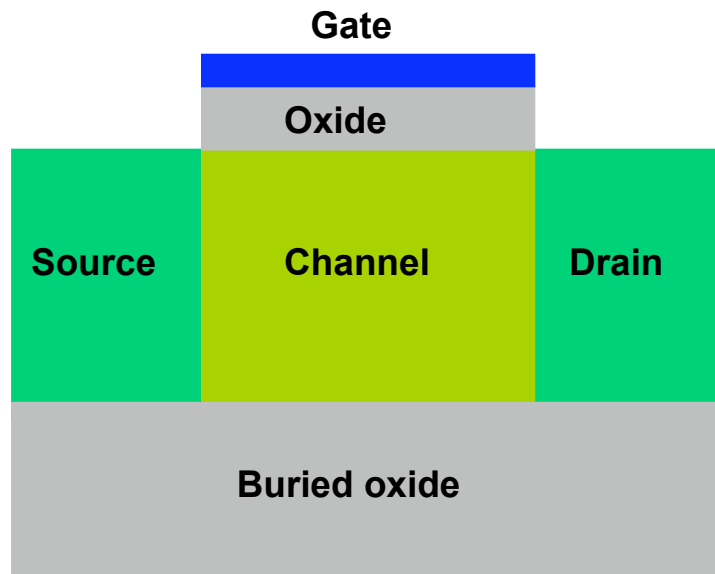
(**MOSFET, MOS-FET, or MOS FET**) is a device used to amplify or switch electronic signals.



- **Gate:** Polysilicon or Metal (eV)
- **Oxide:** SiO_2 used as the dielectric (nm)
- **Channel:** n-type doped semiconductor for PMOS and p-type doped for NMOS
- **Source/Drain:** Heavily doped regions in contact with channel
- **Substrate:** Base semiconductor material

What is a SOI MOSFET?

(**Silicon on Insulator**) **metal–oxide–semiconductor field-effect transistor**
(**SOI**) **MOSFET**: semiconductor device formed above an insulator



Advantages

- Better gate control* over thinner channel
- Reduces short channel effects*

Disadvantages

- Increases parasitic resistance*
- Quantization effects come in leading to increasing (threshold voltage) V_t

*Refer [1] <https://nanohub.org/resources/5085>
for detailed description of working of a
MOSFET.

What Can Be Simulated by the MOSFET Tool?

Structural Properties | Model | Voltage Sweep

Device Type: SOI n-type

Doping Profile: MOSFET n-type, MOSFET p-type, SOI n-type, SOI p-type

Source/Drain: SOI n-type, SOI p-type

Source/Drain Nodes: 15

Channel Length: 50nm

Channel Nodes: 20

Oxide Thickness: 2nm

Oxide Nodes: 5

Junction Depth: 15nm

Junction Nodes: 20

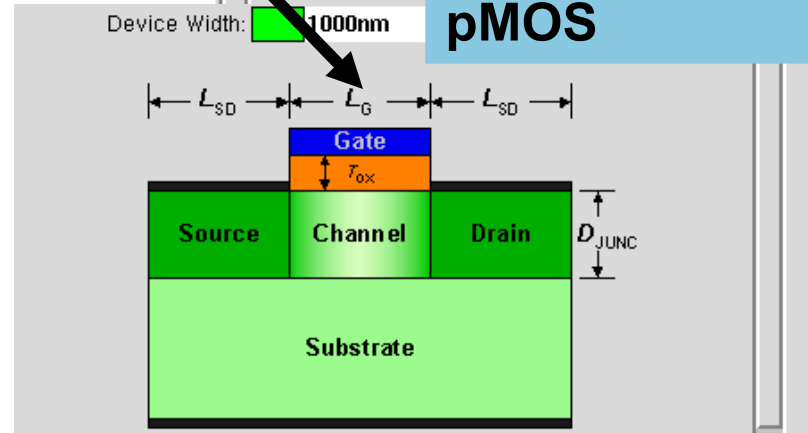
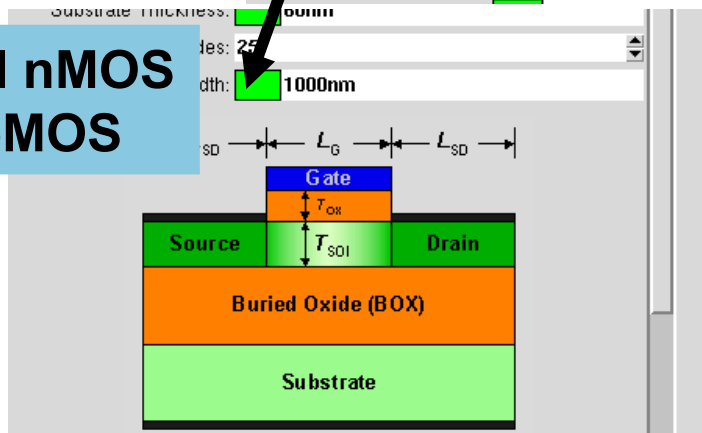
Buried Oxide Thickness: 100nm

Buried Oxide Nodes: 20

MOSFET simulation with different geometry types

Bulk nMOS & pMOS

SOI nMOS & pMOS



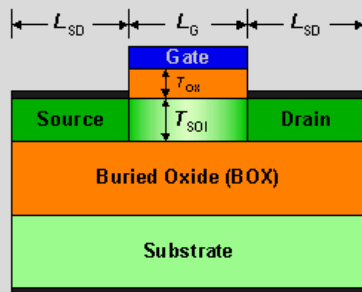
What Can Be Simulated by the MOSFET Tool?

Device Type: SOI n-type
Doping Profile: Uniform Doping Density

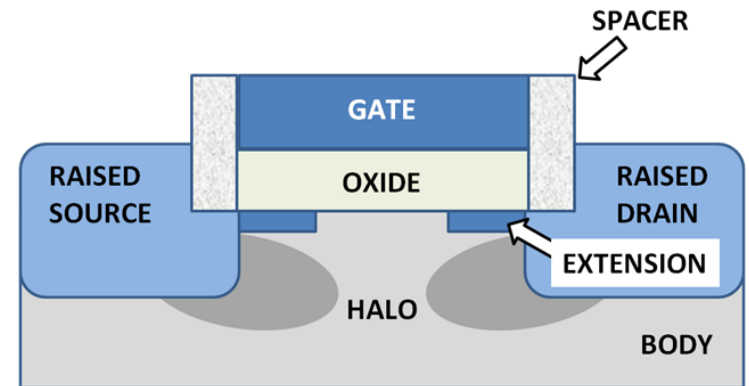
Design different MOSFET structures

Source/Drain Length: 50nm
Source/Drain Nodes: 15
Channel Length: 50nm
Channel Nodes: 20
Oxide Thickness: 2nm
Oxide Nodes: 5
Junction Depth: 15nm
Junction Nodes: 20
Buried Oxide Thickness: 100nm
Buried Oxide Nodes: 20
Substrate Thickness: 68nm
Substrate Nodes: 25
Device Width: 1000nm

More nodes: higher accuracy but more compute time



Source/Drain Doping Concentration: $2e+20/cm^3$
Channel Doping Concentration: $1e+18/cm^3$
Substrate Doping Concentration: $5e+16/cm^3$



Modern MOSFET structure.[2]

3 different doping profiles to simulate real devices:

- Uniform
- Gaussian S/D
- Gaussian S/D + Halo

What Can Be Simulated by the MOSFET Tool?

Structural Properties | Model | Voltage S

Ambient Temperature:

Gate Electrode:

Gate Electrode Workfunction:

Silicon parameters

Silicon Bandgap at 300K:

Silicon Dielectric Constant:

Oxide Parameters

Oxide Barrier Height at 300K:

Oxide Dielectric Constant:

Oxide Fixed Charge Density (/cm³):

CONMOB: yes

FLDMOB: yes

GATMOB: yes

IMPACT Ionization: no

Bipolar Carriers: no

Set material parameters and model

- No poly depletion included in simulations
- Bandgap, dielectric constant, and barrier height can be tuned to simulate another materials

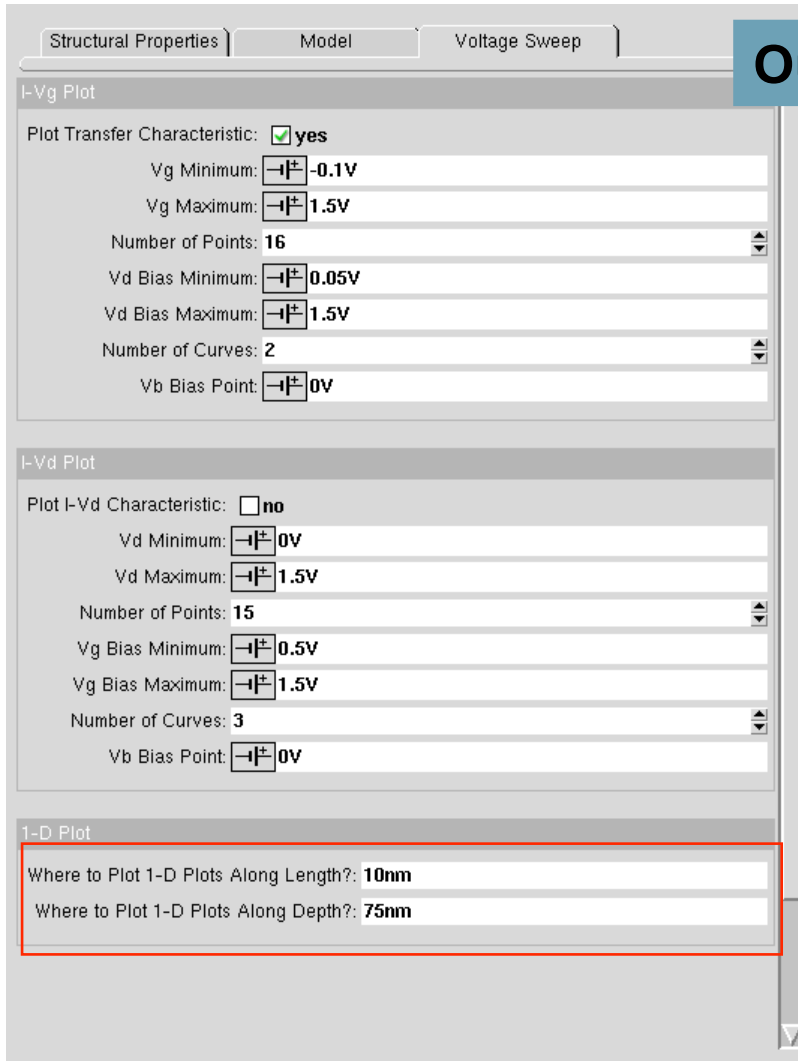
- **CONMOB:** Ionized Impurity scattering
- **FLDMOB:** Velocity Saturation model
- **GATMOB:** Gate-field mobility model

Refer [3] below to know more about the models.

[3]

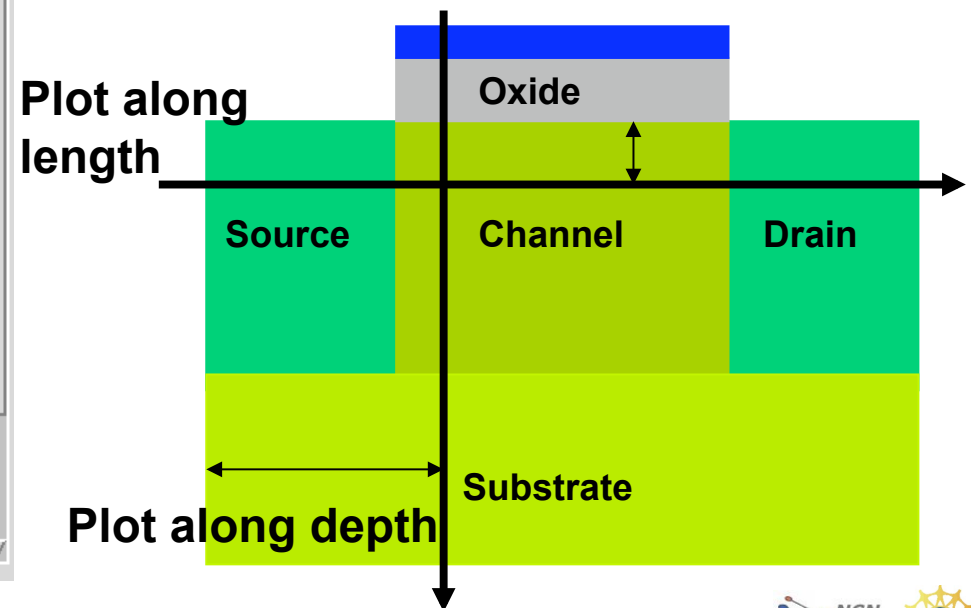
http://nanohub.org/resource_files/tools/padre/doc/padre-ref/mater.html

What Can Be Simulated by in the MOSFET Tool?



Output from MOSFET tool

- Both I_d - V_g and I_d - V_d curves can be simulated during the same run
- Keep number of bias points at 0.1 V spacing for better convergence



What Can Be Simulated by the MOSFET Tool?

Result: Doping

Id-Vg Characteristics
2D Plots

Doping

- Potential energy at Equilibrium
- Potential energy at Final Bias
- Electron density at Equilibrium
- Electron density at Final Bias
- Hole density at Equilibrium
- Hole density at Final Bias
- Electric field at Equilibrium
- Electric field at Final Bias

-----1-D Plots Along Channel Length (x)-----

- Doping (1D)
- Potential at Equilibrium (1D)
- Potential at Final Bias (1D)
- Electric Field at Equilibrium (1D)
- Electric Field at Final Bias (1D)
- Electron quasi-fermi level at Equilibrium (1D)
- Electron quasi-fermi level at Final Bias (1D)
- Electron density at Equilibrium (1D)
- Surface charge vs Vg
- Electron density at Final Bias (1D)

-----1-D Plots Along the Depth (y)-----

- Doping (1Dy)
- Potential at Equilibrium (1Dy)
- Potential at Final Bias (1Dy)
- Electric Field at Equilibrium (1Dy)
- Electric Field at Final Bias (1Dy)
- Electron quasi-fermi level at Equilibrium (1Dy)
- Electron quasi-fermi level at Final Bias (1Dy)
- Electron density at Equilibrium (1Dy)
- Electron density at Final Bias (1Dy)
- Output Log

Download

1 result Parameters...

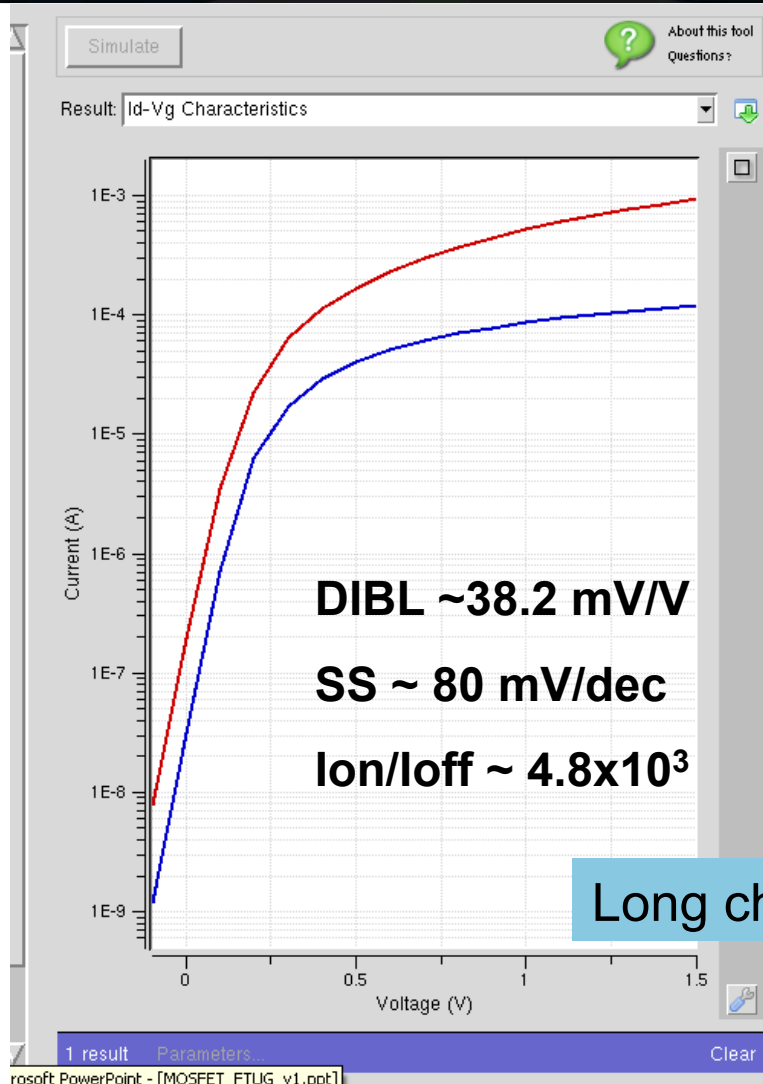
Output Characteristics:

- Id-Vg & Id-Vd

In 2D,1D(along x) and 1D(along y)

- Doping profile (/cm³)
- Potential profile (V)
- Electron density (/cm³)
- Hole density (/cm³)
- Electric field (V/cm)
- Quasi-Fermi level (eV)

What If You Just Hit Simulate?



Default setting simulates Id-Vg characteristics for N-type MOSFET:

Channel length, $L=100\text{nm}$

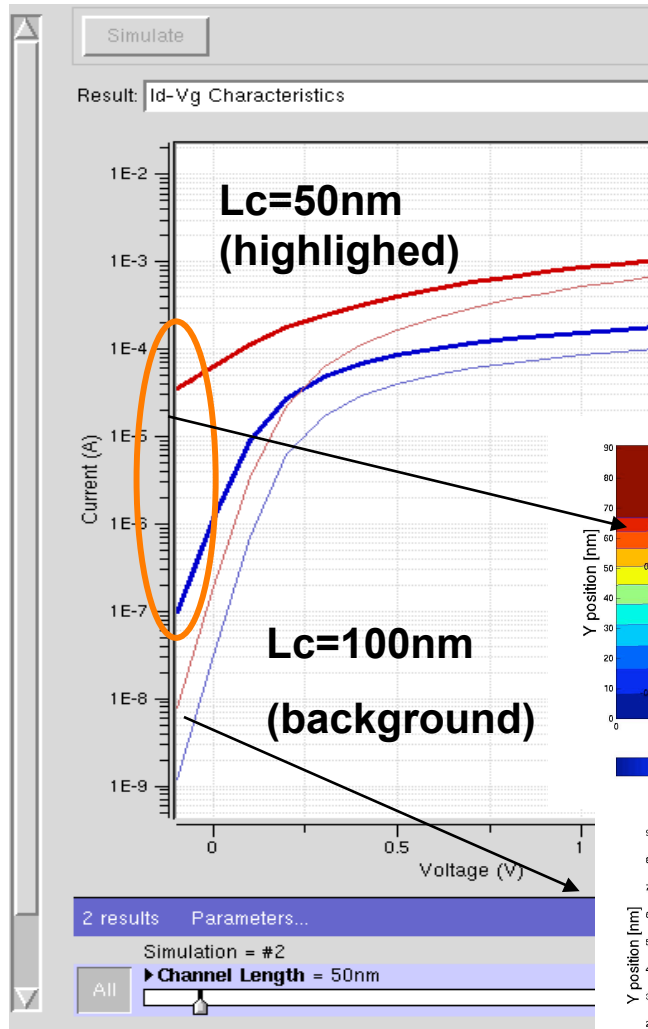
Oxide thickness, $T_{ox}=2\text{nm}$

Channel doping, $N_{ch}=1e18/\text{cm}^3$

Id-Vg simulated are at

$V_d=0.05\text{V}$ (low) & $V_d=1.5\text{V}$ (high)

Example: What if the Channel Length is Changed?



Id-Vg comparison between MOSFET with Lc=50nm & Lc=100nm

Severe short channel effects [3] at Lc=50nm. Vd=1.5V (red) & Vd=0.05 (blue)

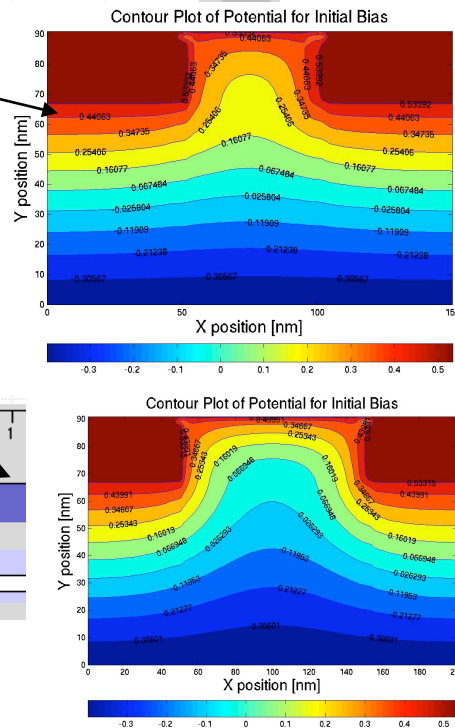
- High OFF state current*
- High DIBL*
- High Subthreshold slope*

*Please refer to reference [3] for more information about short channel effects in MOSFETS

DIBL: Drain Induced Barrier Lowering

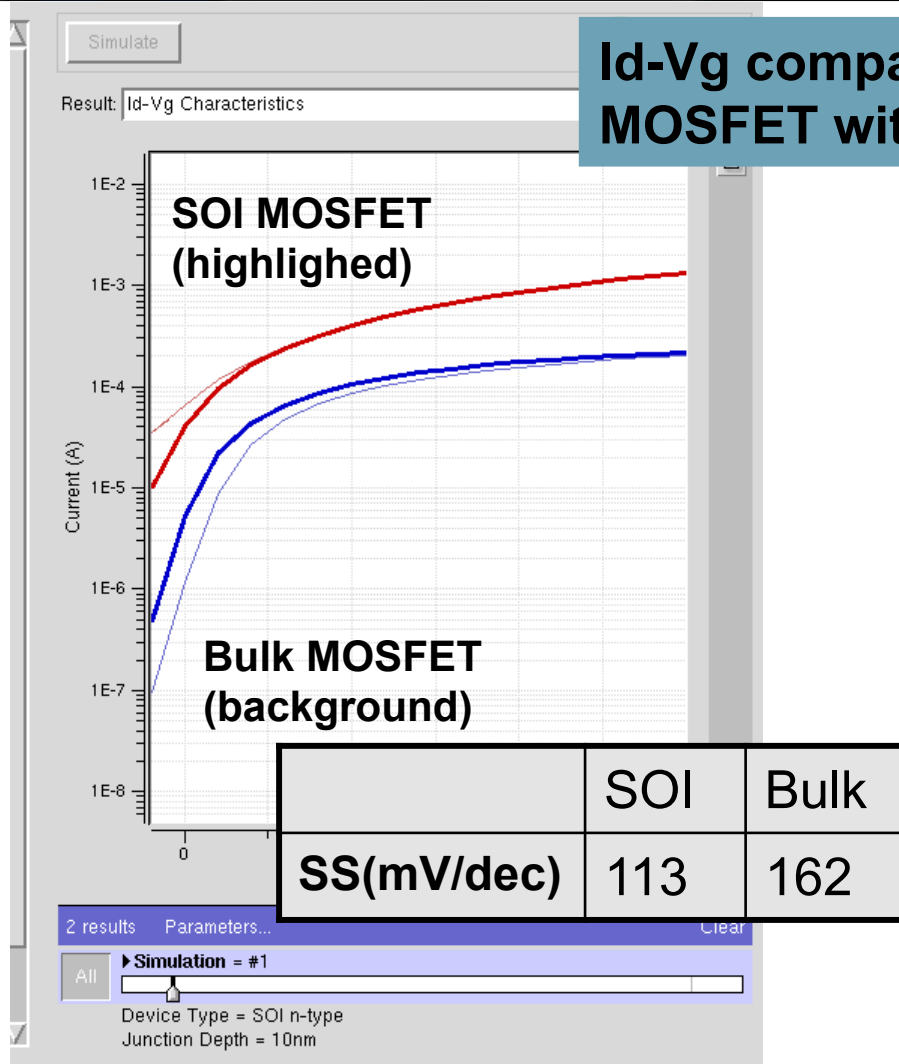
<https://nanohub.org/resources/5085>

Barrier lowered for Lc=50nm



Example: SOI versus Bulk MOSFET

Id-Vg comparison between bulk and SOI MOSFET with Lc=50nm



Improved short channel effects [3] for SOI-MOS (10 nm body thickness) over bulk-MOS at Lc=50nm.

Vd=1.5V(red) & Vd=0.05(blue)

- Lower Ioff
- Lower DIBL
- Lower subthreshold slope

Please refer [3] for more information about Short Channel Effects in MOSFETS

<https://nanohub.org/resources/5085>

Tool Limitations and General Comments

- No polydepletion effects are included in the simulations.
 - Quantum effects are not present in the simulations.
 - » This is important for SOI simulation with very thin (<5nm) body thickness
 - Few bias points during the large bias sweep (V_g or V_d sweep) might lead to non convergence.
 - Take note of the location of 1D output plots while running the simulation (i.e. output profile should lie in the desired region of interest).
-

Please use the following link to submit any issues/comment:

- <https://nanohub.org/resources/3/reviews?action=addreview#reviewform>

If you reference this work in a publication, please cite as follows:

- Matteo Mannino; Shaikh S. Ahmed; Gerhard Klimeck; Dragica Vasileska; Xufeng Wang; Himadri Pal (2006), "MOSFet," [DOI: 10254/nanohub-r452.7](https://doi.org/10.2554/nanohub-r452.7).

References

[1] MOSFET OPERATION DESCRIPTION:

<https://nanohub.org/resources/5085>

[2] MODERN MOSFET STRUCTURE (image)

http://en.wikipedia.org/wiki/File:MOSFET_junction_structure.png

[3] PADRE DEVICE SIMULATOR MANUAL:

http://nanohub.org/resource_files/tools/padre/doc/padre-ref/mater.html

[4] PADRE SIMULATOR: <https://nanohub.org/resources/941/>