Negative Bias Temperature Instability (NBTI) in p-MOSFETs: Characterization, Material/Process Dependence and Predictive Modeling (Part 1 of 3)

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Outline

Introduction, Basic NBTI signatures

Fast / Ultra-fast drain current degradation measurement

Estimation of pre-existing and generated defects

Part-I

Transistor process / material dependence

Role of Nitrogen – Study by Ultrafast measurement

Part-II

Predictive modeling

Conclusions / outlook

Part-III

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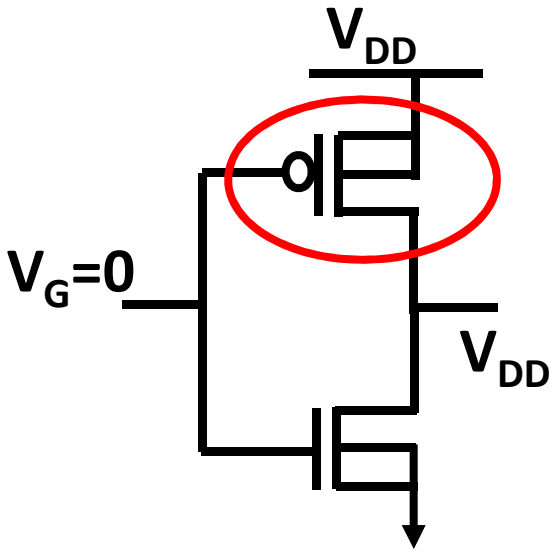
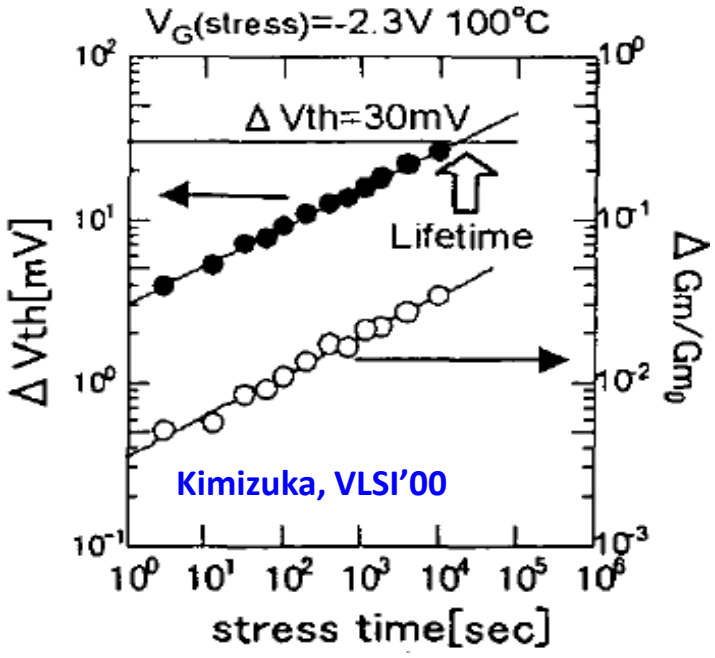
Negative Bias Temperature Instability (NBTI)

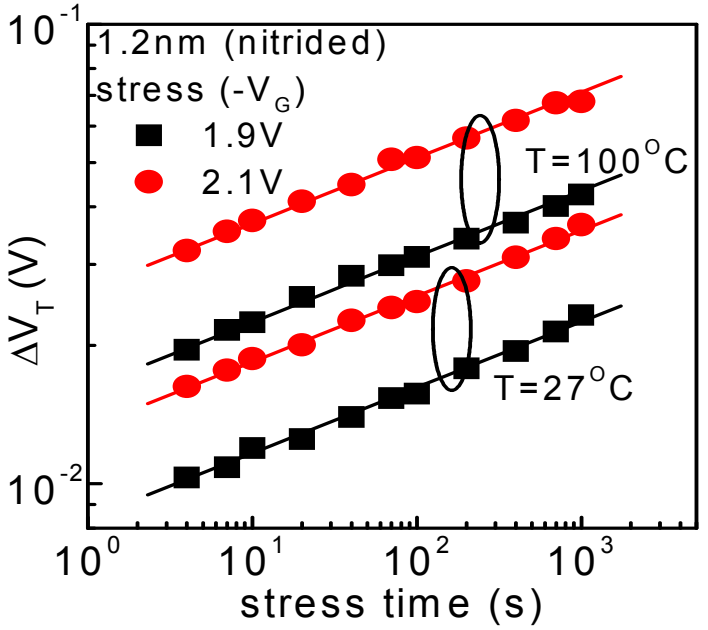


Issue: p-MOSFET in inversion

Parametric degradation (ΔV_T, Δg_m) in time, shows power law time dependence (~ $A*t^n$)

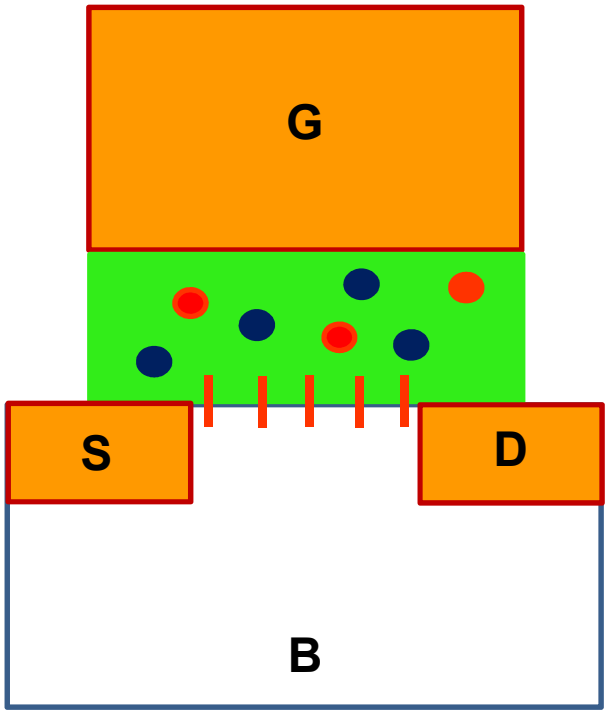
Degradation increases at higher T and higher (negative) stress bias





A Simple Physical Framework of NBTI

Parametric (V_T, g_m, I_{DLIN}) shift due to positive charges generated at the Si/SiO_2 interface and/or at SiO_2 bulk

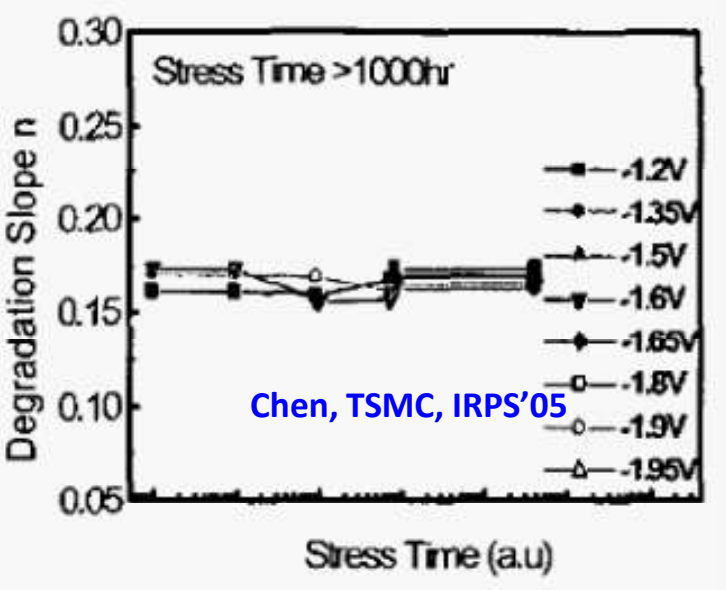


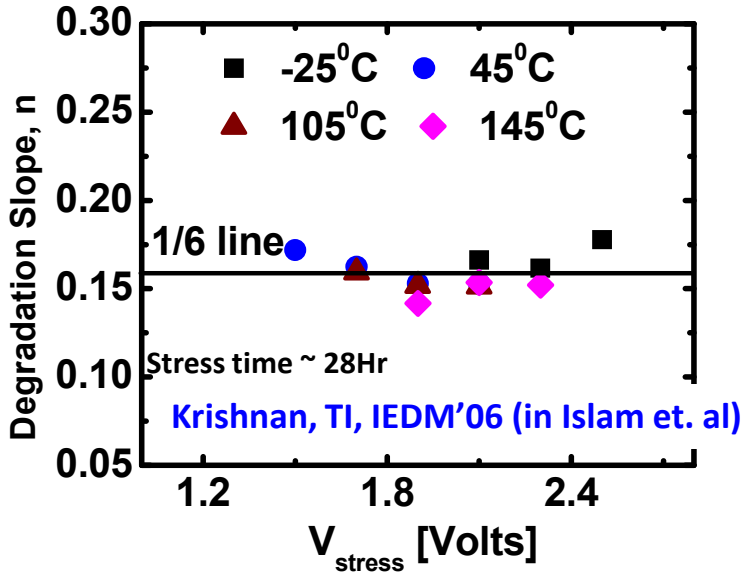
Generation of interface traps

Generation and subsequent charging of bulk oxide traps

Charging of pre-existing (process related) bulk oxide traps

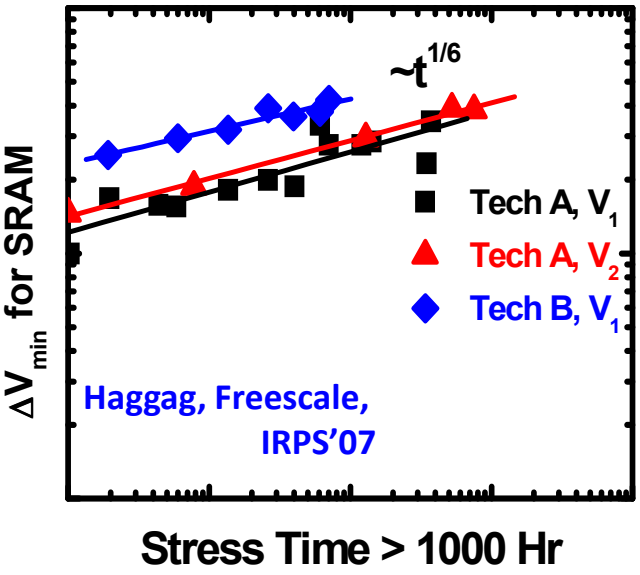
Very Long Time Degradation





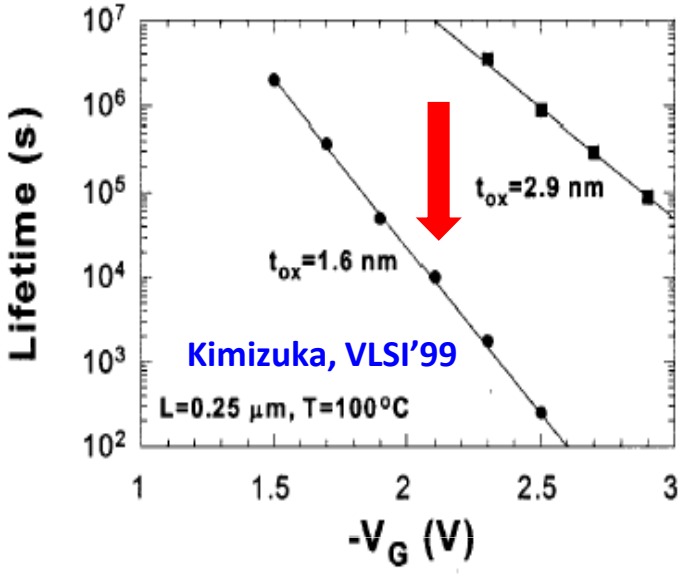
Universally observed long-time power-law time exponent of n = 1/6 in "production quality" devices

Similar observation in circuits

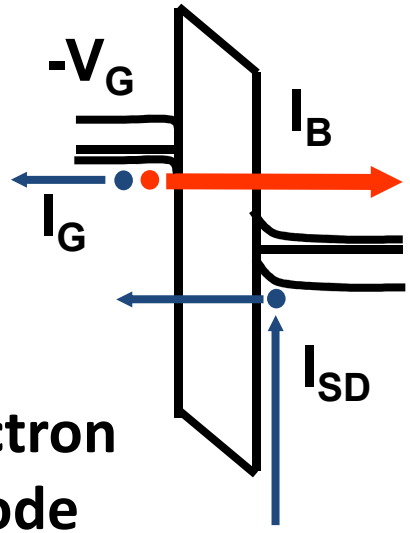


Important feature for prediction of degradation at end-of-life

Dependence on Stress V_G and Gate Leakage



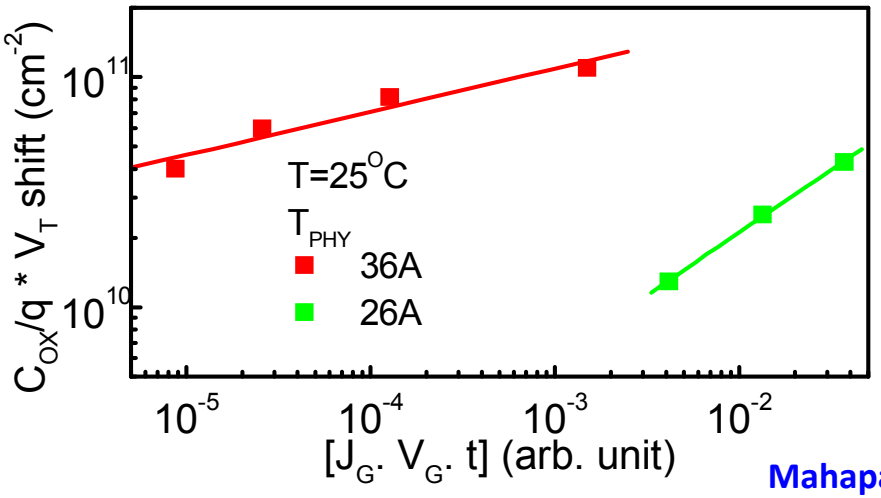
NBTI not governed by gate voltage – higher NBTI (lower lifetime) for thinner oxide

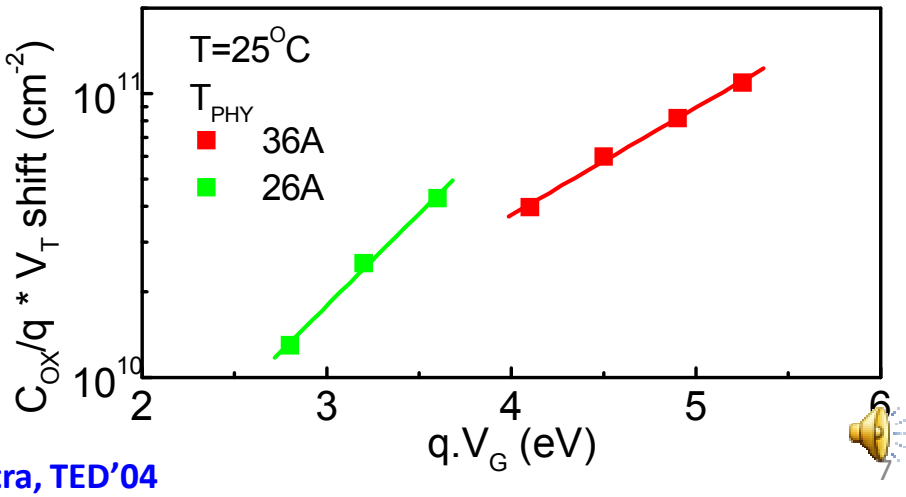


p-MOSFET inversion: Electron tunneling from gate to bulk, hole tunneling from bulk to gate

No correlation with electron energy dissipated in anode

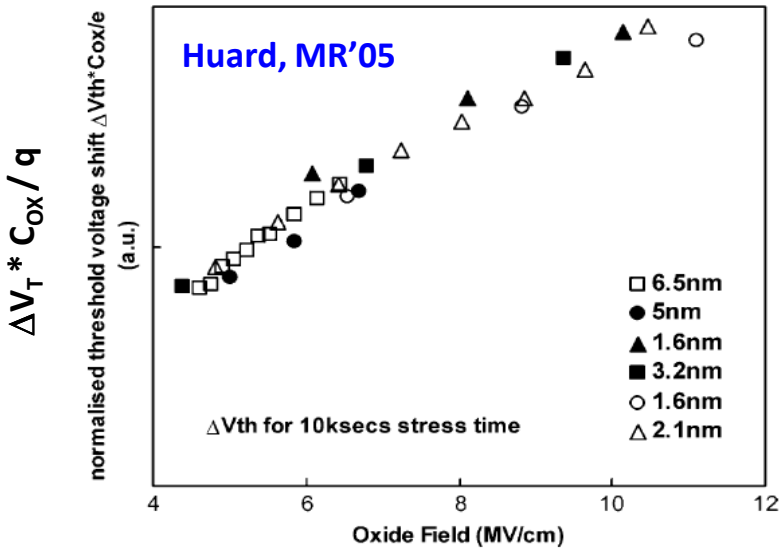
No correlation with electron energy even under ballistic limit

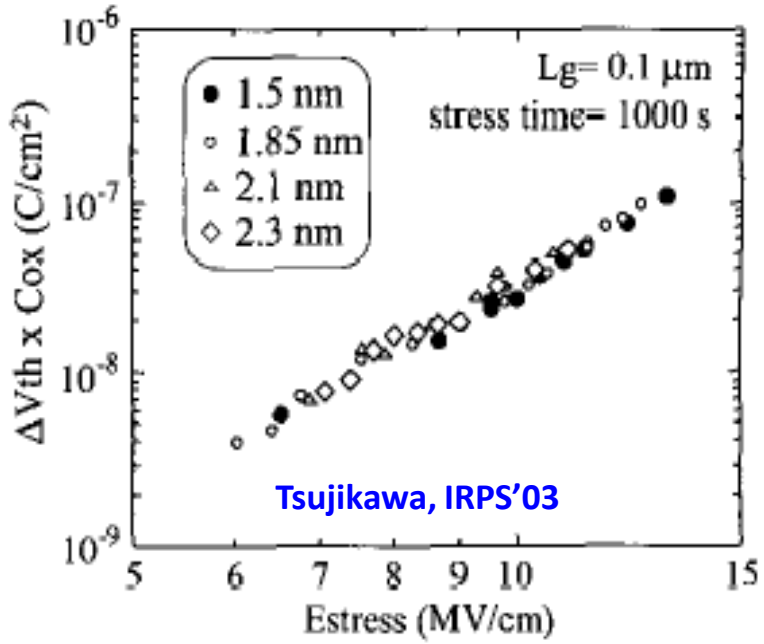




Mahapatra, TED'04

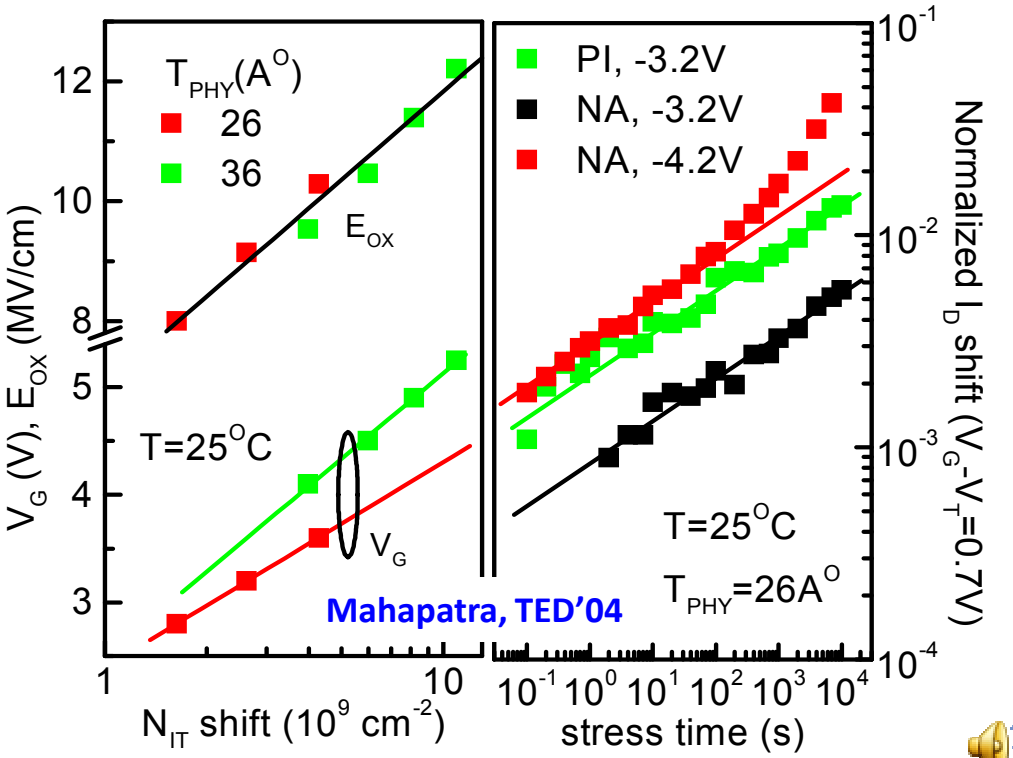
Dependence on Stress E_{OX}



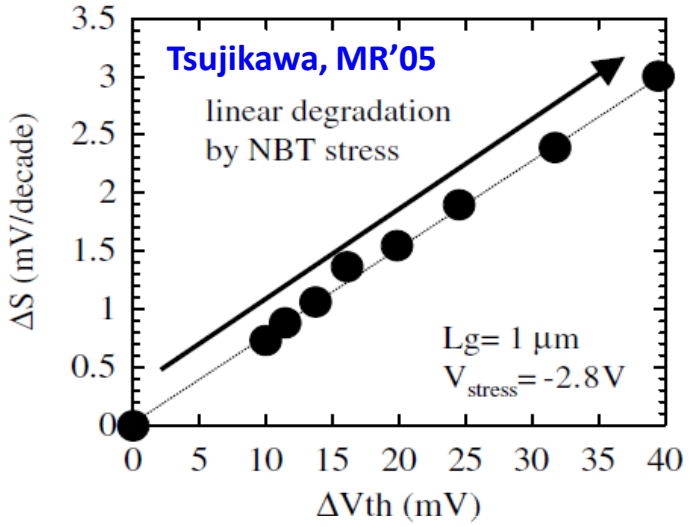


NBTI governed by oxide electric field

PMOS inversion shows similar NBTI as NMOS accumulation under similar oxide field (not same voltage)



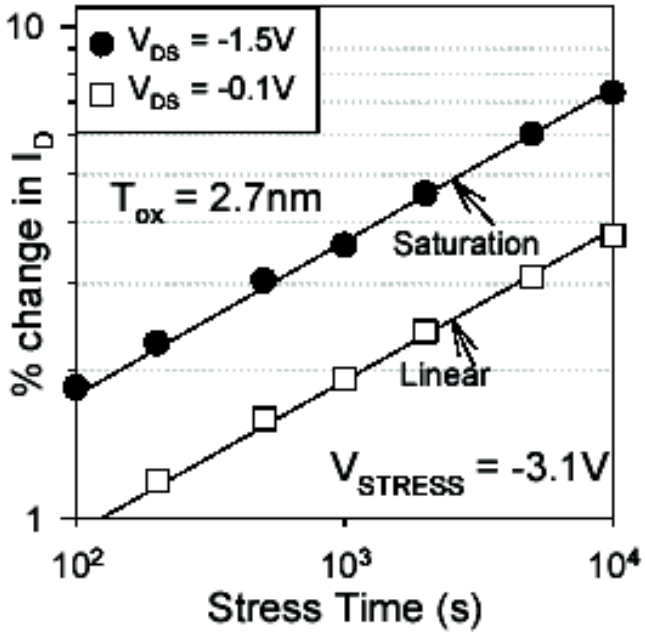
Parametric Degradation



Degradation in subthreshold slope (due to generation of interface traps, N_{IT})

For a given ΔV_T, $\Delta I_{DSAT} > \Delta I_{DLIN}$ (as $1 < \theta < 2$)

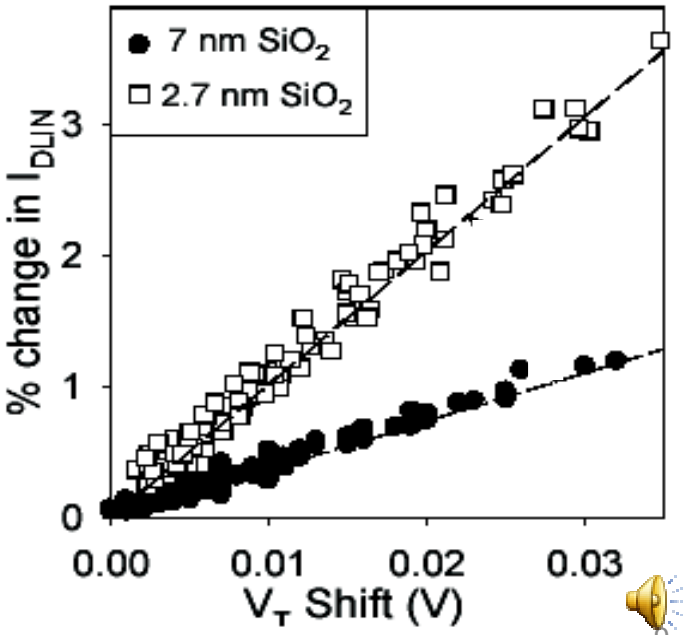
For a given ΔV_T, larger ΔI_{DLIN} for thinner oxide (lower overdrive)



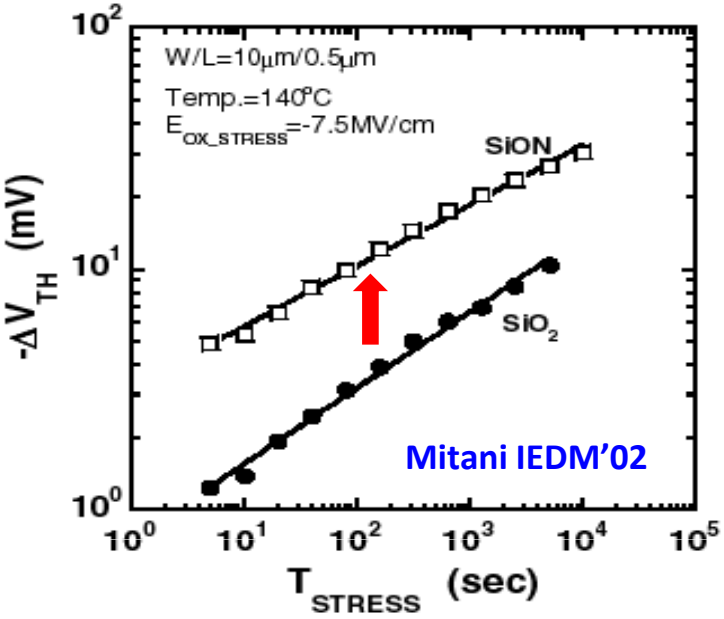
$$\frac{\Delta I_{DLIN}}{I_{DLIN}} \approx \frac{(-\Delta V_T)}{(V_G - V_T)}$$

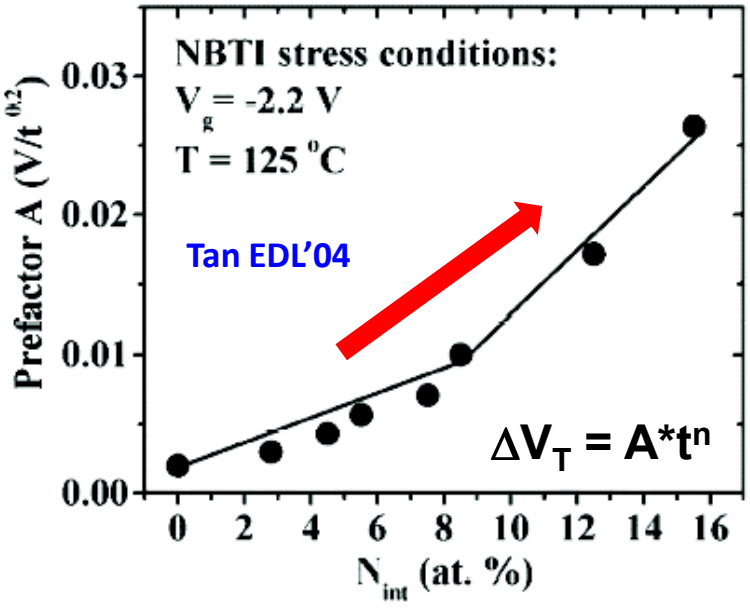
$$\frac{\Delta I_{DSAT}}{I_{DSAT}} \approx \theta \frac{(-\Delta V_T)}{(V_G - V_T)}$$

Krishnan, IEDM'03



Gate Insulator Material / Process Impact

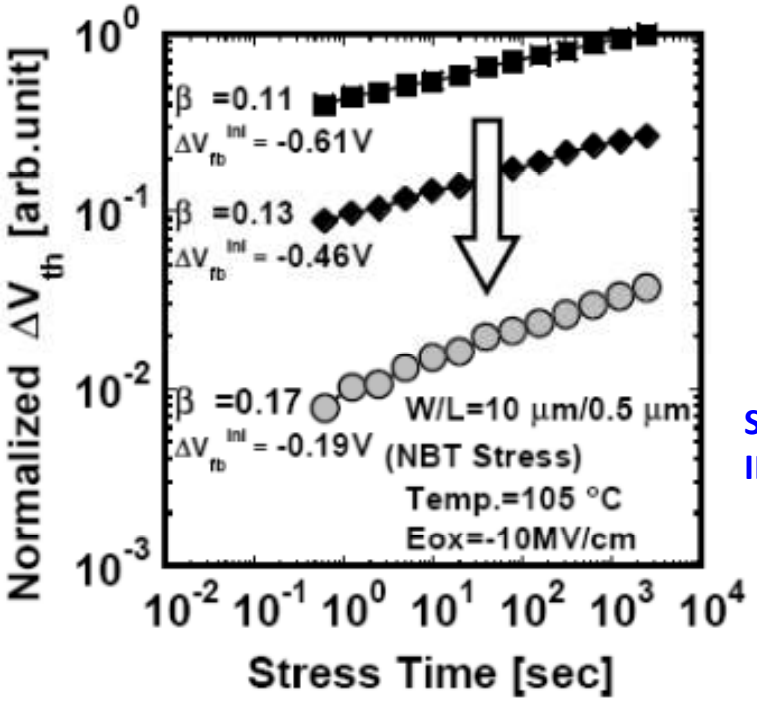




Larger NBTI for SiON compared to SiO_2 gate insulator

Increase in NBTI with higher N content in the gate insulator

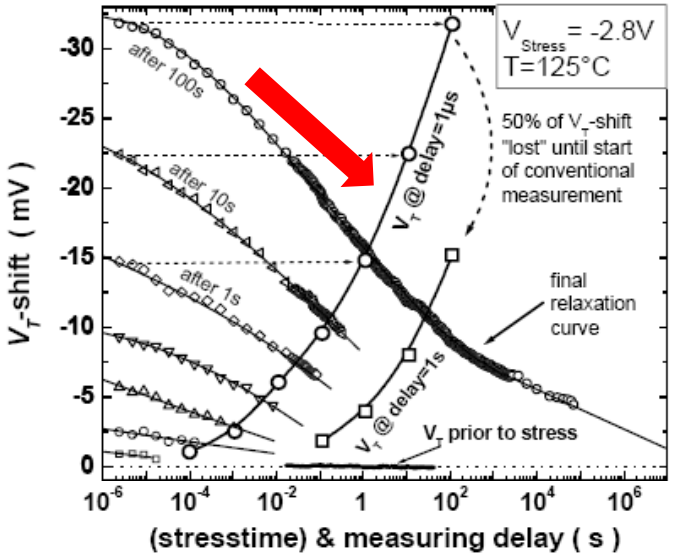
NBTI reduction by suitable "process optimization"

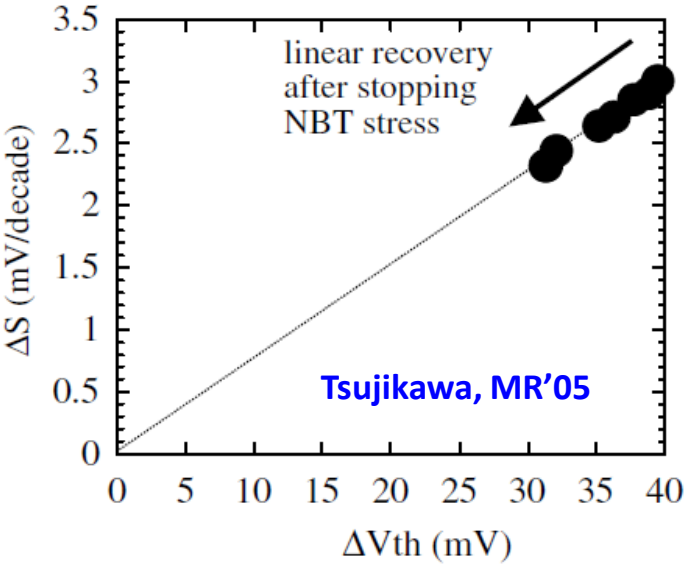


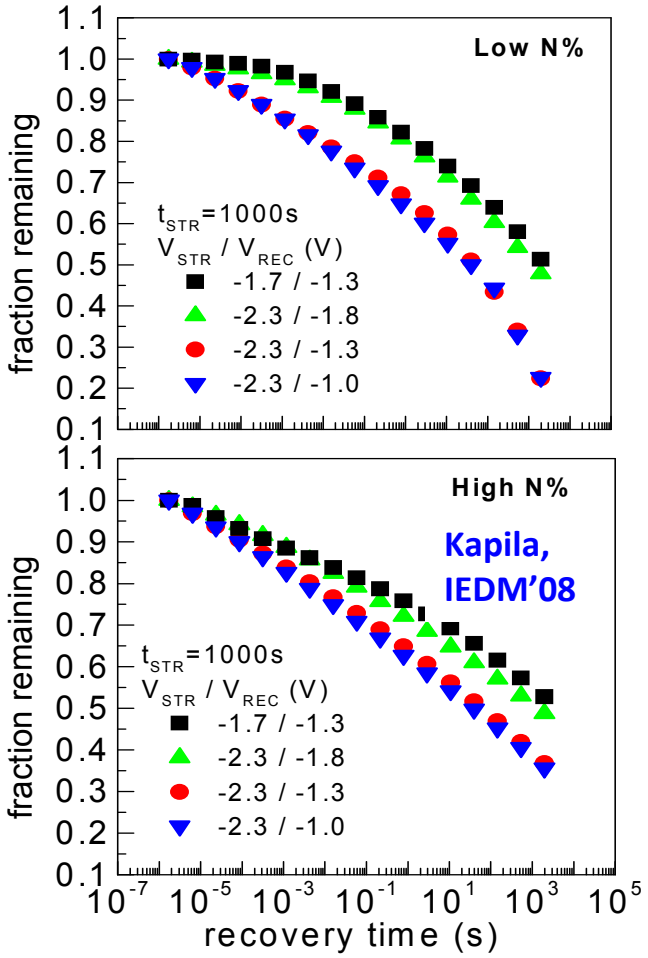
Sakuma IRPS'06

Post Stress NBTI Recovery

Reisinger IRPS'06





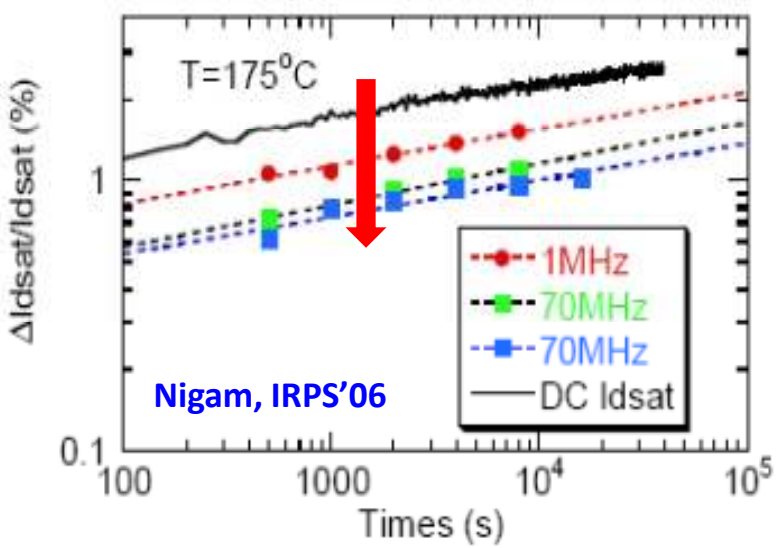


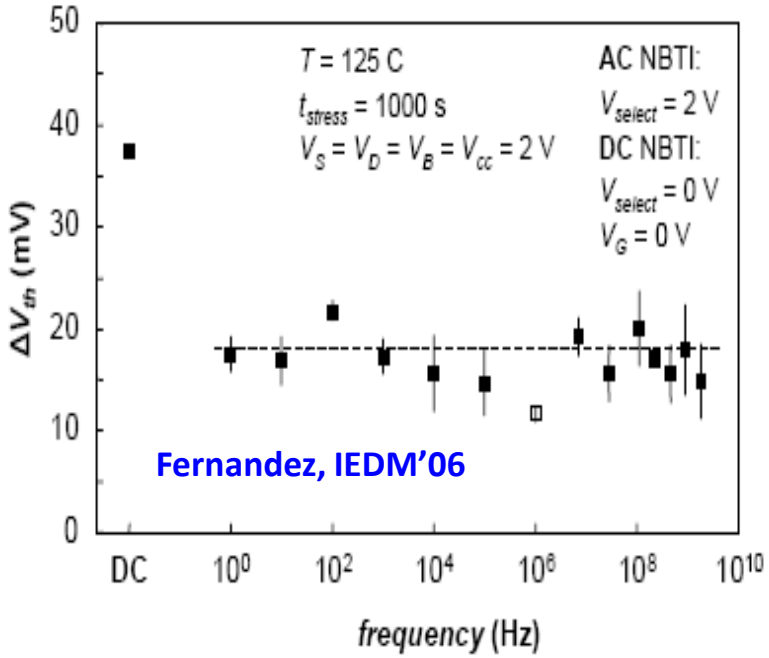
Recovery of degradation after removal of stress

Recovery of subthreshold slope → interface trap passivation

Recovery depends on stress-recovery bias difference and SiON process

DC and AC Stress – Duty Cycle & Frequency

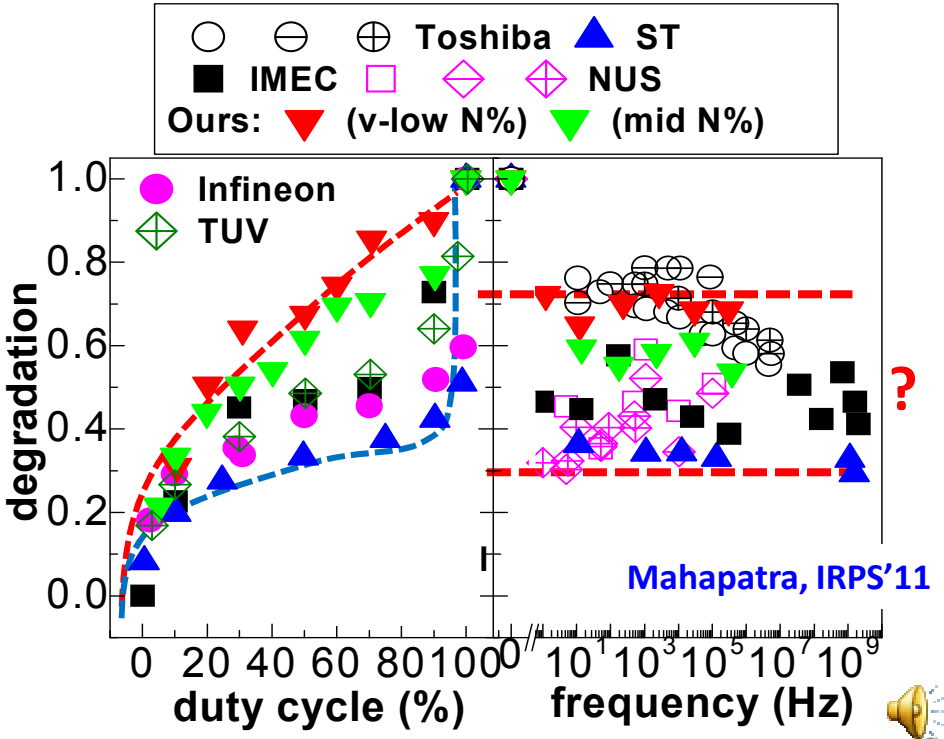




Recovery: Lower NBTI for AC stress

Independent of frequency when properly measured (no high f reflection)

Large spread of published data on duty cycle dependence, AC/DC ratio



Motivation

Explanation of the following features:

- **Strong gate insulator process dependence**
- **Time evolution of degradation, prediction at long time**
- **Temperature and oxide field dependence of degradation**
- **Recovery of degradation after DC stress**
- **Duty cycle and frequency dependence under AC stress**

Understanding and estimation of defects responsible for degradation under accelerated stress condition

Predictive modeling for lifetime projection – extrapolation of short-time accelerated stress data to end-of-life under use condition

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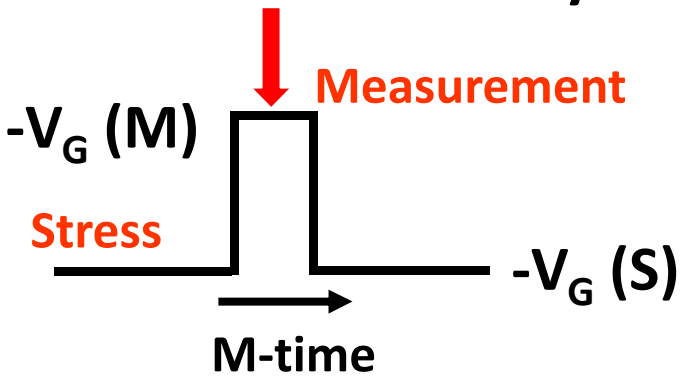
Issues with Measure-Stress-Measure Approach

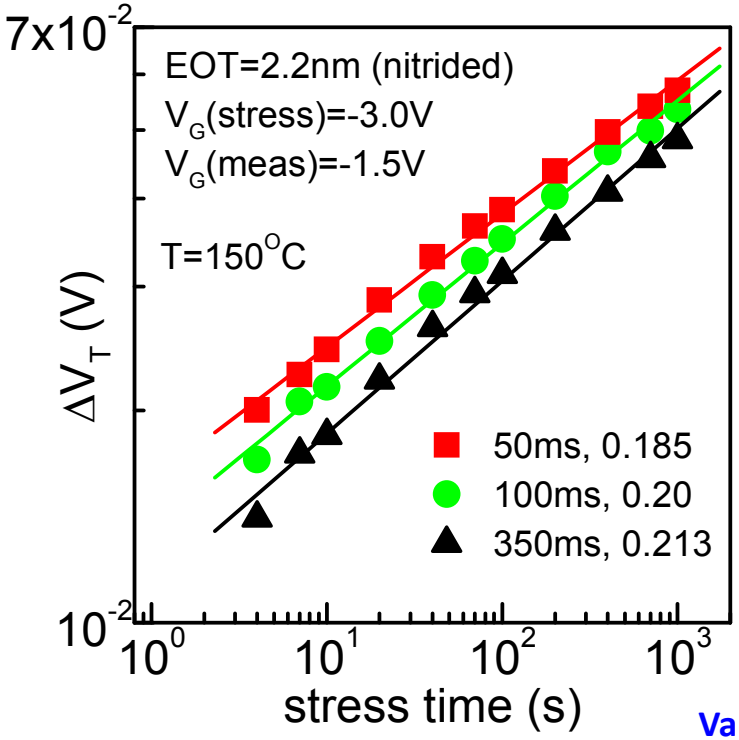
Unintentional recovery during measurement delay

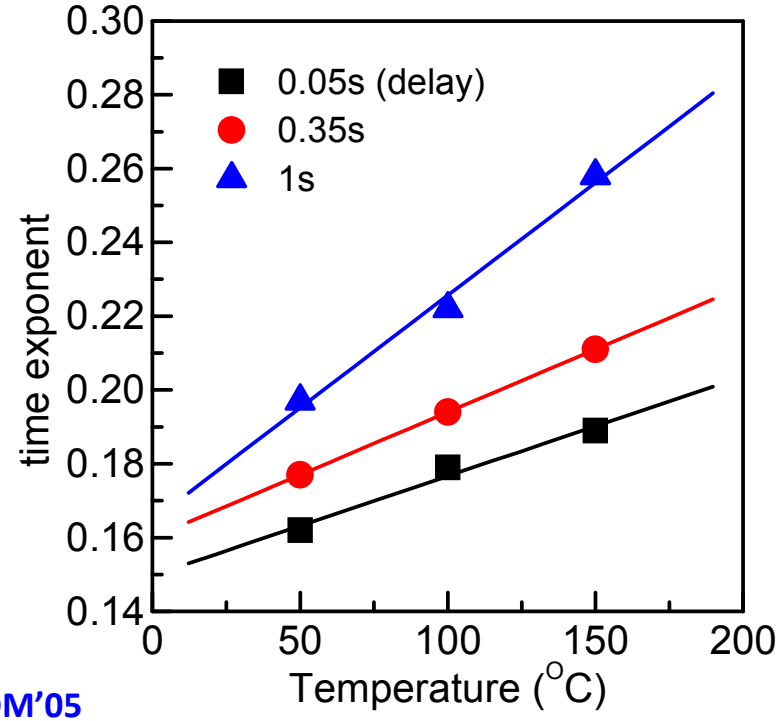


Lower magnitude & higher slope (n) due to recovery during measure delay

Increase in slope (n) with higher T and higher measure delay – artifact

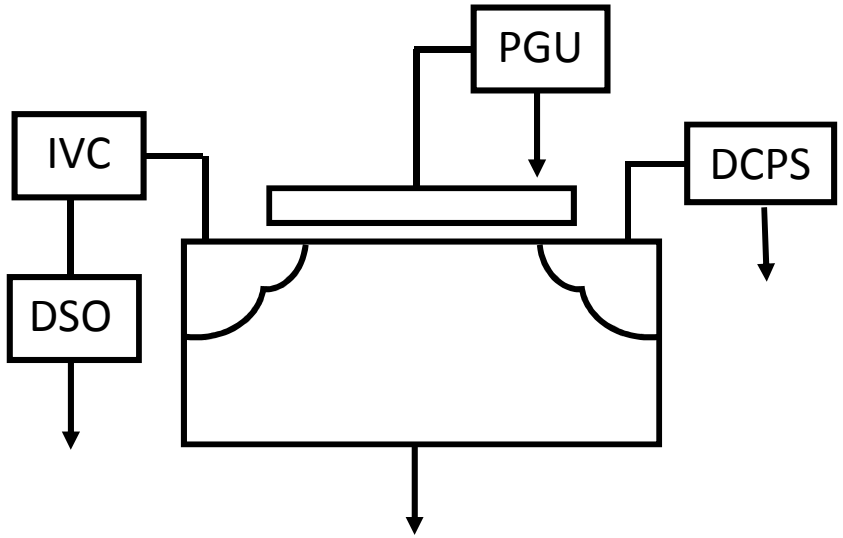
Need "delay-free" measurement

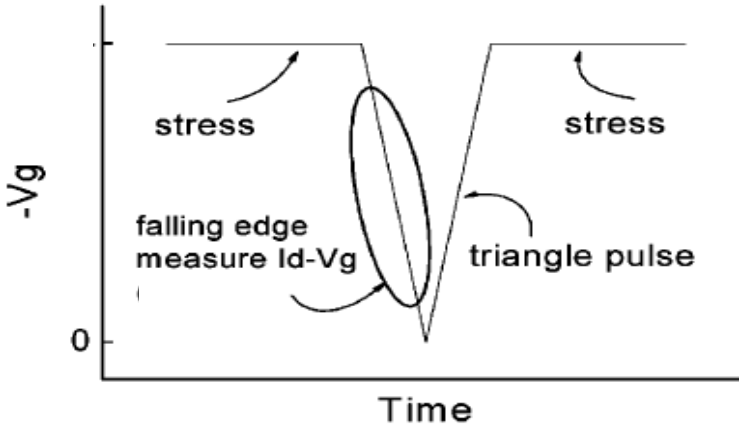




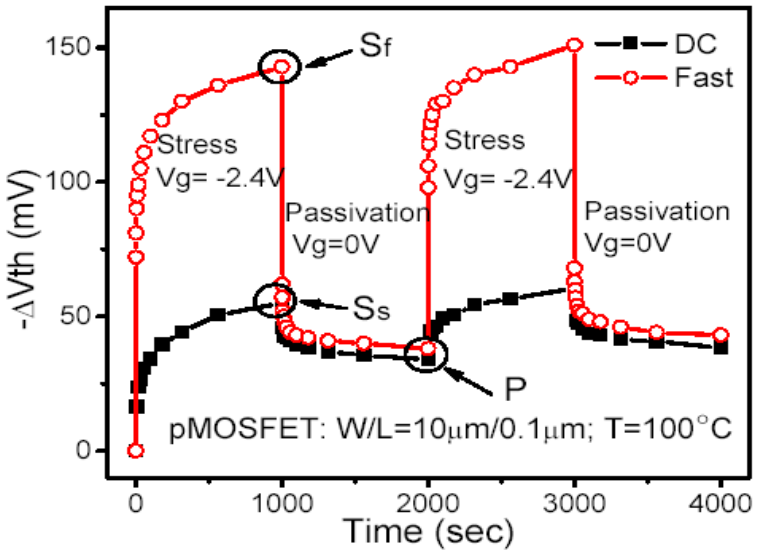
Varghese, IEDM'05

Ultra-Fast Measure-Stress-Measure (MSM) Method





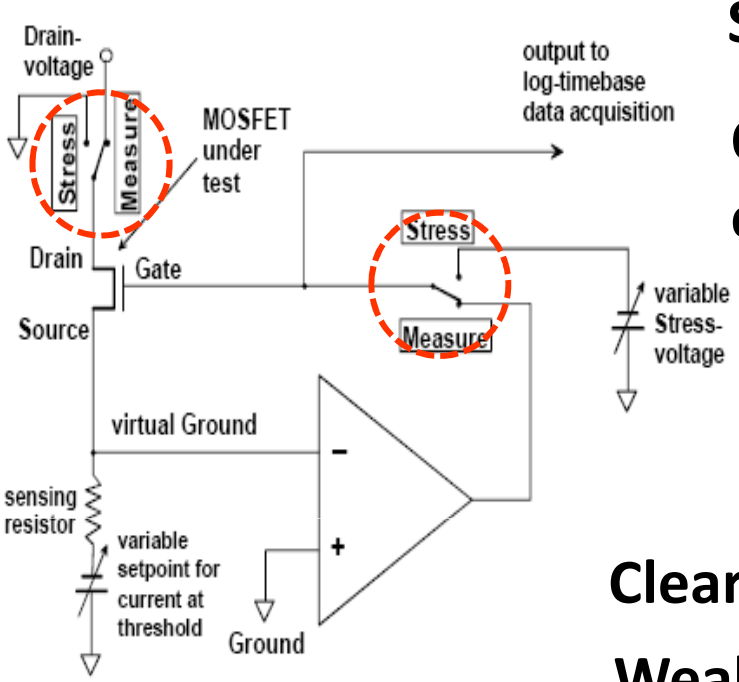
Yang, VLSI'05



Superpose fast triangular pulse on top of stress gate voltage – measure I_D-V_G (hence V_T) using IVC-DSO

Larger degradation and recovery magnitude for fast MSM compared to conventional (slow) MSM

Ultra Fast MSM (Constant Current) Method



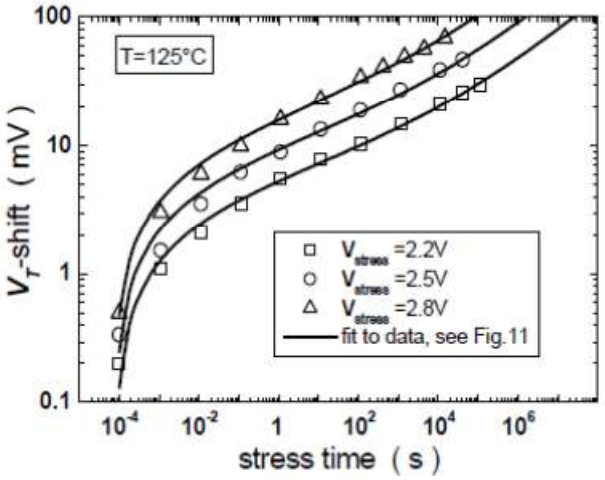
Switch between stress & measure modes

OPAMP based feedback to force constant current in measure mode

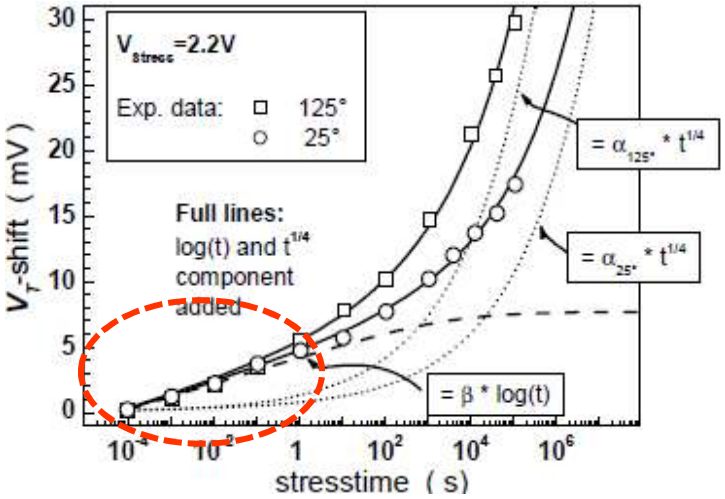
I_D kept constant, change in V_T (due to NBTI stress) gets adjusted by V_G change, hence $\Delta V_T \sim \Delta V_G$

Clear stress V_G dependence of degradation

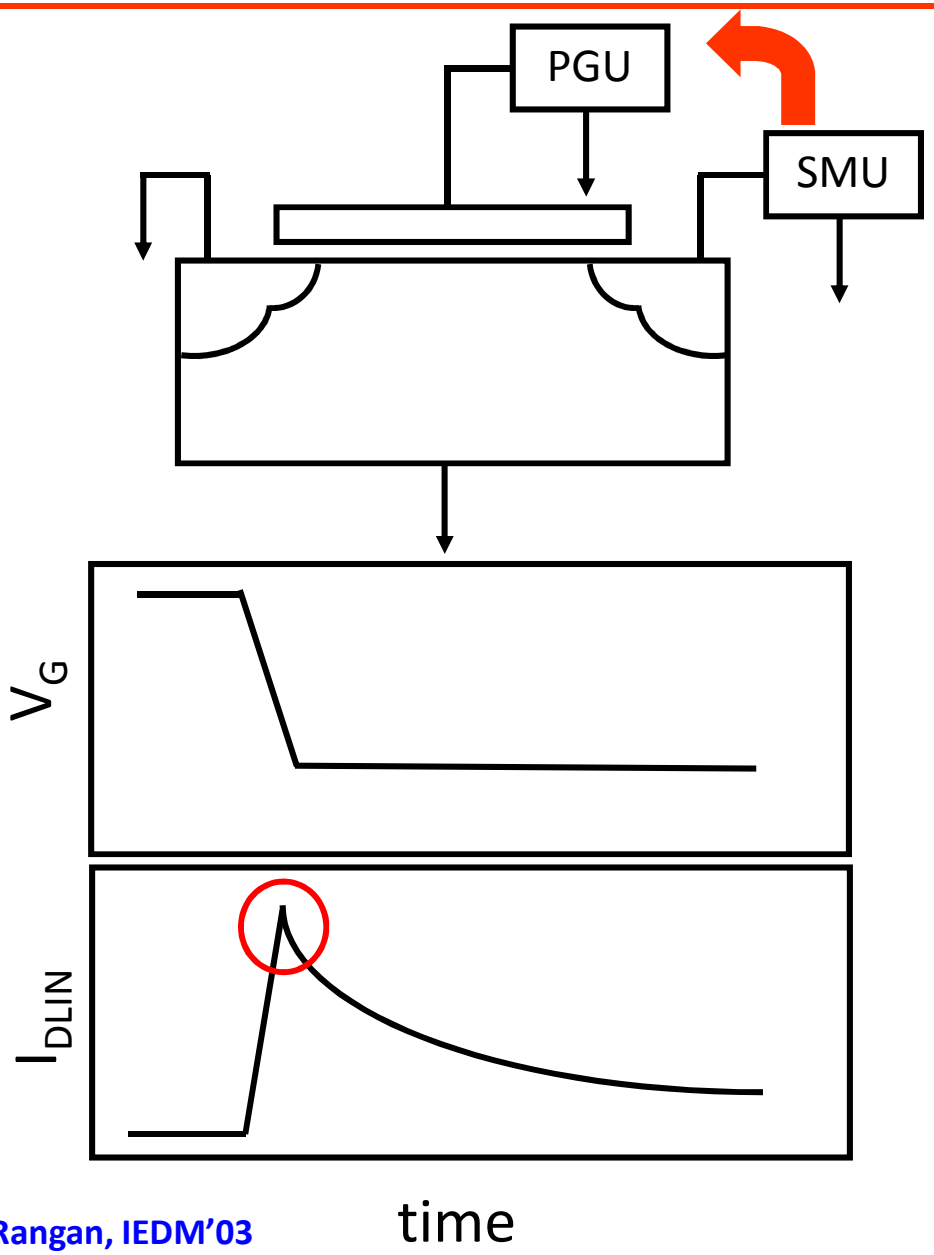
Weak T activation of degradation at short stress time



Reisinger, IRPS'06



On-The-Fly (OTF) I_{DLIN} Method (Conventional)

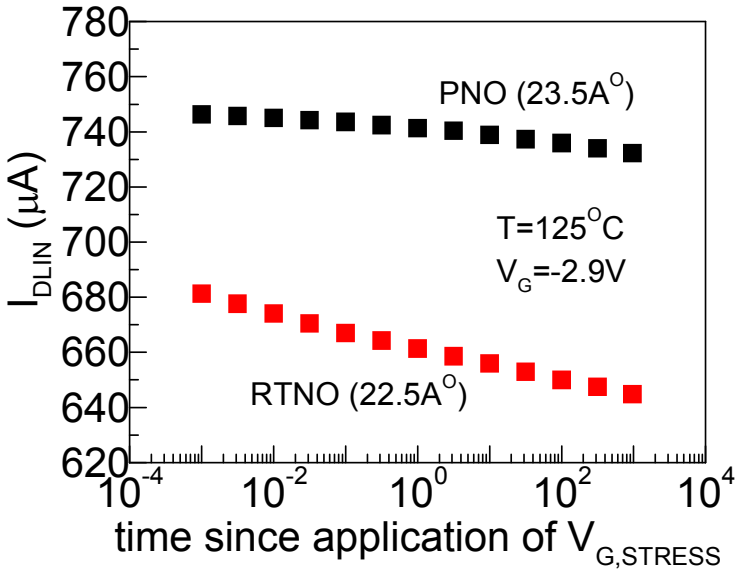


Rangan, IEDM'03

Start I_D sampling in SMU

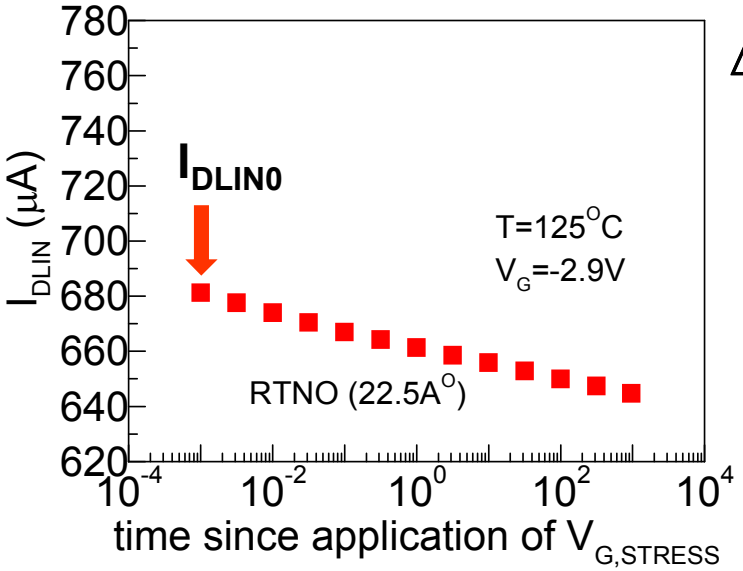
SMU triggers PGU, PGU provides gate stress pulse

Continue I_D sampling without interrupting stress



Delay in I_{DLIN0} measurement: time-zero delay t_0 ~ 1ms

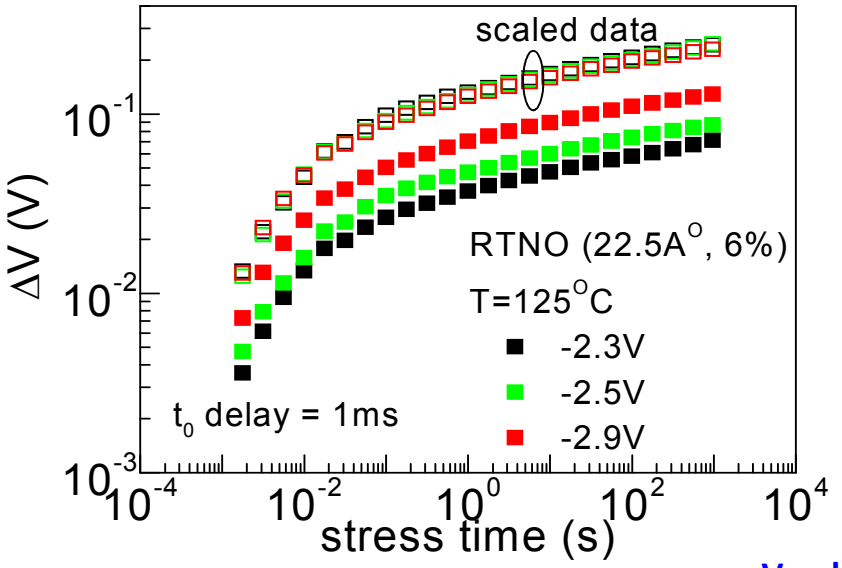
Calculated Degradation from I_{DLIN} Transient

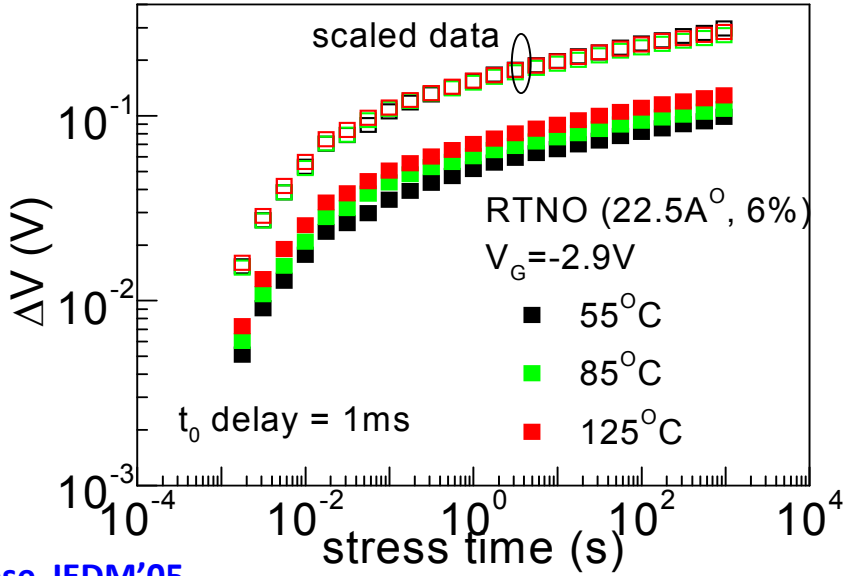


$$\Delta V(t) = -(I_{DLIN}(t) - I_{DLIN0}(1ms))/I_{DLIN0}(1ms)$$

Clear bias dependence for all time – scalable to unique relation

Clear T dependence for all time – scalable to unique relation





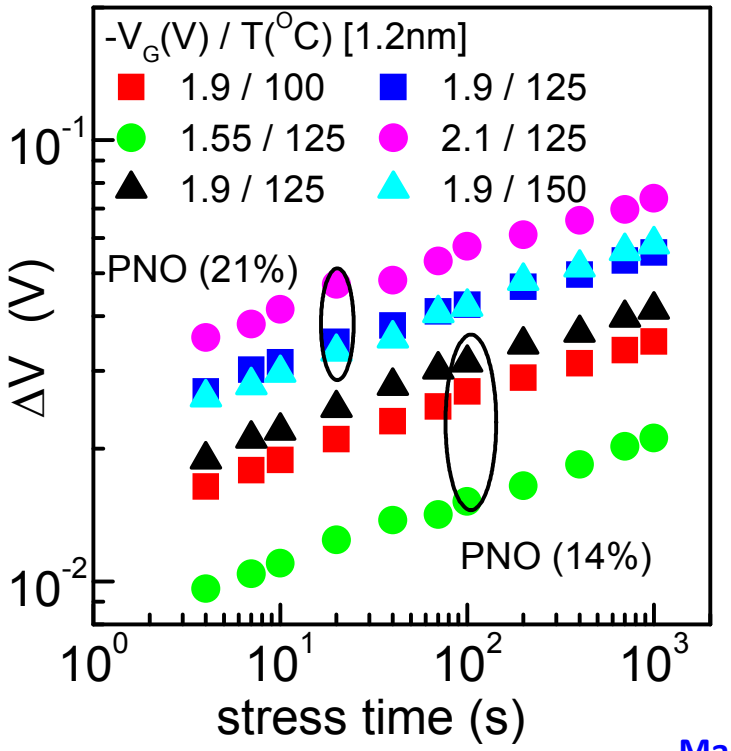
Varghese, IEDM'05

Conventional OTF Measurement Results

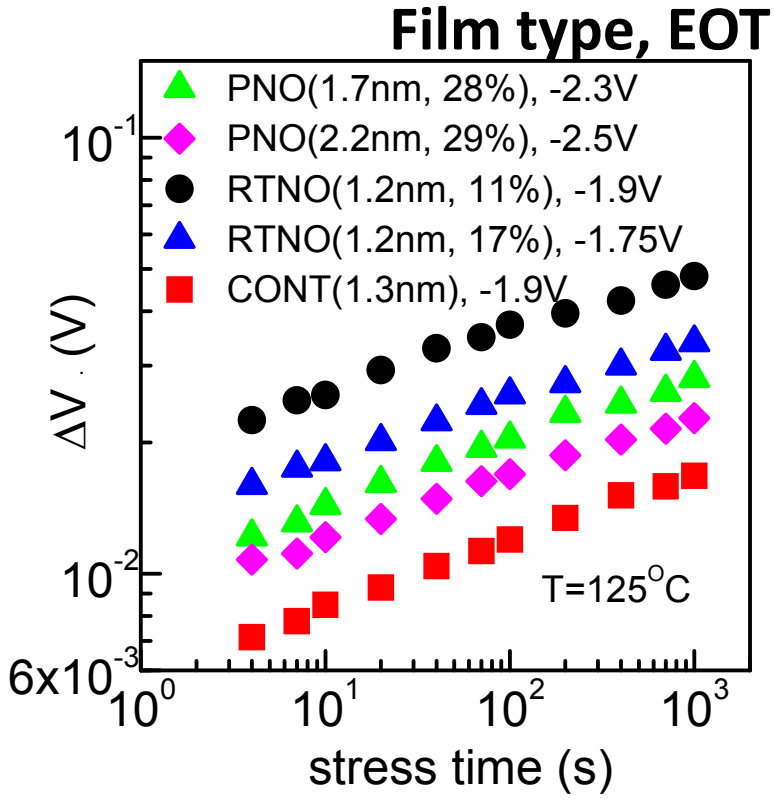
Power law time dependence of longer time data, with time exponent n ~ 0.14-0.15 for all stress bias and temperature

Different magnitude but similar time exponent for different film type (Details of GOX process dependence discussed later)

Stress V_G and T

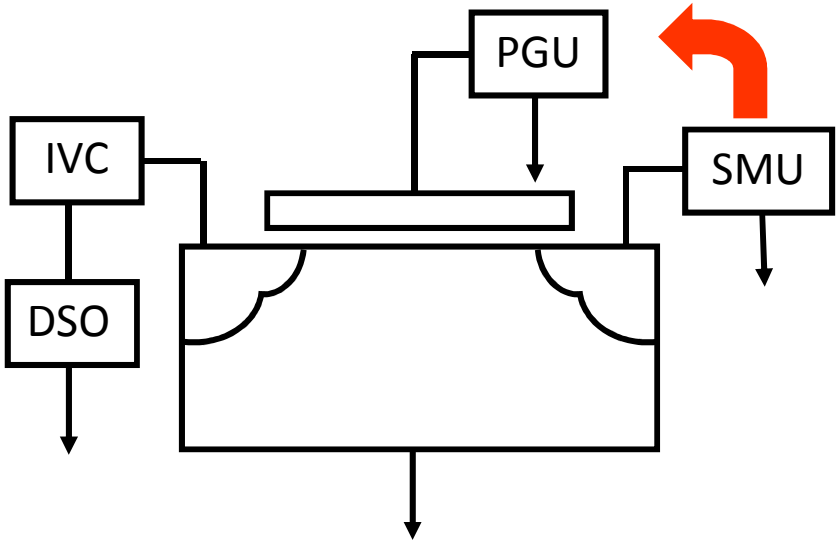


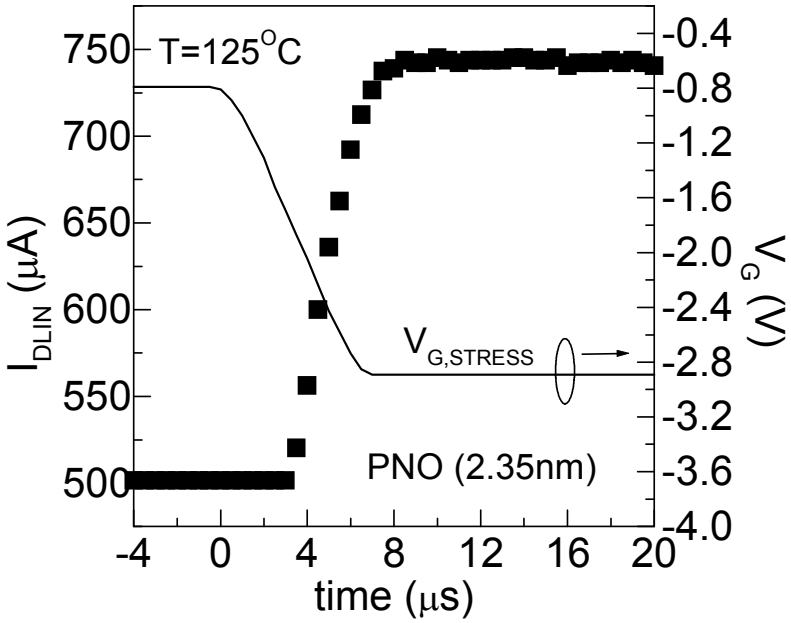
Film type, EOT



Mahapatra, IRPS'07

Ultra-Fast On-The-Fly (UF-OTF) I_{DLIN} Method

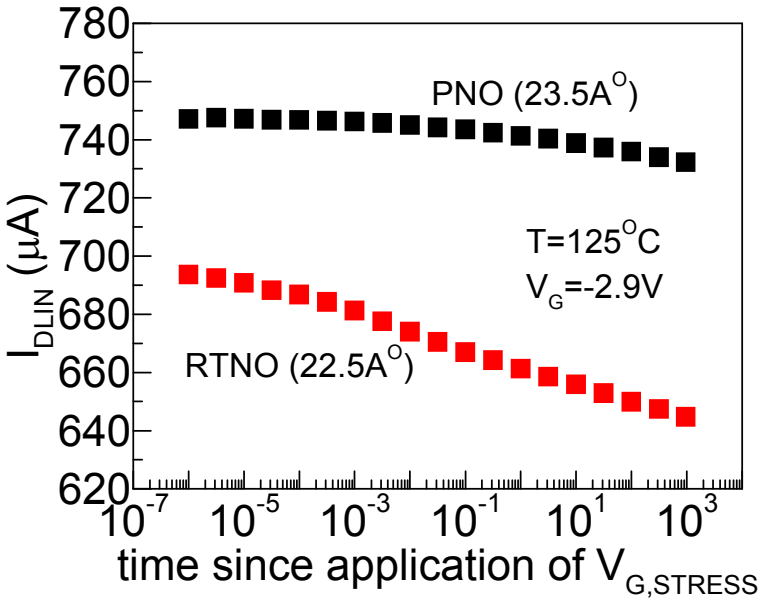




Kumar, IEDM'07

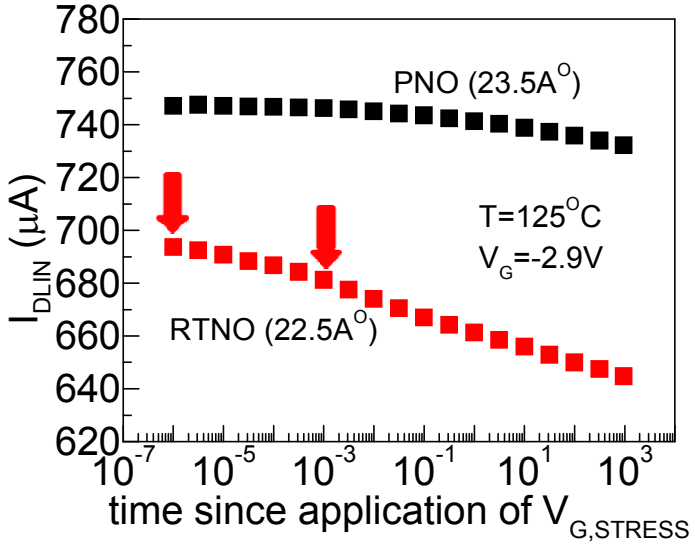
Start I_D sampling (1μs rate) using IVC-DSO, trigger PGU via SMU

Current measurement: Short-time (1μs-100ms) using IVC-DSO, long time (≥1ms) using SMU



Delay in I_{DLIN0} measurement: time-zero delay t_0 ~ 1μs

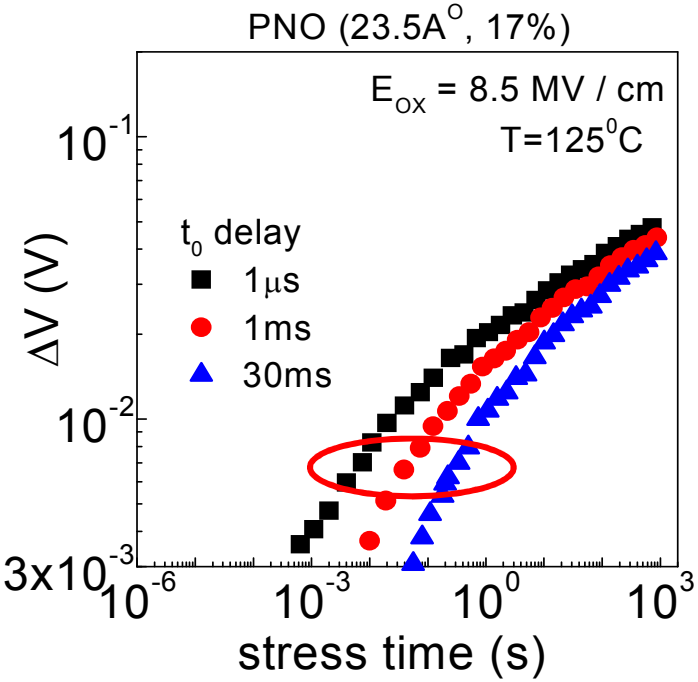
Degradation: Impact of "Time-Zero" Delay

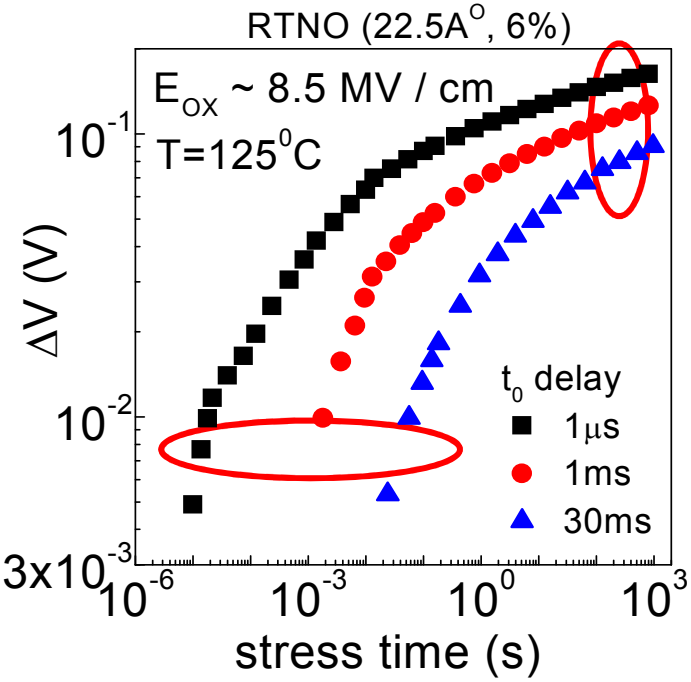


t_0 delay: Time lag between application of stress V_G and measurement of 1st I_{DLIN} data

PNO: Higher NBTI for lower t_0 delay, t_0 delay mostly impacts short-time data

RTNO: Large t_0 impact on short- and long-time data, higher NBTI compared to PNO

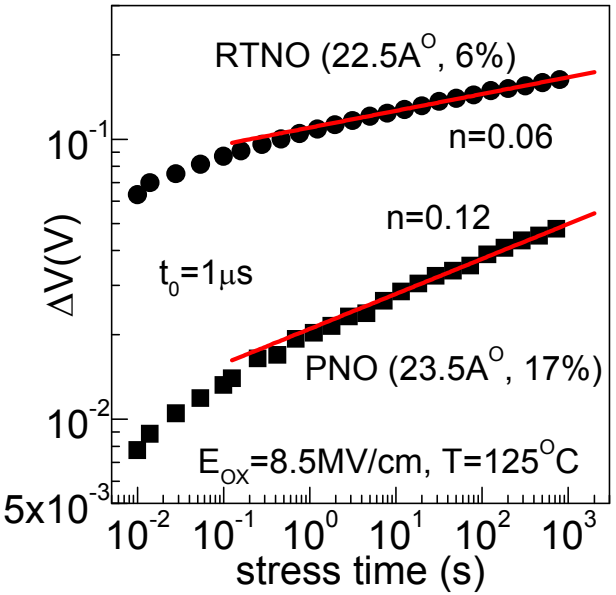


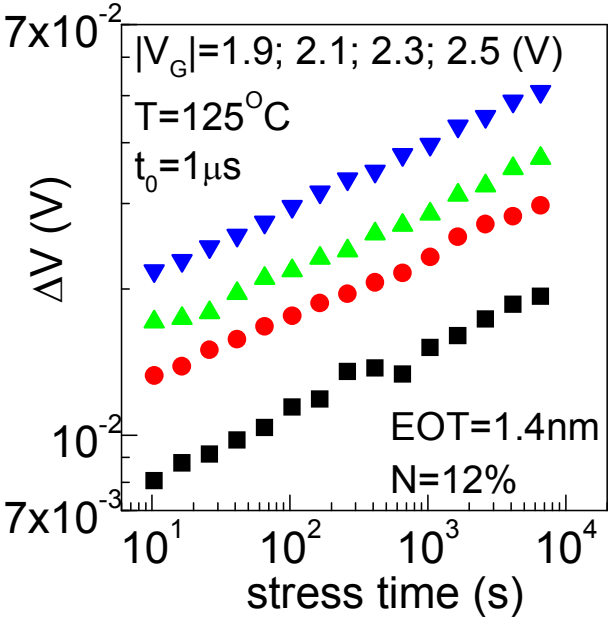


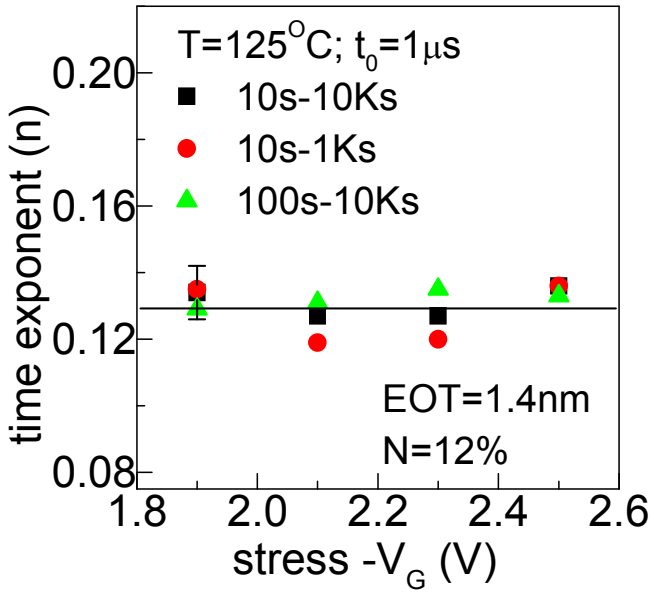
$\Delta V = -\Delta I_{DLIN}/I_{DLIN0} * (V_G - V_{T0})$, where I_{DLIN0} picked at 1μs, 1ms and 30ms

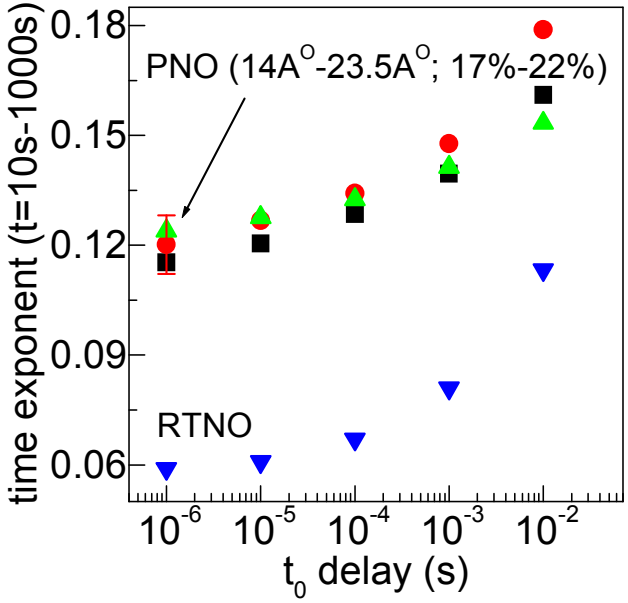
Maheta, PhD thesis (IITB)

Time Evolution of Long-time Degradation









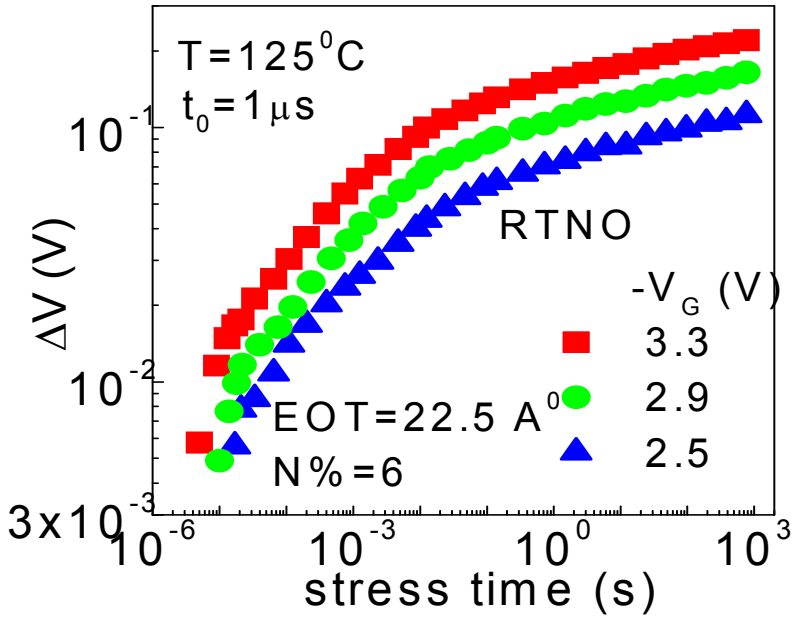
Power-law time dependence at longer stress

Similar n for different stress V_G, time range for linear fit

Time exponent (n) depends on t_0 delay – reduces at lower t_0 but saturates for t_0 < 10μs

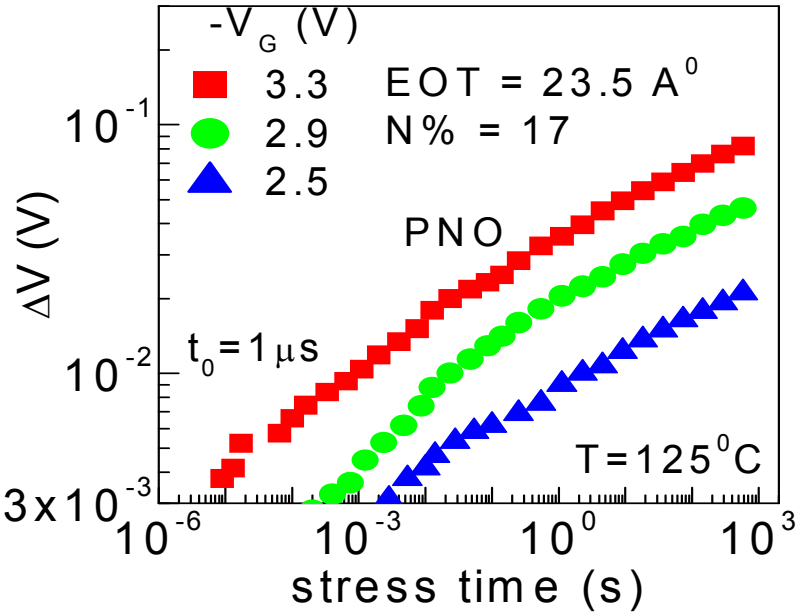
Maheta, PhD thesis (IITB)

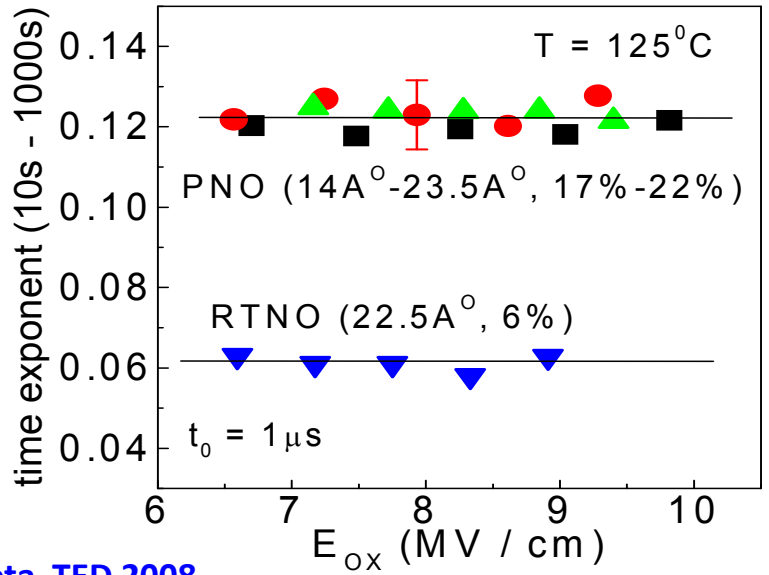
UF-OTF: Bias Dependence of Degradation



RTNO shows higher magnitude and lower bias dependent acceleration compared to PNO

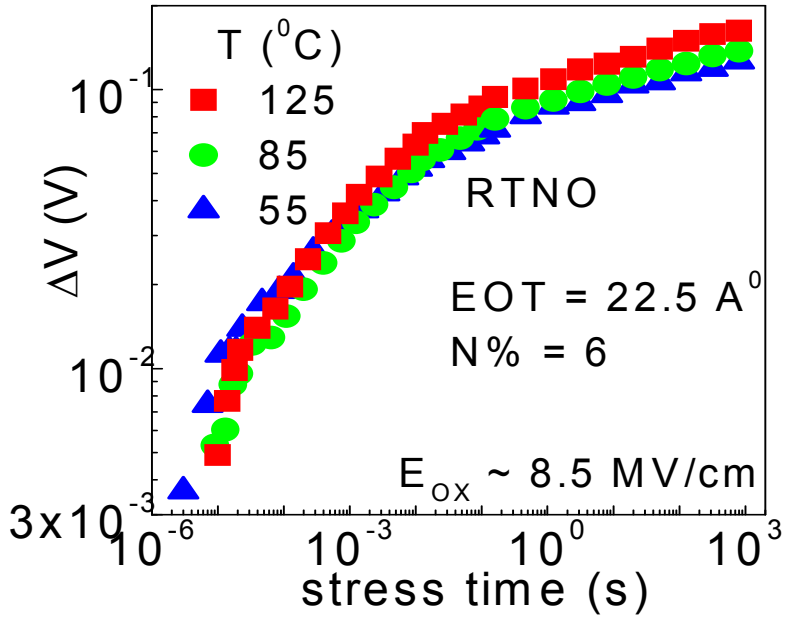
Lower long-time power law time exponent (n) for RTNO compared to PNO – n independent of oxide field

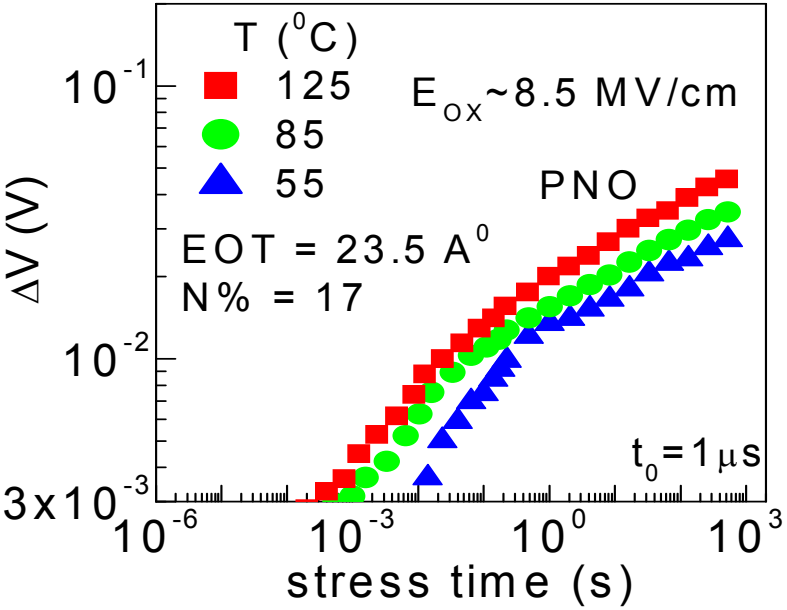




Maheta, TED 2008

UF-OTF: Temperature Dependence of Degradation

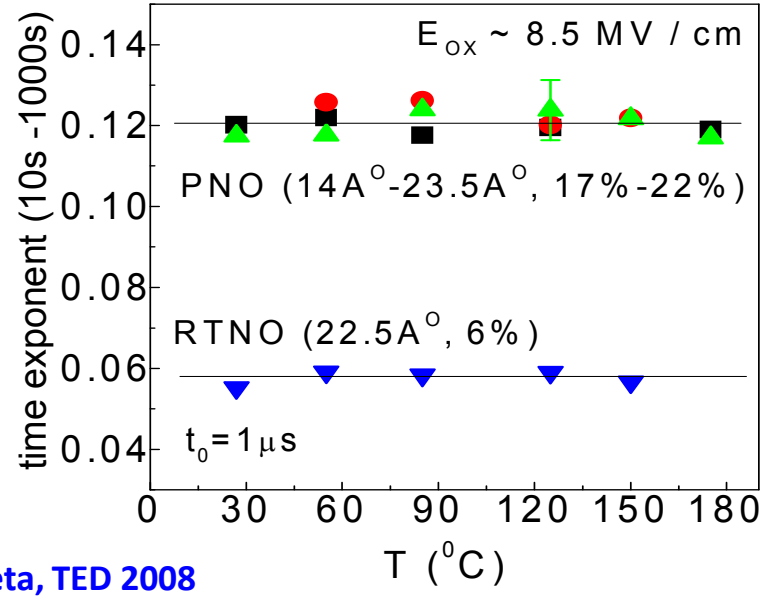




RTNO shows negligible T dependence at short time, weak T activation at longer time

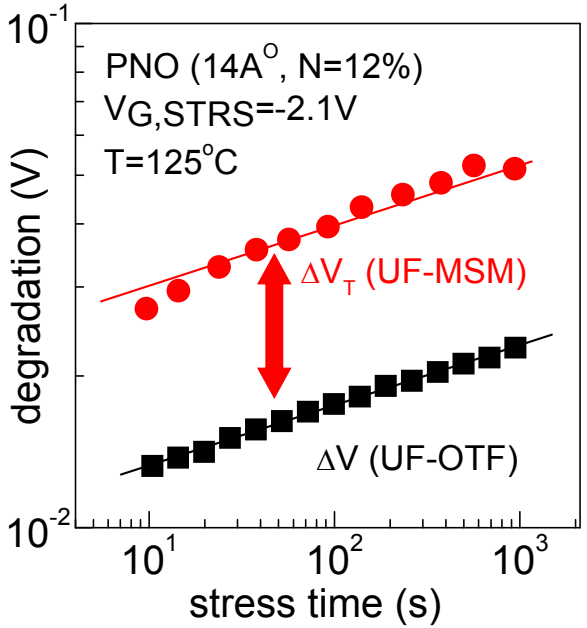
PNO shows strong T activation from short to longer time

Long-time power law time exponent (n) independent of T (no delay artifact)



Maheta, TED 2008

Mobility Correction

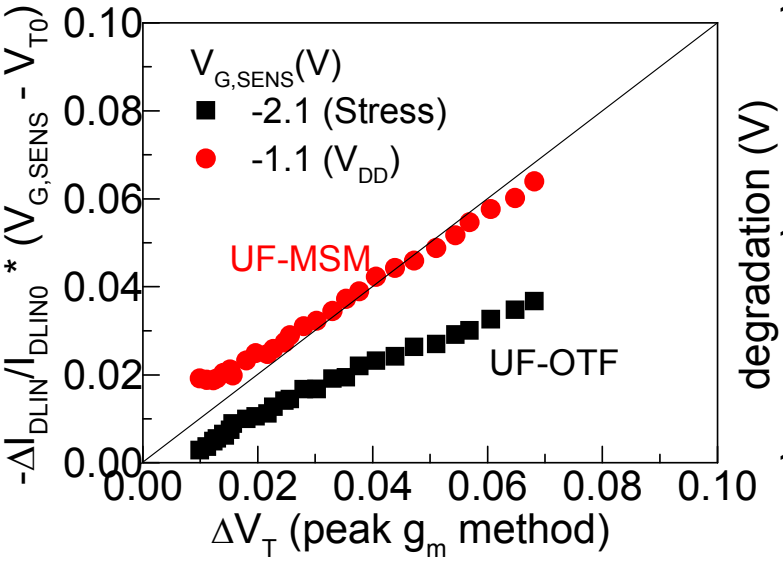


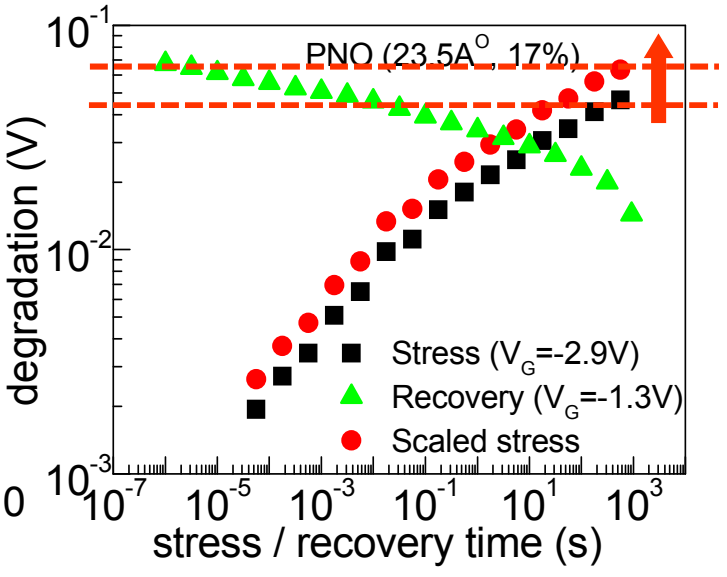
Difference between ΔV (OTF) and ΔV_T (MSM, peak gm method) due to mobility degradation

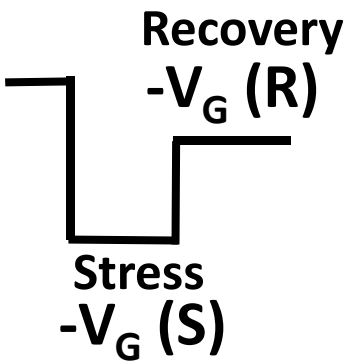
ΔV read at V_{DD} gives 1:1 correlation with ΔV_T

OTF: Stress followed by recovery at V_G=V_{DD}

Scaling end of stress data to recovery data measured at 1μs enforces mobility correction







Mobility correction: Islam, IRPS'08

Summary

Recovery of NBTI degradation after removal of stress – issues with conventional "slow" MSM methods

Ultrafast MSM can provide V_T shift with negligible artifacts, is useful for capturing long time degradation for lifetime determination, early part (t<1s) degradation cannot be studied

Constant current ultrafast MSM method is an alternative, but needs subthreshold slope correction to determine proper V_T shift

On-the-fly (OTF) I_{DLIN} methods can be used to study degradation from 1ms (fast version) and 1μs (ultra-fast version) time scale

Important process dependent signatures observed in sub ms time scale by UF-OTF method (discussed in detail later)

OTF I_{DLIN} needs mobility correction to obtain V_T shift

Outline

Introduction, Basic NBTI signatures

Fast / Ultra-fast drain current degradation measurement

Estimation of pre-existing and generated defects ⬅

Transistor process / material dependence

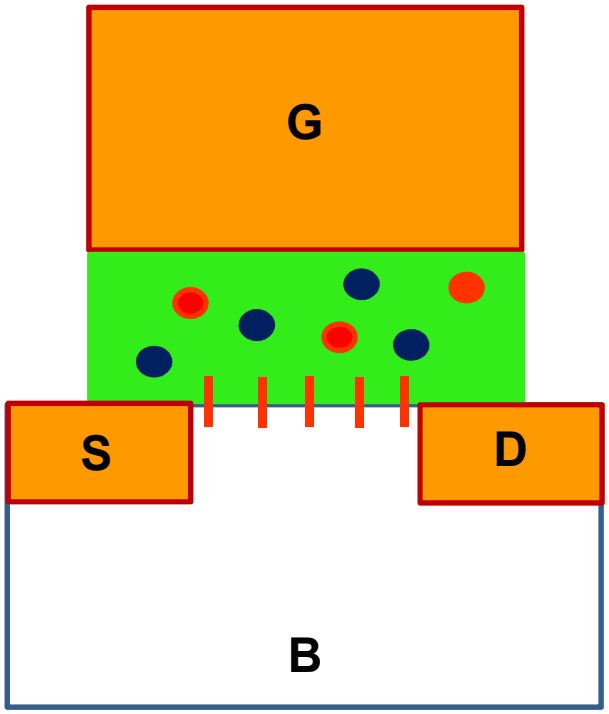
Role of Nitrogen – Study by Ultrafast measurement

Predictive modeling

Conclusions / outlook

Background – The "Philosophy"

I-V measurements (previous section) influenced by generation of interface and bulk traps, plus trapping in pre-existing traps



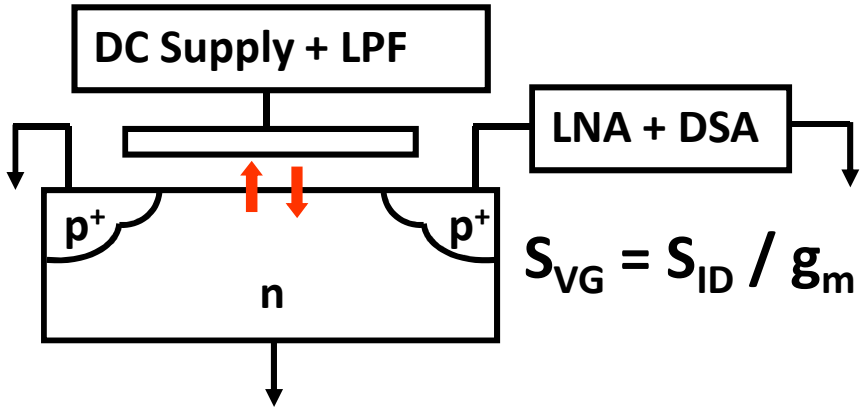
How to independently estimate pre-existing traps? Eg: Flicker noise

How to independently estimate interface and bulk trap generation? Eg: DCIV, Charge pumping, Flicker noise, LVSILC and SILC

Can different measurements be correlated?

Flicker Noise Measurement (Pre-stress)

Measure I_D power spectral density versus frequency at low gate overdrive

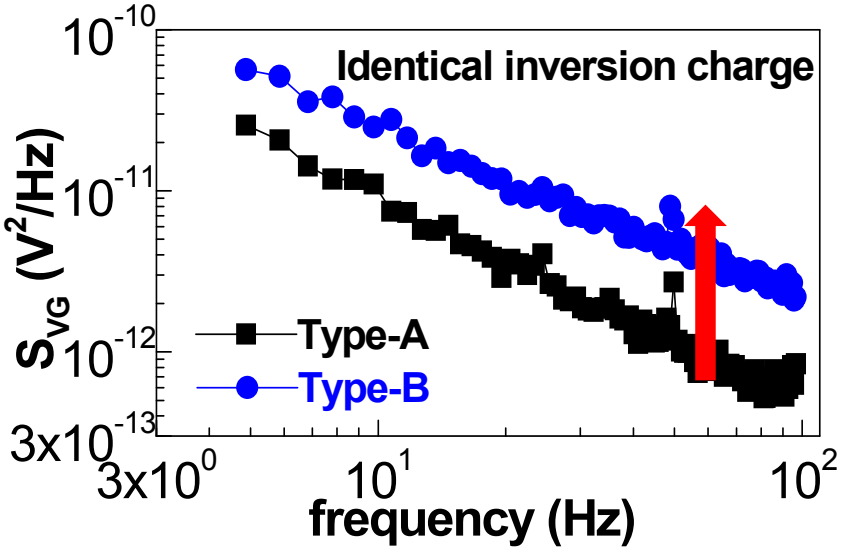


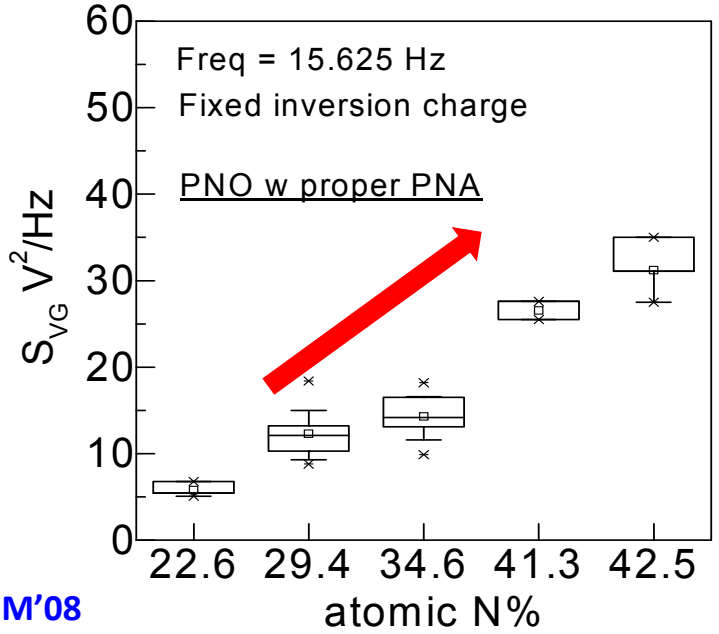
$S_{VG} = S_{ID} / g_m$

Flicker noise due to trapping/ detrapping of holes in oxide traps

High pre-existing hole trap density for certain (type-B) devices

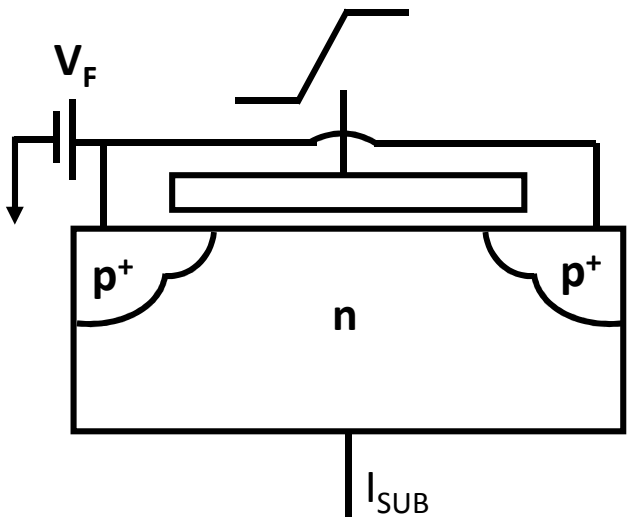
Increase in pre-existing hole trap density with N density





Kapila, IEDM'08

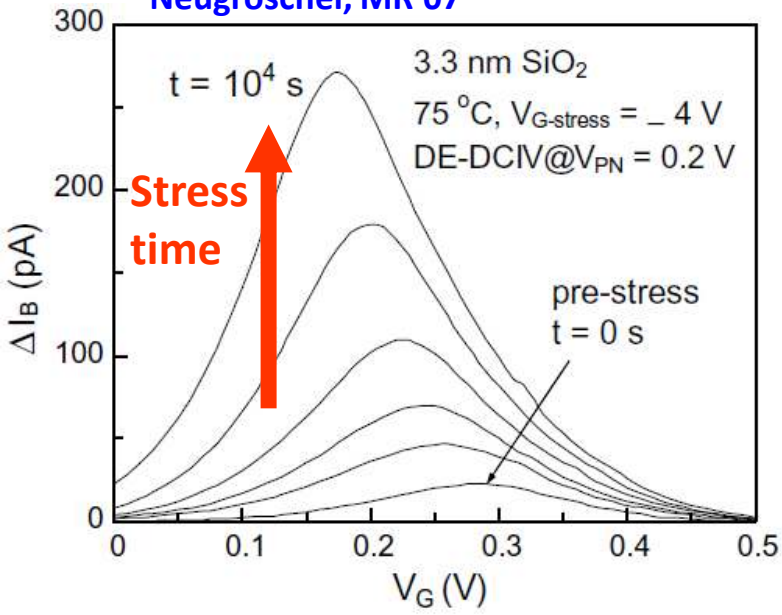
DCIV Measurements



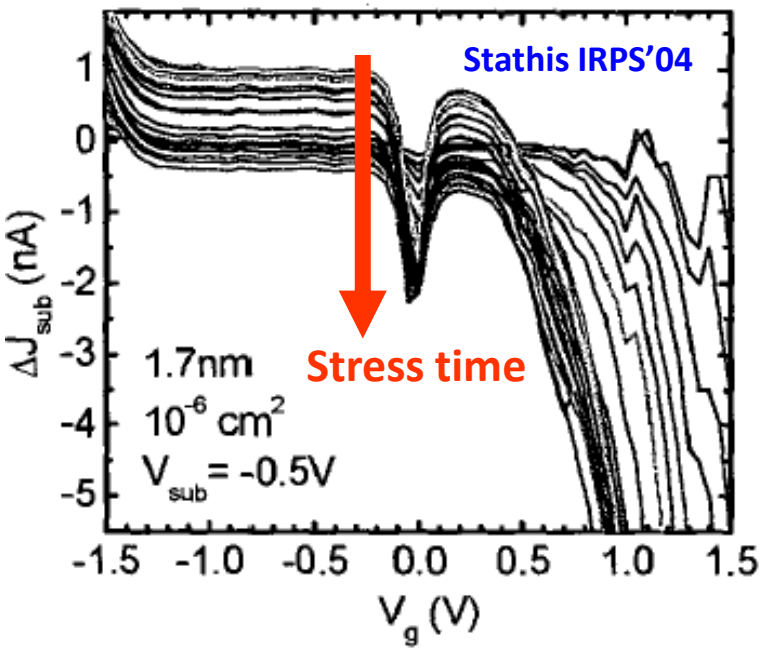
Sweep V_G with S/D in F.B, measure I_{SUB} due to electron-hole recombination in traps at or near Si/SiO_2 interface

Increase in I_{SUB} due to stress seen in both SiO_2 and SiON: Indicates trap generation at or near Si/SiO_2 interface

Neugroschel, MR'07

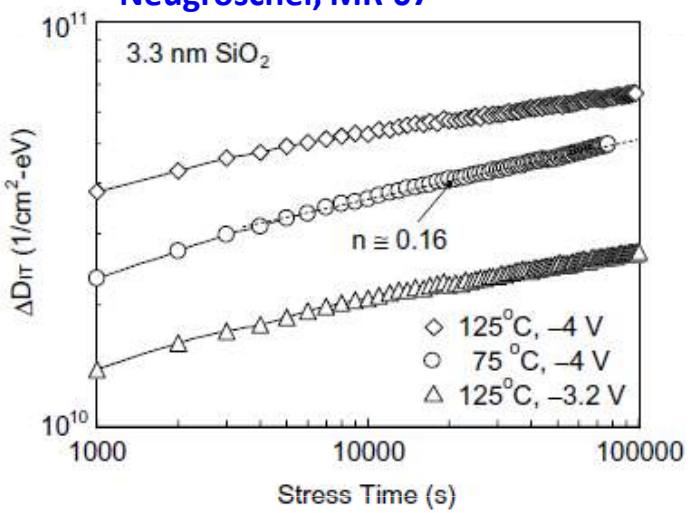


Stathis IRPS'04



DCIV Measurements

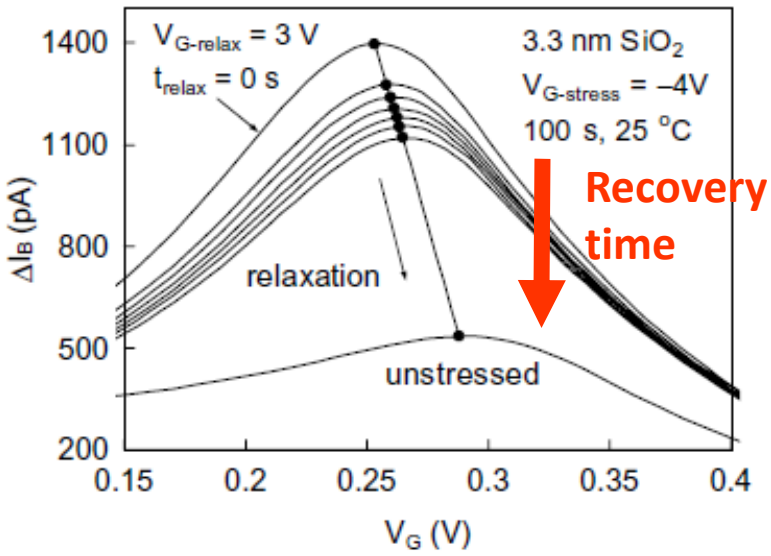
Neugroschel, MR'07

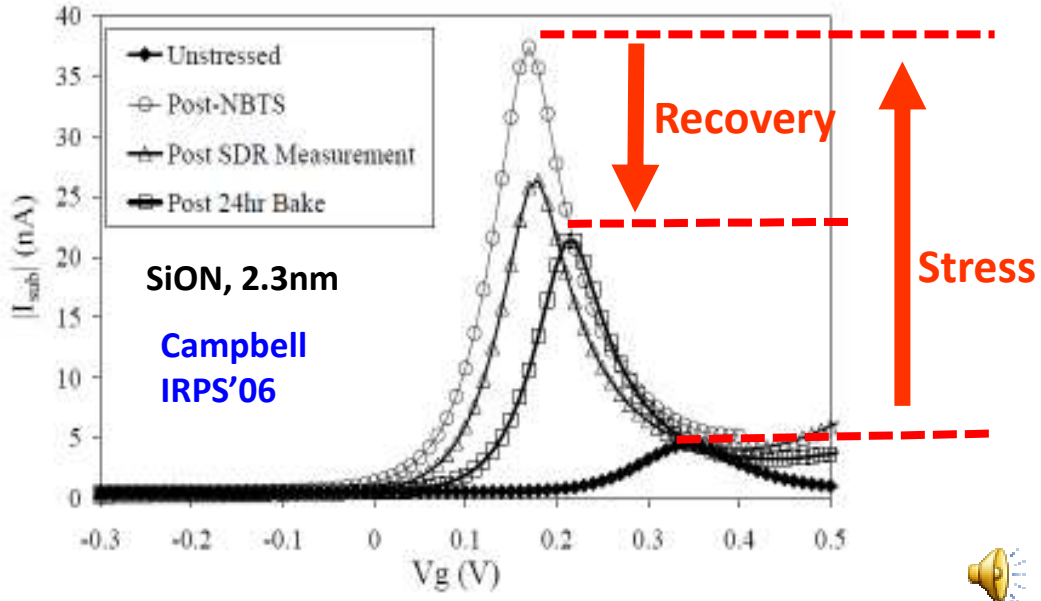


Power law time dependence ($A*t^n$), with n ~ 1/6 at long stress time for different stress V_G and T

Reduction in I_{SUB} after stress seen in both SiO_2 and SiON: Indicates recovery of generated traps

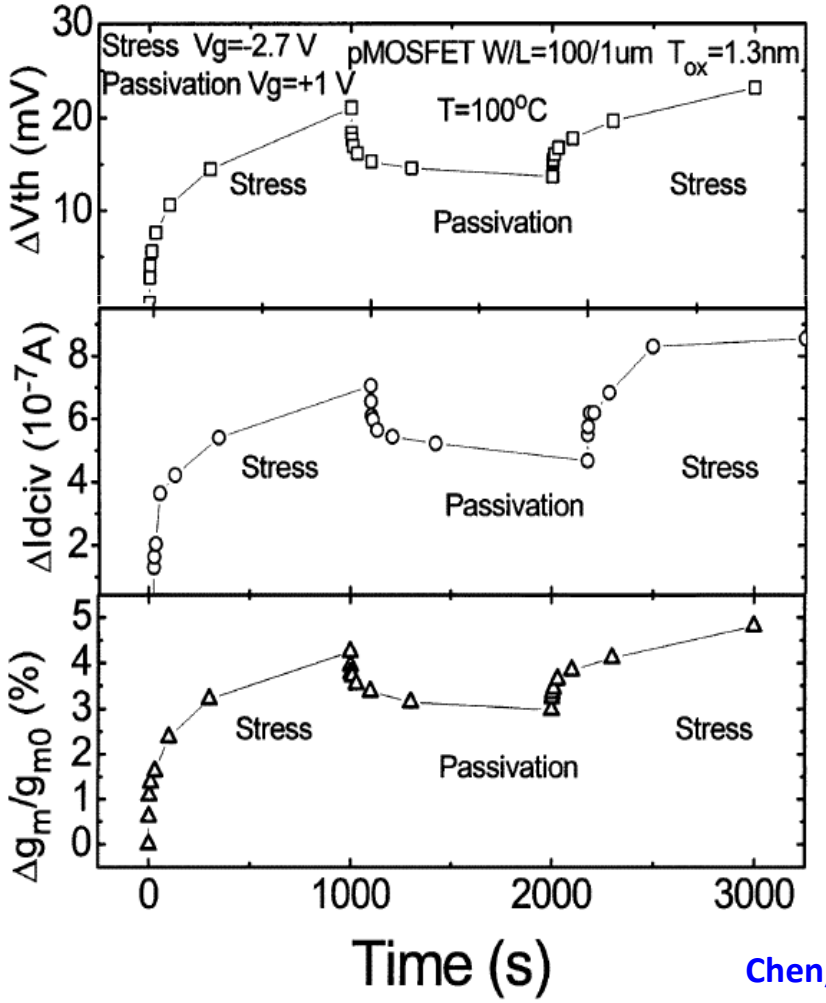
Neugroschel, MR'07



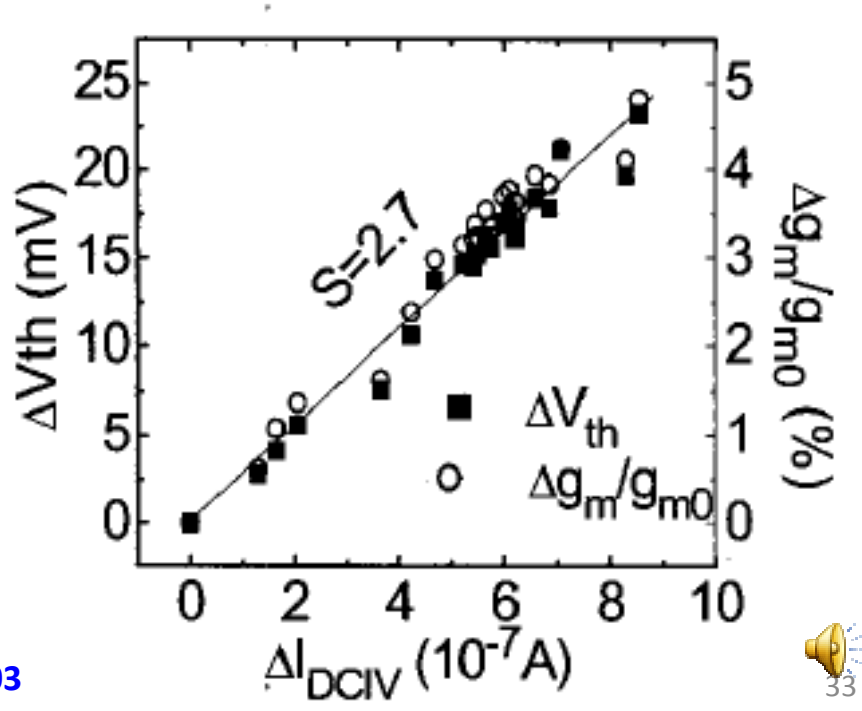


Correlation of DCIV to I-V Measurements

Similar degradation and recovery signatures across different methods: ΔV_T, Δg_m (from slow MSM I-V) and ΔI_{DCIV} (DCIV)

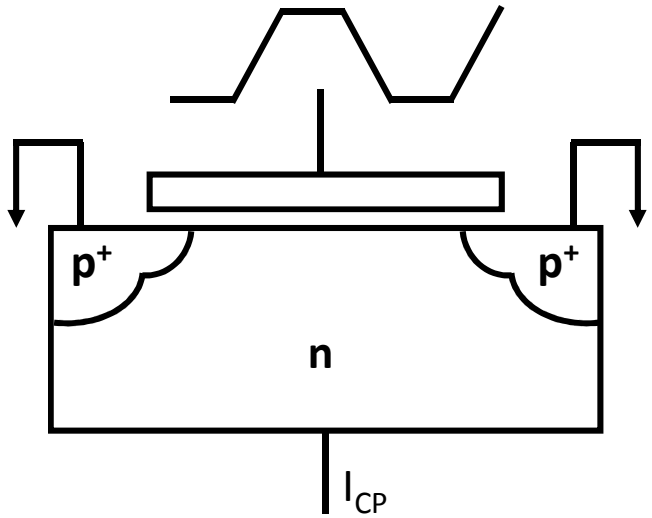


Good correlation of ΔI_{DCIV} to ΔV_T & Δg_m degradation during stress and recovery



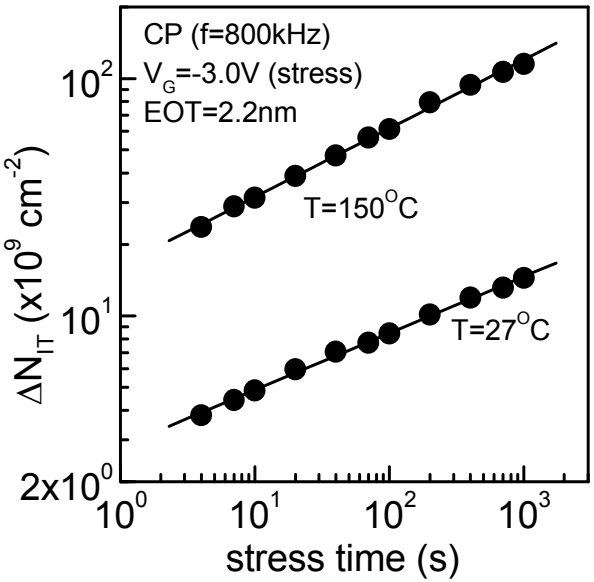
Chen, IRPS'03

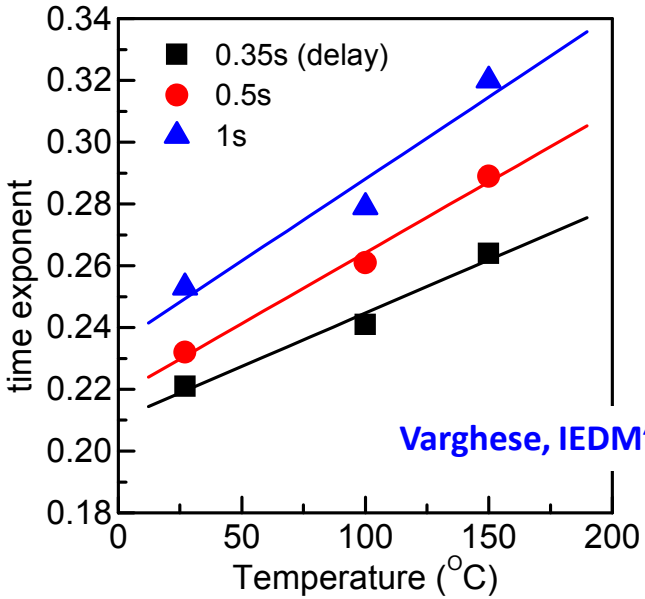
Charge Pumping Measurements



Pulse V_G repetitively from inversion to accumulation, measure I_{SUB} due to electron-hole recombination in traps at Si/SiO_2 interface and inside SiO_2 bulk

CP current increase (trap generation) with stress time - power law time dependence - larger n than I_{DLIN} measurement

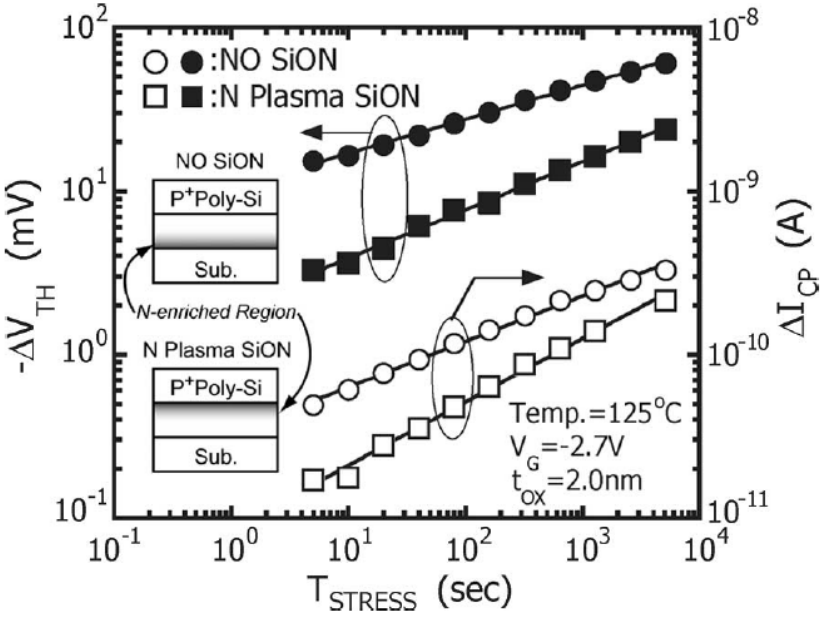




Varghese, IEDM'05

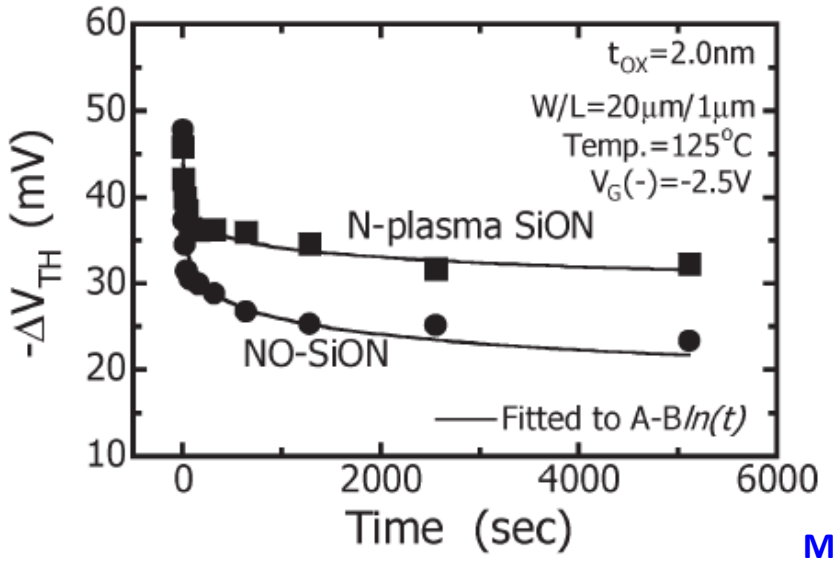
Time exponent increases with delay time and stress T – recovery related artifact

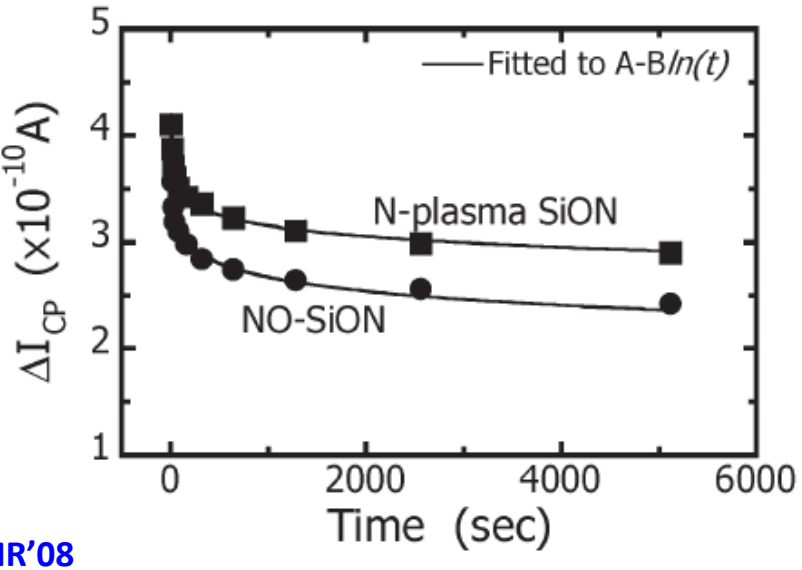
Correlation of CP to I – V Measurements



Both ΔV_T (slow MSM) and ΔI_{CP} shows power law time dependence and higher degradation for NO-SiON

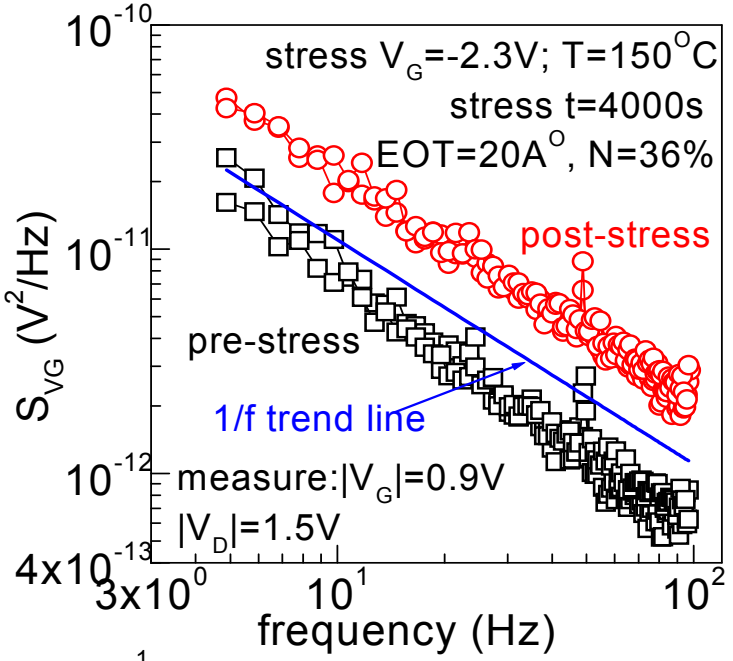
Both ΔV_T (slow MSM) and ΔI_{CP} shows recovery of degradation, and larger recovery for NO-SiON

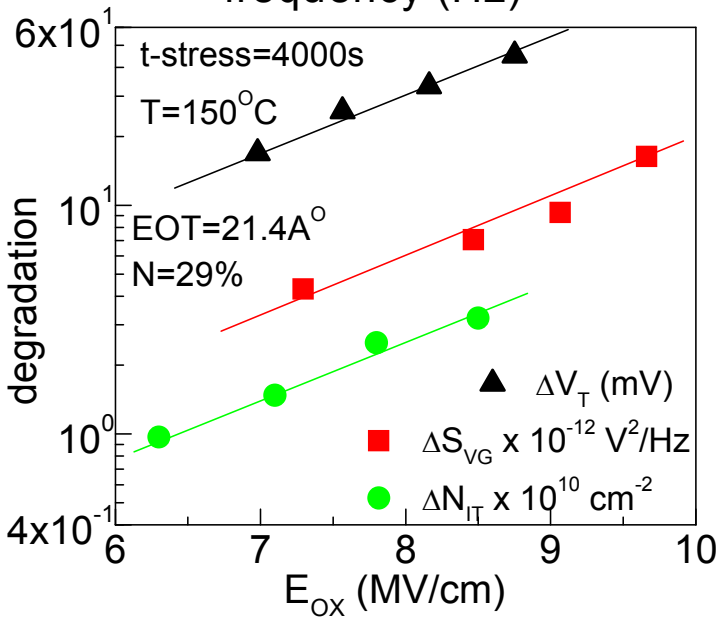




Mitani, MR'08

Impact of Stress on Flicker Noise

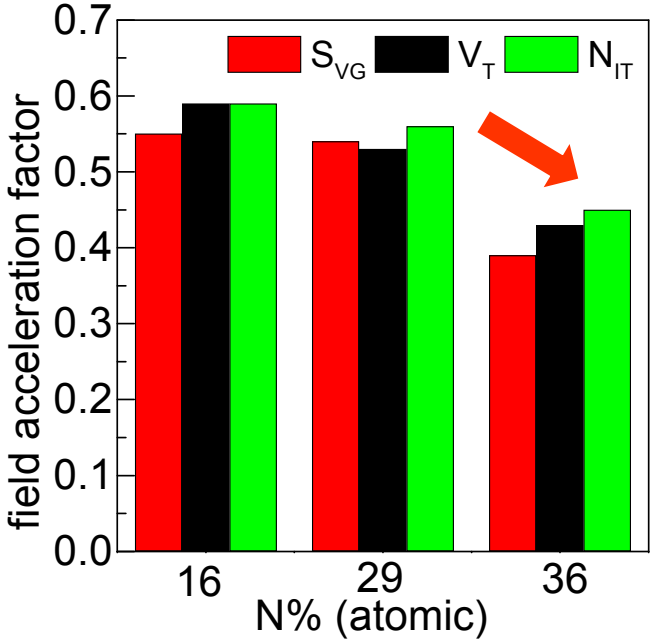




Increase in flicker noise after stress → generation of traps

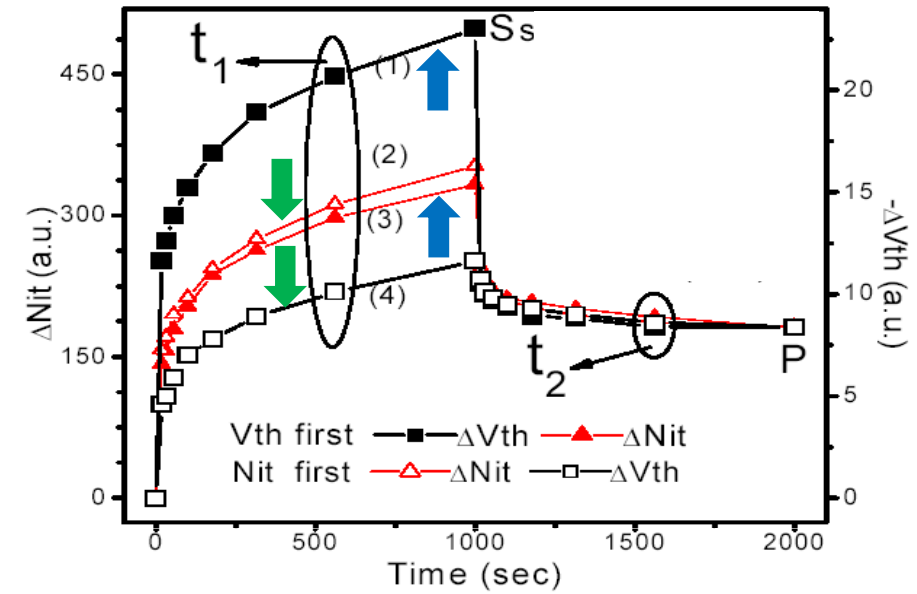
Similar voltage acceleration (Γ) of ΔV_T (I-V), ΔN_{IT} (CP) and ΔS_{VG} (Noise)

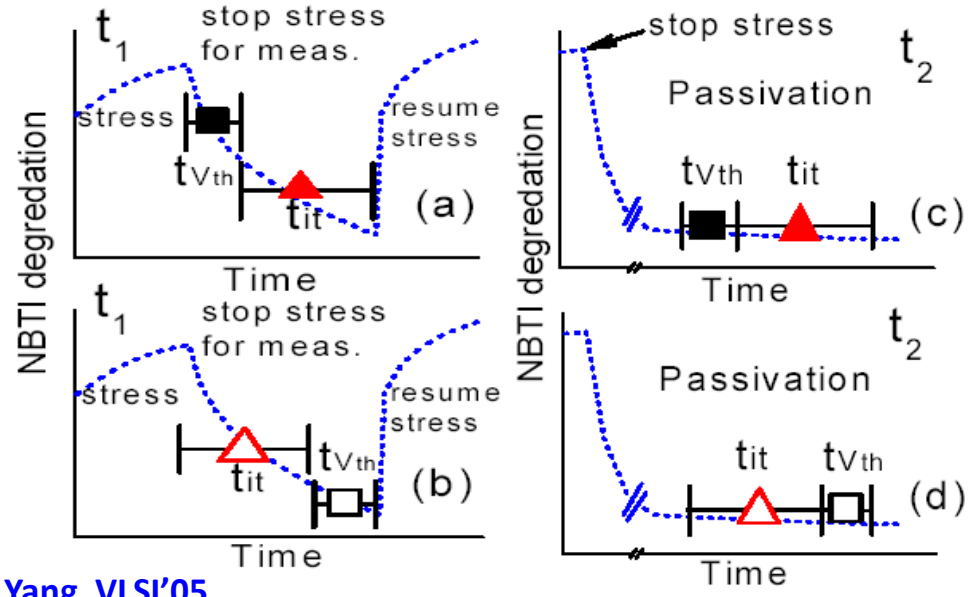
Similar reduction of Γ for ΔV_T, ΔN_{IT} and ΔS_{VG} with increase in N (trap generation near interface)



Kapila, IEDM'08

Direct Comparison of Multiple Measurements





Yang, VLSI'05

Two measurement methods in sequence to determine ΔV_T and ΔN_{IT} during stress and recovery

Measured degradation (during stress) depends on measurement sequence

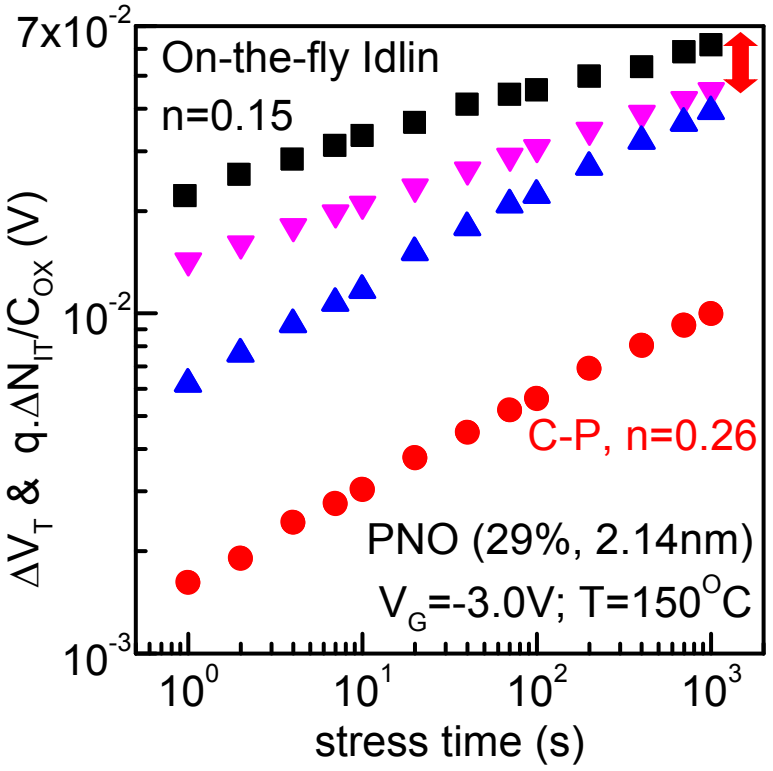
Measurement (stress off) triggers recovery, captured degradation depends on measurement time and gate voltage during measurement

Less issue if measured long time after stress is stopped, as recovery goes in log-time scal

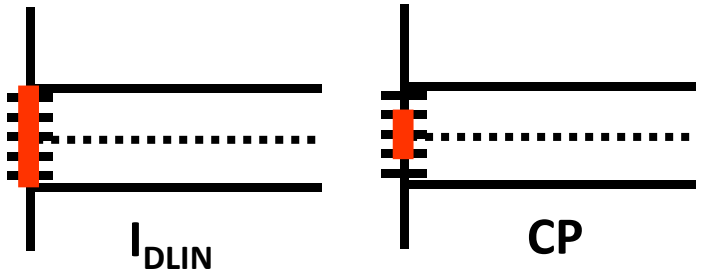
Comparison of CP and OTF-I_{DLIN} (t_0=1ms)

As measured difference ~ 10X → NBTI not due to trap generation?

Final difference within ~ 20%

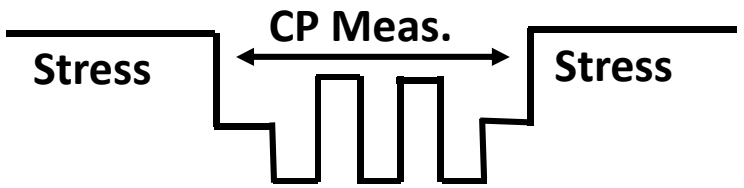


Band gap scan: Full for I_{DLIN}, partial near midgap for CP



Correct for band gap difference

Inherent recovery for CP

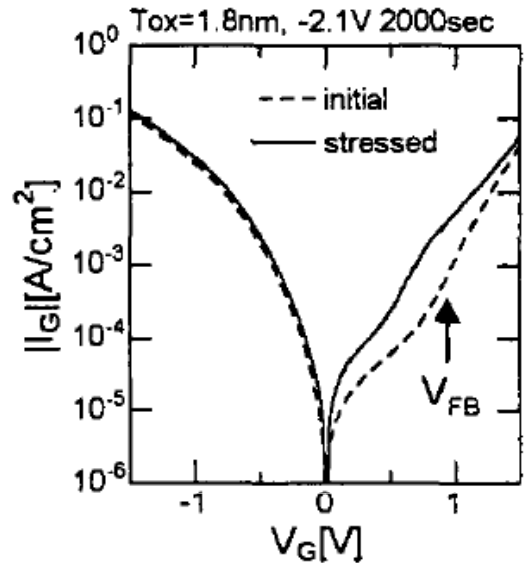


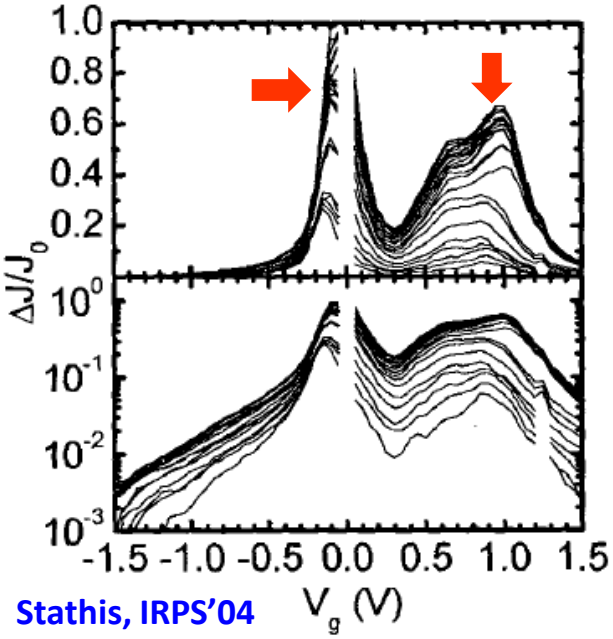
Correct for recovery

Mahapatra, IRPS'07

Low Voltage (LV) SILC

Kimizuka, VLSI 00





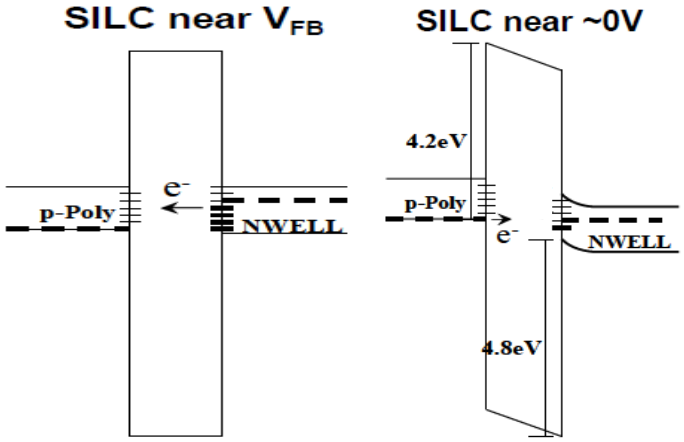
Stathis, IRPS'04

Increase in gate leakage current after stress

Two peaks evolve with stress time at V_G~V_{FB} (1V) and V_G ~ 0V

SILC (~V_{FB}) due to electron tunneling from Si/SiO_2 to SiO_2/poly-Si interface traps

SILC (~0V) due to VB electron tunneling from poly-Si to Si/SiO_2 interface traps

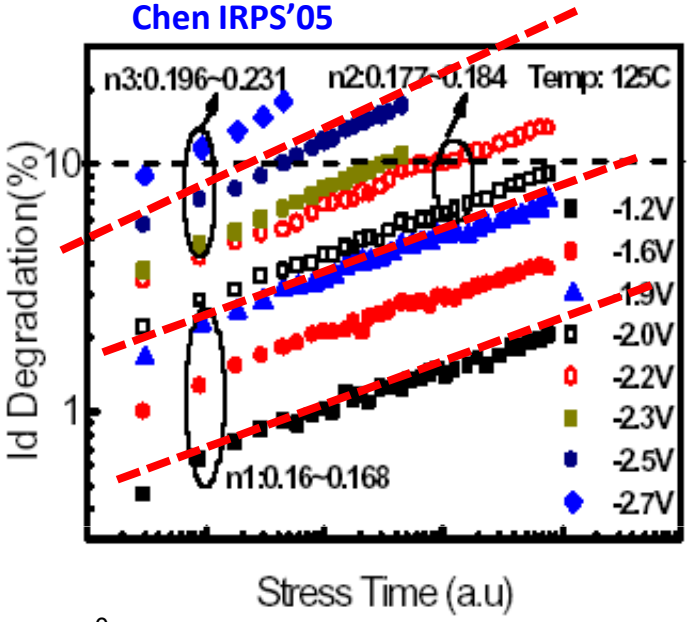


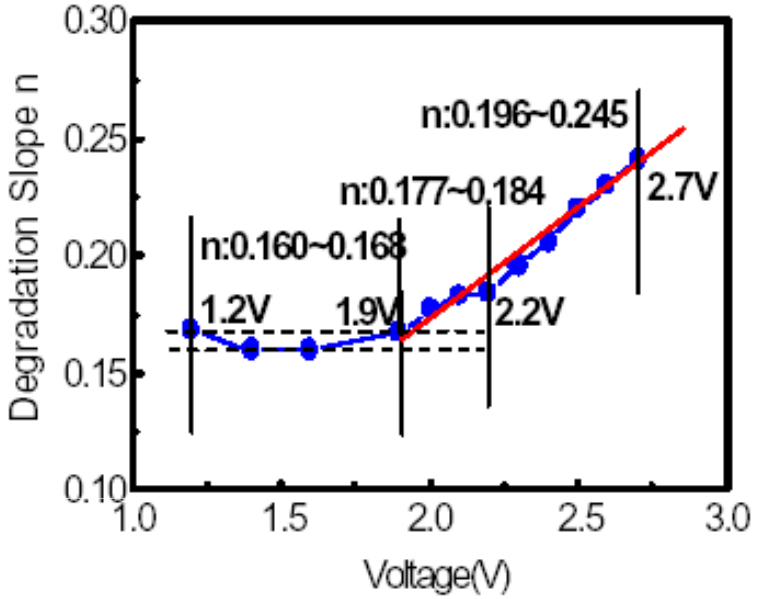
LVSILC increase ~ Interface trap generation

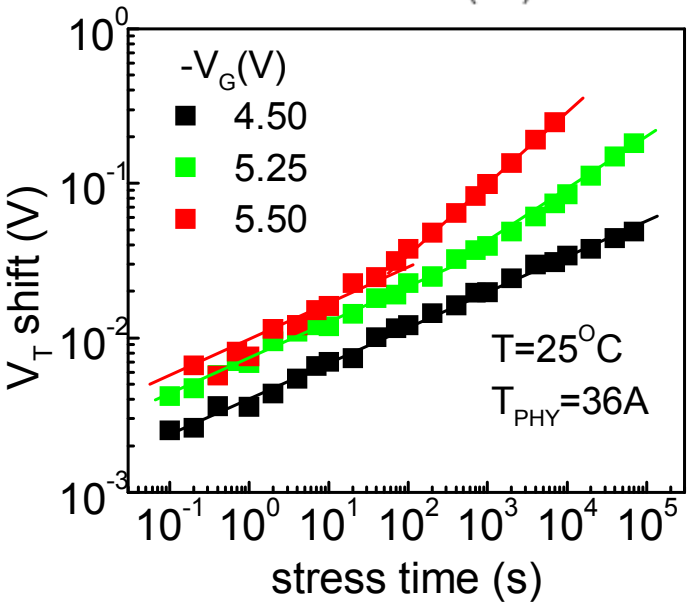
Krishnan, IEDM'05

Anomalous NBTI Degradation?

Chen IRPS'05







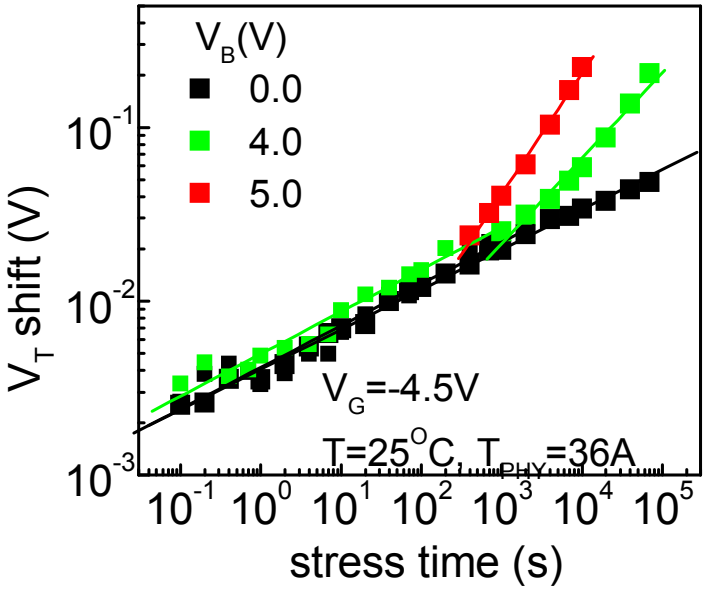
Identical time exponent (n) at different (lower) stress V_G – "normal NBTI"

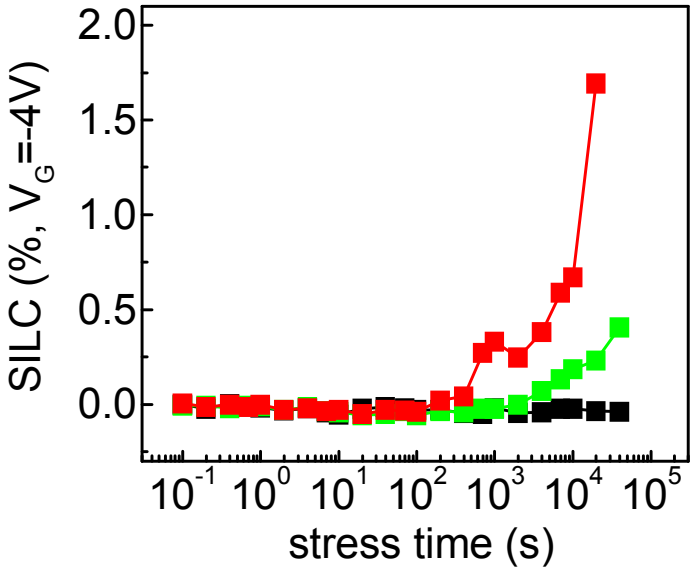
Increase in n at higher stress V_G – contribution from additional physical process?

Similar effect seen in thicker oxide

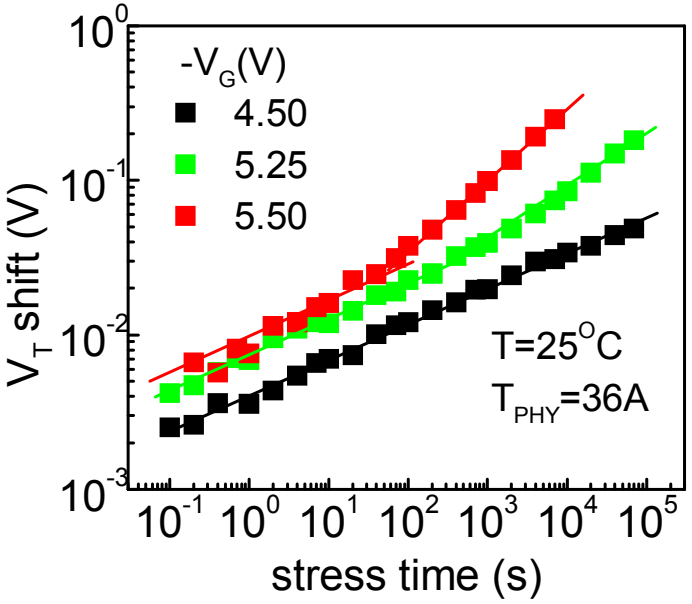
Mahapatra, IEDM'02

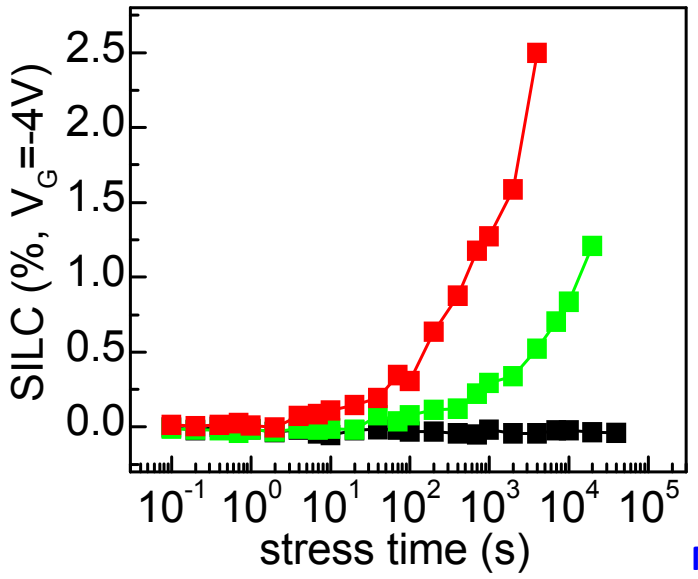
Anomalous NBTI – Bulk Trap Generation





Increase in "n" also seen for high stress V_B





Higher n coincides with SILC (~generation of bulk oxide traps)

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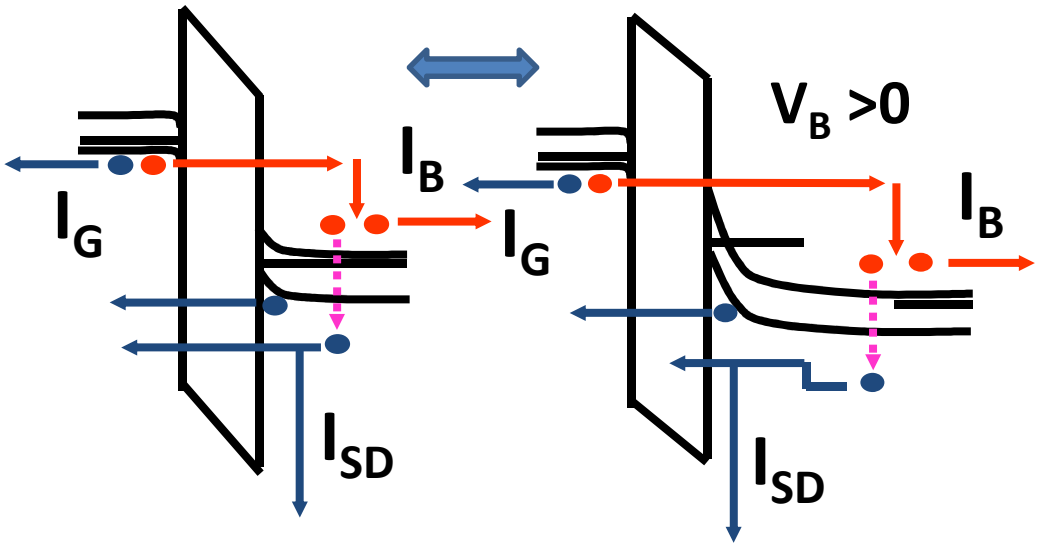
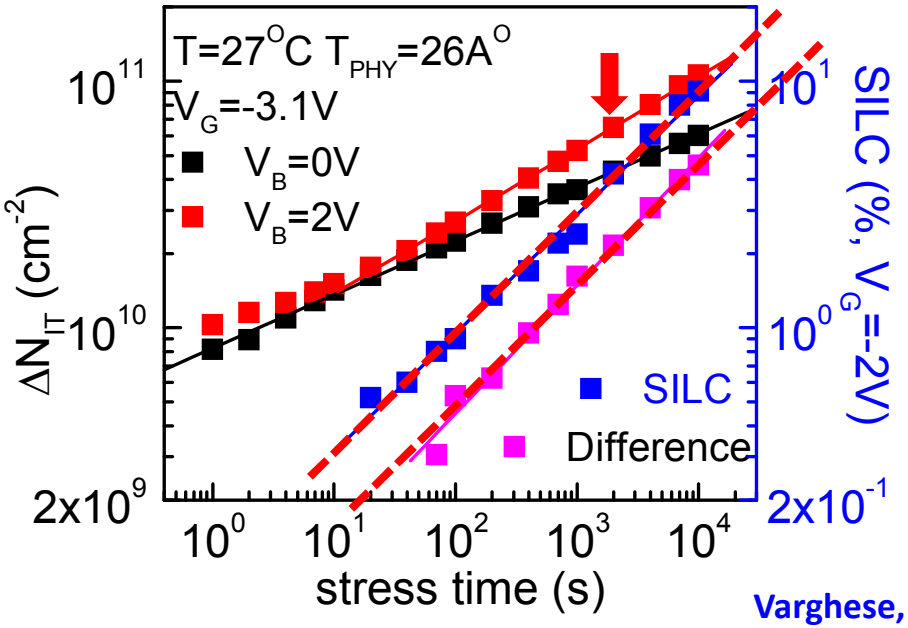
Hot Hole Induced Generation of Bulk Traps



HH generation at higher V_G reproduced by V_B>0 at lower V_G

Increased n at V_B>0, presence of SILC, similar degradation of SILC and enhanced degradation

No recovery of enhanced degradation for V_B>0 stress



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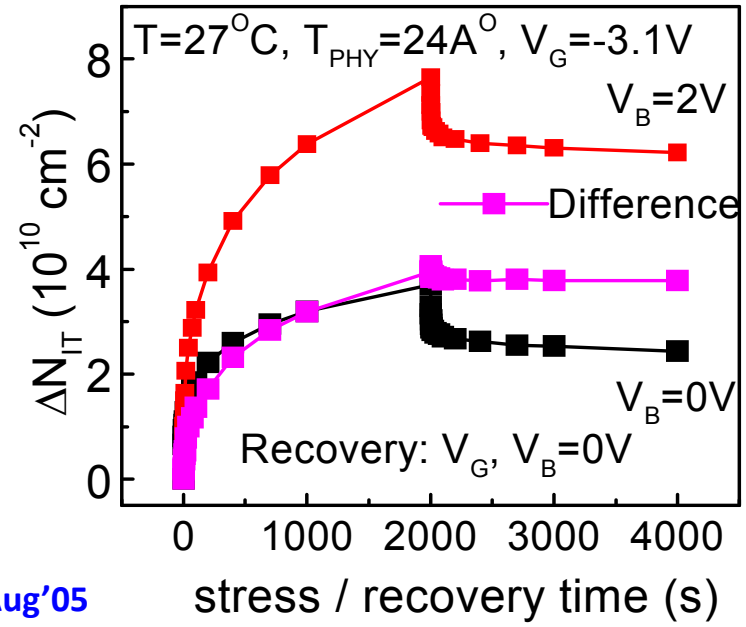

Summary

NBTI: Generation of interface traps, charging of pre-existing and generated bulk traps

Differently processed devices show difference in pre-existing bulk traps (Flicker noise on pre-stressed devices)

Interface / near interface and bulk trap generation signatures shown by multiple measurements

- **Evidence of interface / near interface trap generation from DCIV, high frequency charge pumping, LVSILC**
- **Evidence of bulk trap generation from HVSILC**

Several important factors need to be carefully considered if attempts are made to compare multiple measurements

Outline

Introduction, Basic NBTI signatures

Fast / Ultra-fast drain current degradation measurement

Estimation of pre-existing and generated defects

Transistor process / material dependence

Role of Nitrogen – Study by Ultrafast measurement

Go to Part – II

Predictive modeling

Conclusions / outlook