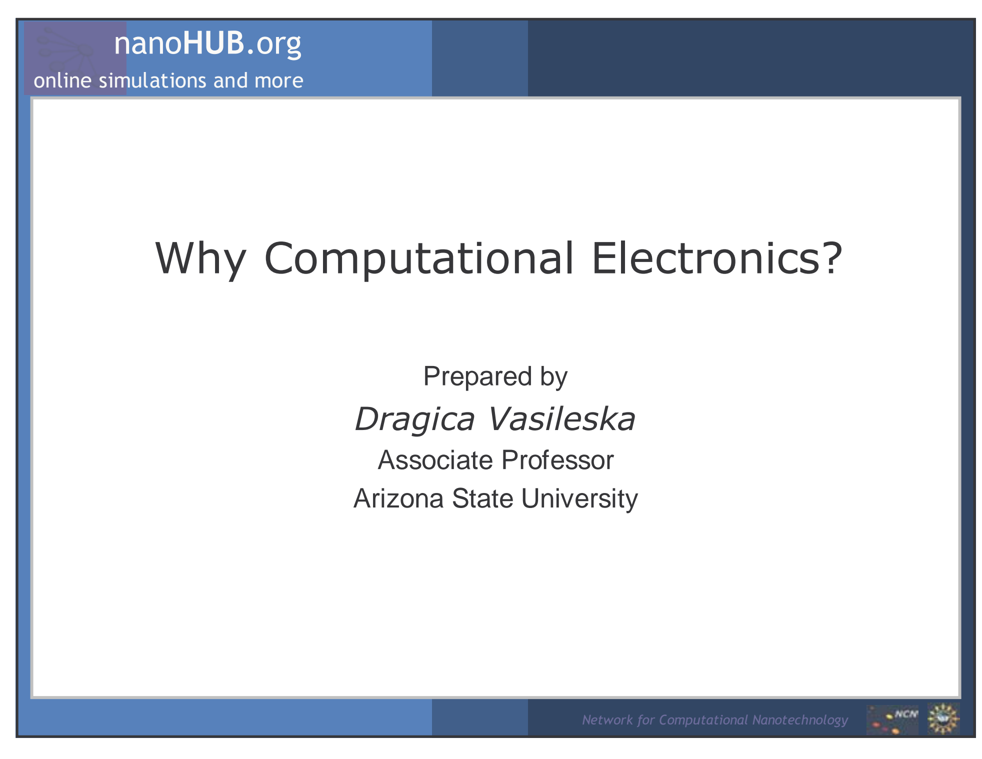
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Why Computational Electronics?
Prepared by
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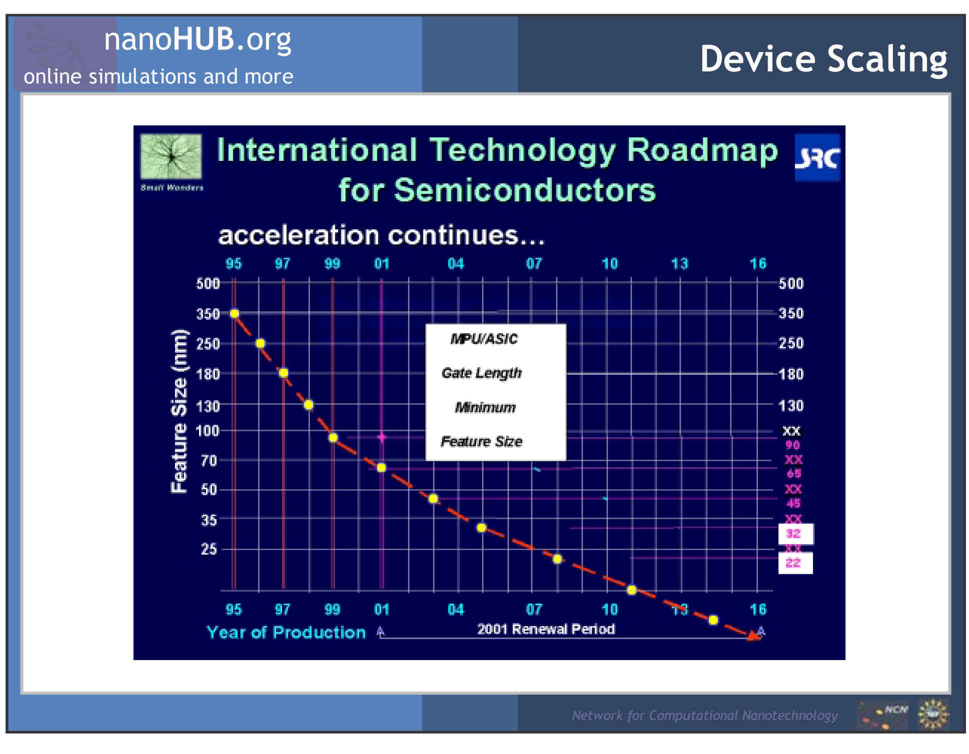
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Device Scaling
International Technology Roadmap for Semiconductors
acceleration continues...
Feature Size (nm)
MPU/ASIC
Gate Length
Minimum
Feature Size
Year of Production
2001 Renewal Period
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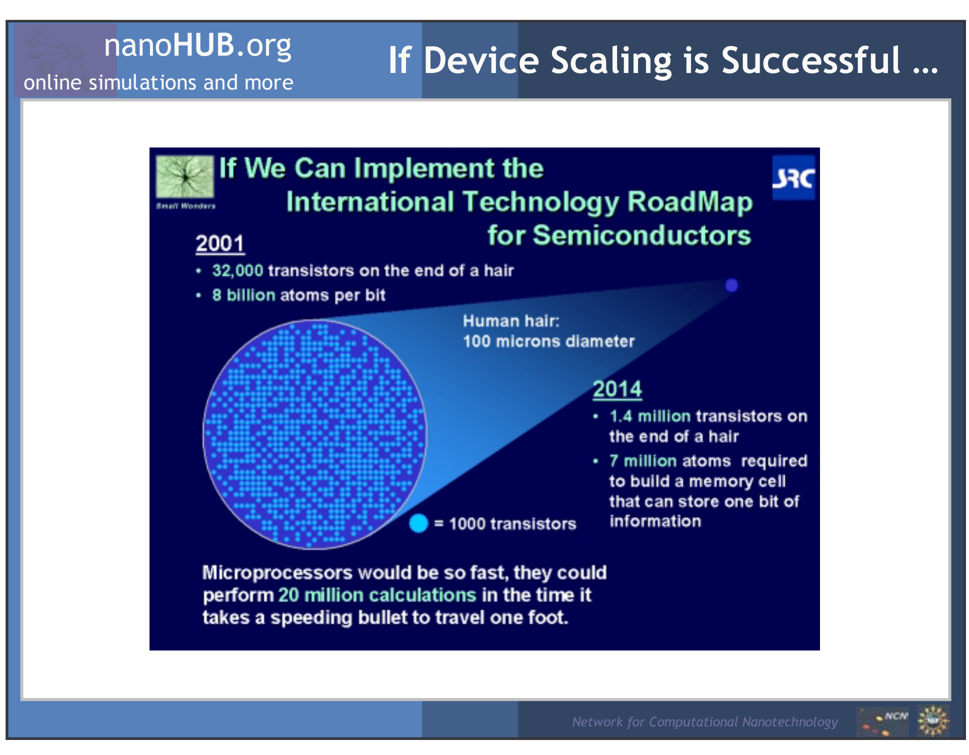
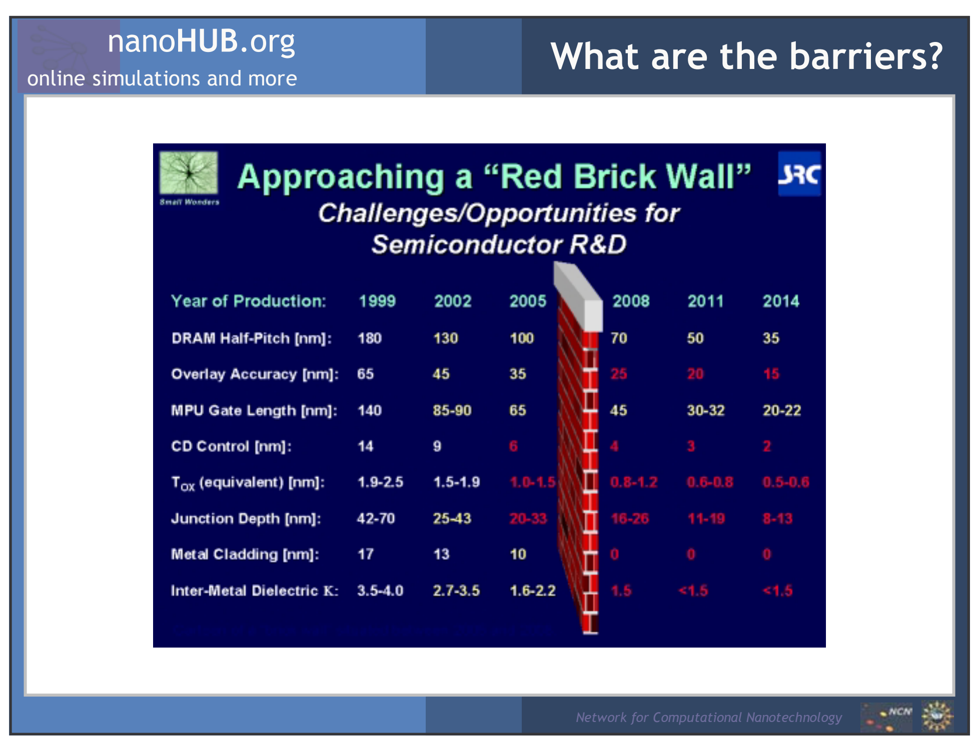
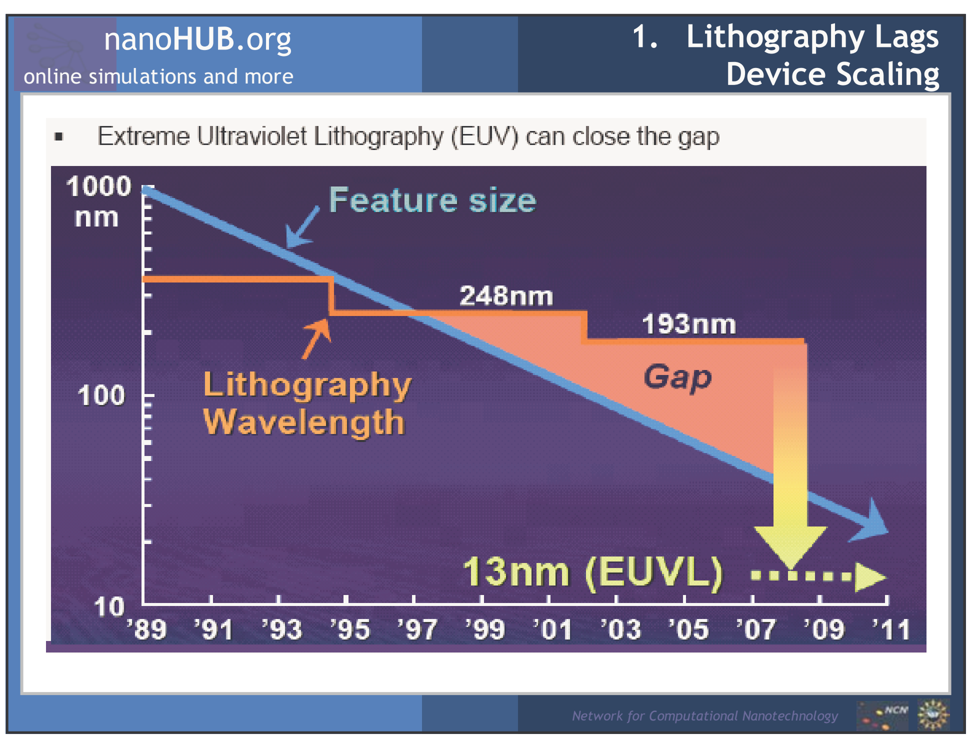




Year of Production:	1999	2002	2005	2008	2011	2014
DRAM Half-Pitch [nm]:	180	130	100	70	50	35
Overlay Accuracy [nm]:	65	45	35	25	20	15
MPU Gate Length [nm]:	140	85-90	65	45	30-32	20-22
CD Control [nm]:	14	9	6	4	3	2
T_{ox} (equivalent) [nm]:	1.9-2.5	1.5-1.9	1.0-1.5	0.8-1.2	0.6-0.8	0.5-0.6
Junction Depth [nm]:	42-70	25-43	20-33	16-26	11-19	8-13
Metal Cladding [nm]:	17	13	10	0	0	0
Inter-Metal Dielectric K:	3.5-4.0	2.7-3.5	1.6-2.2	1.5	<1.5	<1.5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1. Lithography Lags Device Scaling
Extreme Ultraviolet Lithography (EUV) can close the gap
1000 nm
Feature size
248nm
193nm
Gap
100
Lithography Wavelength
13nm (EUVL)
10
'89 '91 '93 '95 '97 '99 '01 '03 '05 '07 '09 '11
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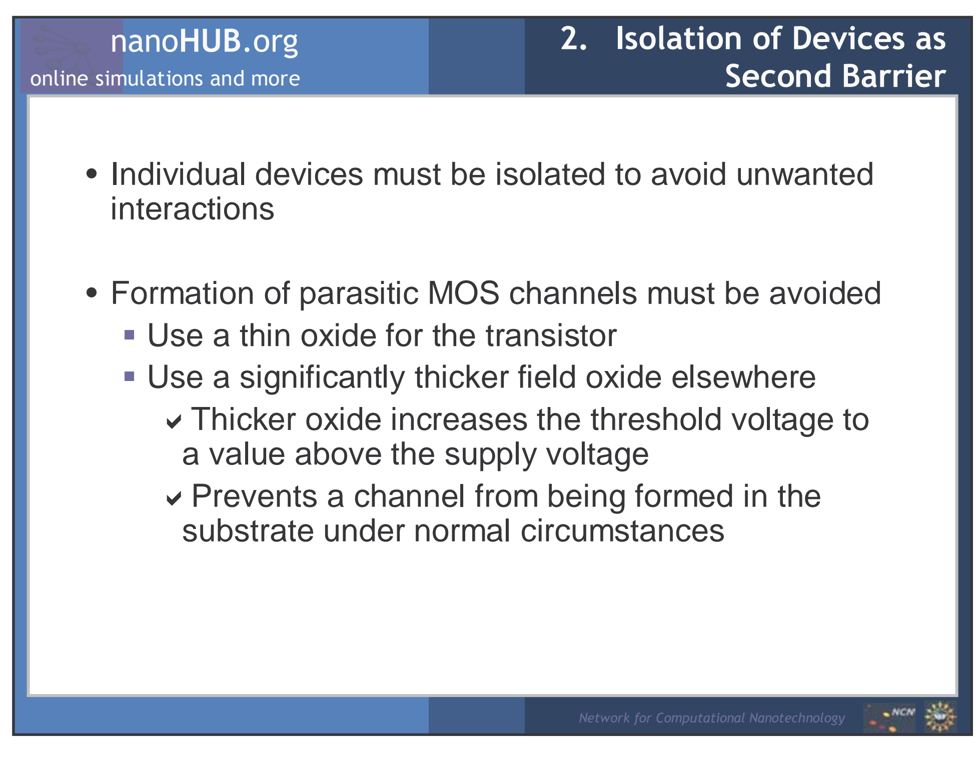
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2. Isolation of Devices as Second Barrier
Individual devices must be isolated to avoid unwanted interactions
Formation of parasitic MOS channels must be avoided
Use a thin oxide for the transistor
Use a significantly thicker field oxide elsewhere
Thicker oxide increases the threshold voltage to a value above the supply voltage
Prevents a channel from being formed in the substrate under normal circumstances
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Alternatives to Classical MOSFETs

NON-CLASSICAL CMOS DEVICES					
Device	***Ultrathin Body SOI***	***Band-Engineered Transistor***	***Vertical Transistor***	***FinFET***	***Double-Gate Transistor***
Concept	Fully-depleted SOI	SiGe or Strained Si Channel; bulk Si or SOI	Double-gate or surround-gate structure		
Application/Driver	Higher performance, higher transistor density, lower power dissipation				
Advantages	Improved subthreshold slope; V_T controllability	Higher drive current; compatible with bulk Si and SOI	Higher drive current; lithography independent gate length	Higher drive current; Improved subthreshold slope; improved short-channel effect (SCE); stacked NAND	
Scaling Issues	Si film thickness, gate stack; worse SCE than bulk CMOS	High mobility film thickness (SOI); gate stack; integratability	Si film thickness; gate stack; integratability; process complexity; accurate TCAD including quantum-mechanical (QM) effects		Gate alignment; Si film thickness; gate stack; integratability; process complexity; accurate TCAD
Design Challenges	Device characterization; compact model and parameter extraction	Device characterization	Device characterization; PD versus FD; compact model and parameter extraction; applicability to mixed signal applications		

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The Emergence of Computational Electronics …

- As devices shrink into the nanometer scale, the trial and error approach is becoming more and more expensive
- As a result, the Computational Electronics have emerged as an important field in the device manufacturing process as it can offer:
  - The possibility to test hypothetical devices which has not yet been manufactured
  - Observation of phenomena that can not be measured on real devices

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What is Computational Electronics?

- Computational electronics is related to, but different from TCAD (technology for computer-aided design).
- The relationship between the various simulation design steps needed to achieve certain customer need is summarized on the figure.

Customer Need
Process Simulation
Device Simulation
Computational Electronics
Parameter Extraction
Circuit Level Simulation
no
yes

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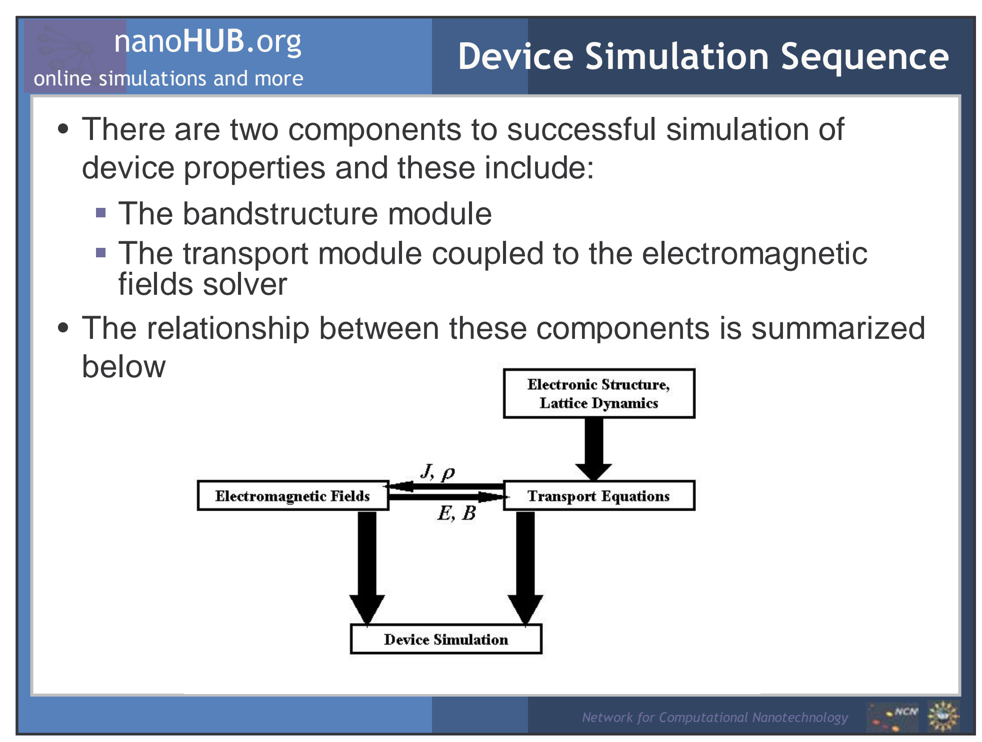

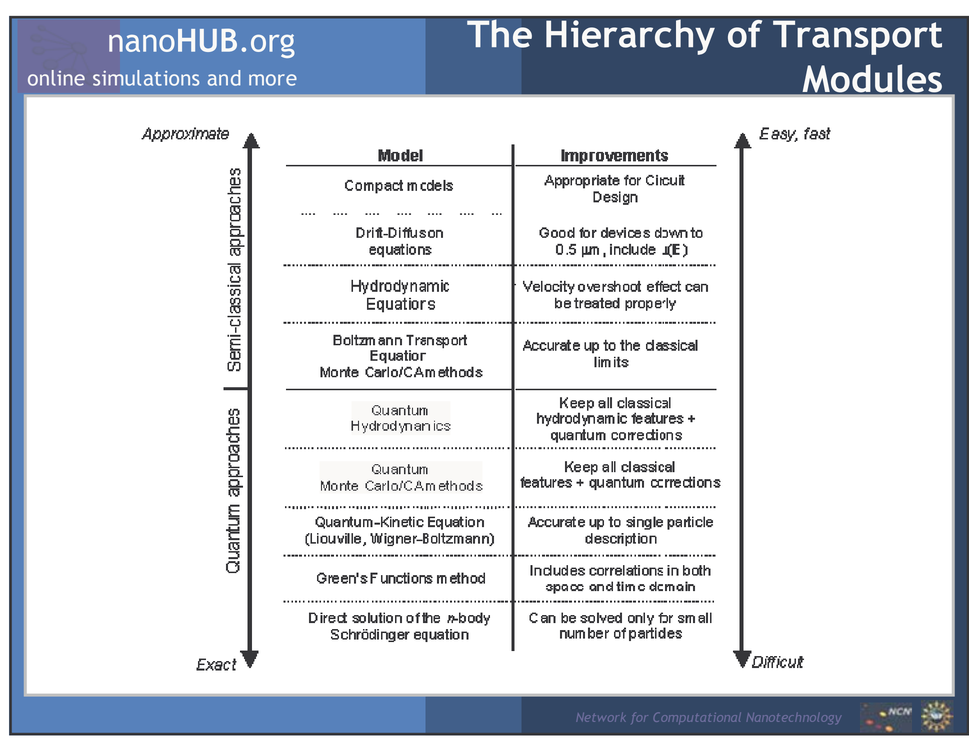
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The Hierarchy of Transport Modules
Approximate
Exact
Semi-classical approaches
Quantum approaches
Easy, fast
Difficult
Model
Improvements
Compact models
Appropriate for Circuit Design
Drift-Diffusion equations
Good for devices down to 0.5 µm, include µ(E)
Hydrodynamic Equations
Velocity overshoot effect can be treated properly
Boltzmann Transport Equation
Monte Carlo/CA methods
Accurate up to the classical limits
Quantum Hydrodynamics
Keep all classical hydrodynamic features + quantum corrections
Quantum Monte Carlo/CA methods
Keep all classical features + quantum corrections
Quantum-Kinetic Equation (Liouville, Wigner-Boltzmann)
Accurate up to single particle description
Green's Functions method
Includes correlations in both space and time domain
Direct solution of the n-body Schrödinger equation
Can be solved only for small number of particles
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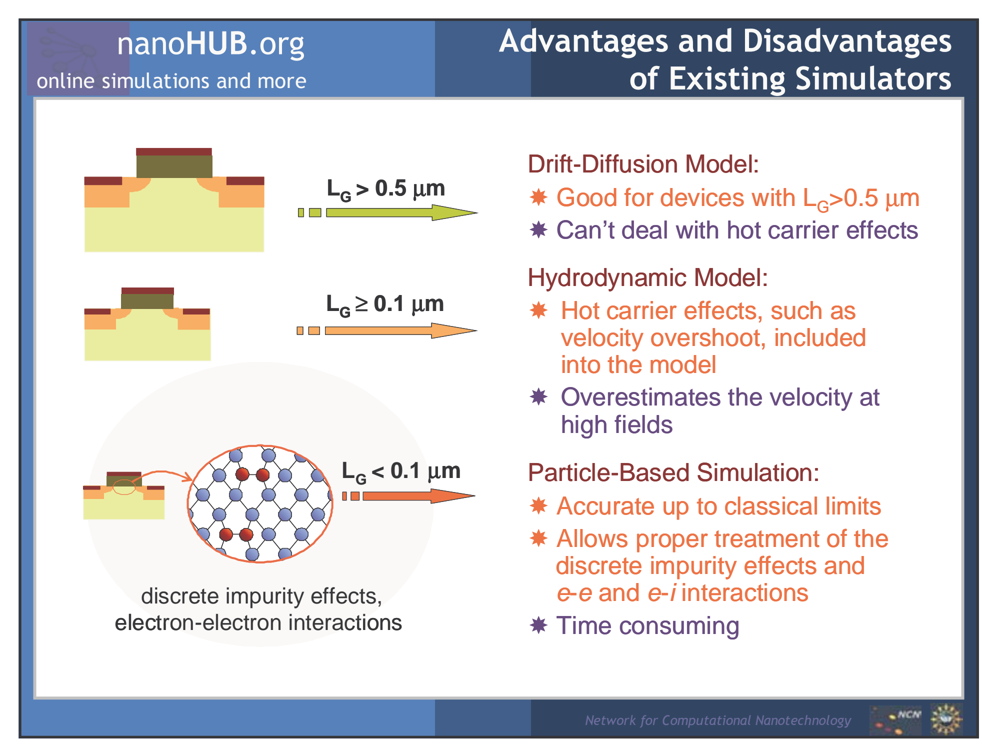
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Advantages and Disadvantages of Existing Simulators
LG > 0.5 µm
LG ≥ 0.1 µm
LG < 0.1 µm
discrete impurity effects,
electron-electron interactions
Drift-Diffusion Model:
Good for devices with LG>0.5 µm
Can't deal with hot carrier effects
Hydrodynamic Model:
Hot carrier effects, such as velocity overshoot, included into the model
Overestimates the velocity at high fields
Particle-Based Simulation:
Accurate up to classical limits
Allows proper treatment of the discrete impurity effects and e-e and e-i interactions
Time consuming
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The Emergence of the Need for Quantum Transport Simulators

	$L << l_{e-ph}$			$L \sim l_{e-ph}$	$L >> l_{e-ph}$
	$L < \lambda$	$L < l_{e-e}$	$L >> l_{e-e}$		
Transport Regime	Quantum	Ballistic	Fluid	Fluid	Diffusive
Scattering	Rare	Rare	e-e (Many), e-ph (Few)		Many
Model:					
Drift-Diffusion					
Hydrodynamic	Quantum Hydrodynamic				
Monte Carlo					
Schrodinger/Green's Functions	Wave				
Applications	Nanowires, Superlattices	Ballistic Transistor	Current IC's	Current IC's	Older IC's

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