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ECE695: Reliability Physics of Nano-Transistors

Lecture 28: Circuit Implications of Dielectric Breakdown

Based on a IRPS Tutorial by
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(Edited by Muhammad A. Alam)

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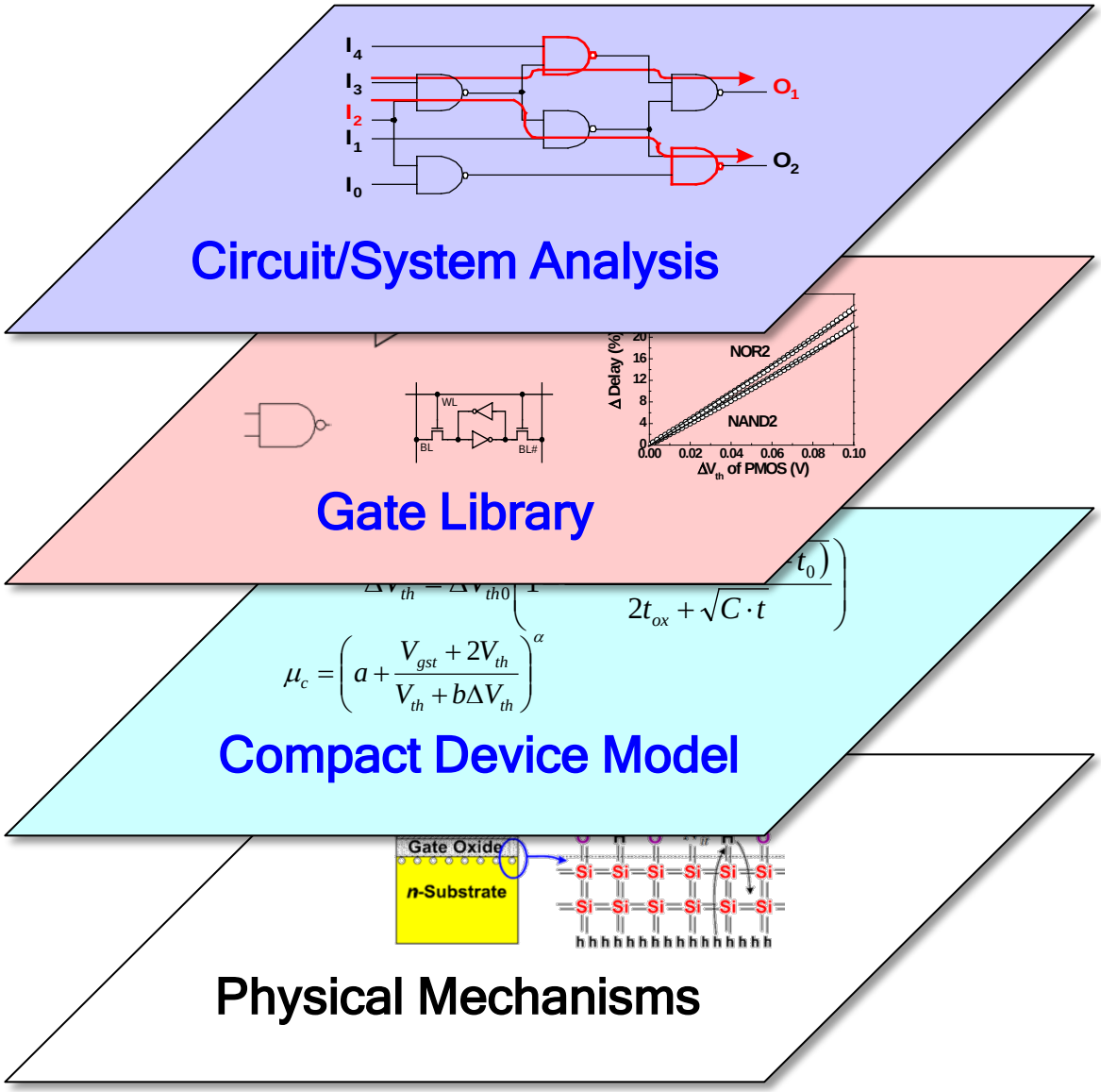
Outline

- *Part 1* - Understanding Post-BD FET behavior
  1. BD position determination
  2. Hard and Soft BD in FETs
  3. Distinguishing leakage and intrinsic FET parameters shifts

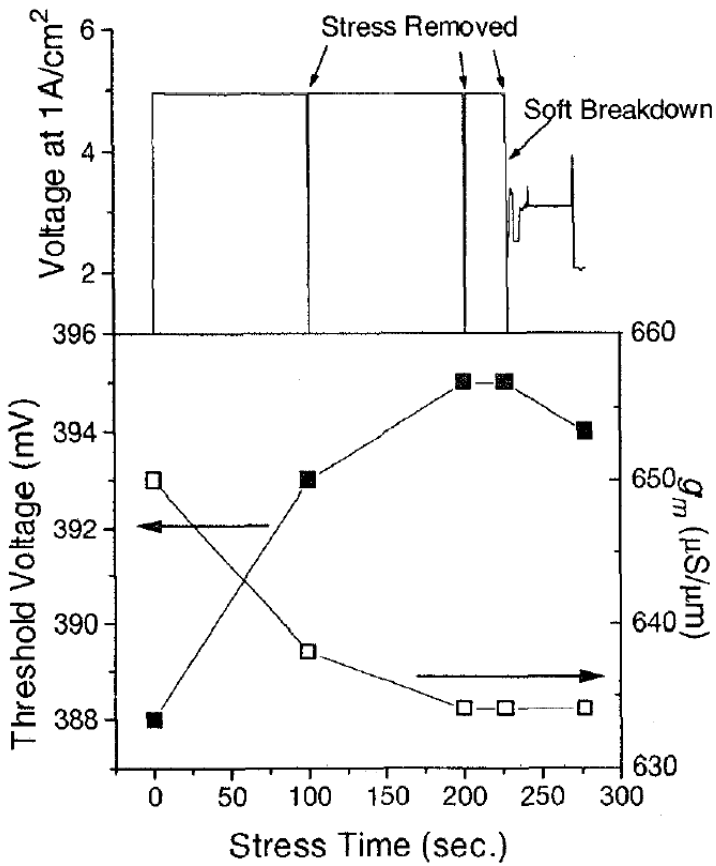
- *Part 2* - Impact of breakdown on digital circuit operation
  1. BD in ring oscillator
  2. BD in SRAM cell
  3. Timing, BD into soft node

Hierarchical Approach



Courtesy:
K. Cao

Ultra-thin gate dielectrics: they break down, but do they fail? (Weir et al., 1997)



- No significant degradation of g_m or V_T is observed after soft breakdown of 2.5nm dielectrics.

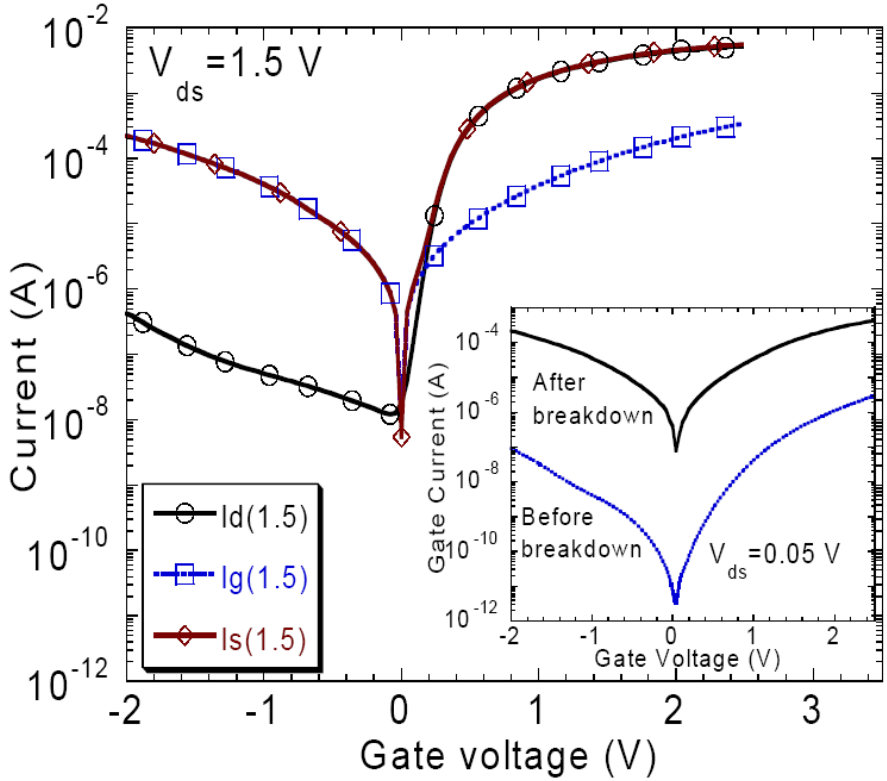
Since the only impact of soft breakdown in ultra-thin oxides is an increase in gate noise, soft breakdown should not prevent devices from functioning in many applications. This suggests the possibility of a low-voltage technology which does not have gate-oxide breakdown as a failure mode.

t_{ox}=0.5nm, A=2.5um^2

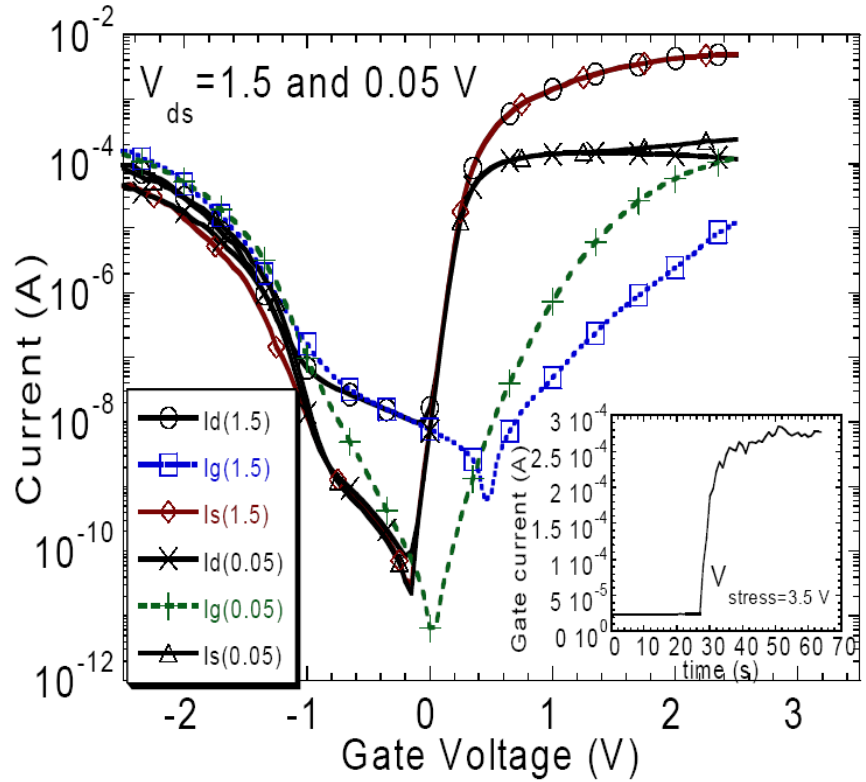
Weir et al., IEDM, p. 73 (1997)

Post-BD characteristics understood through BD position

Gate-Source SBD



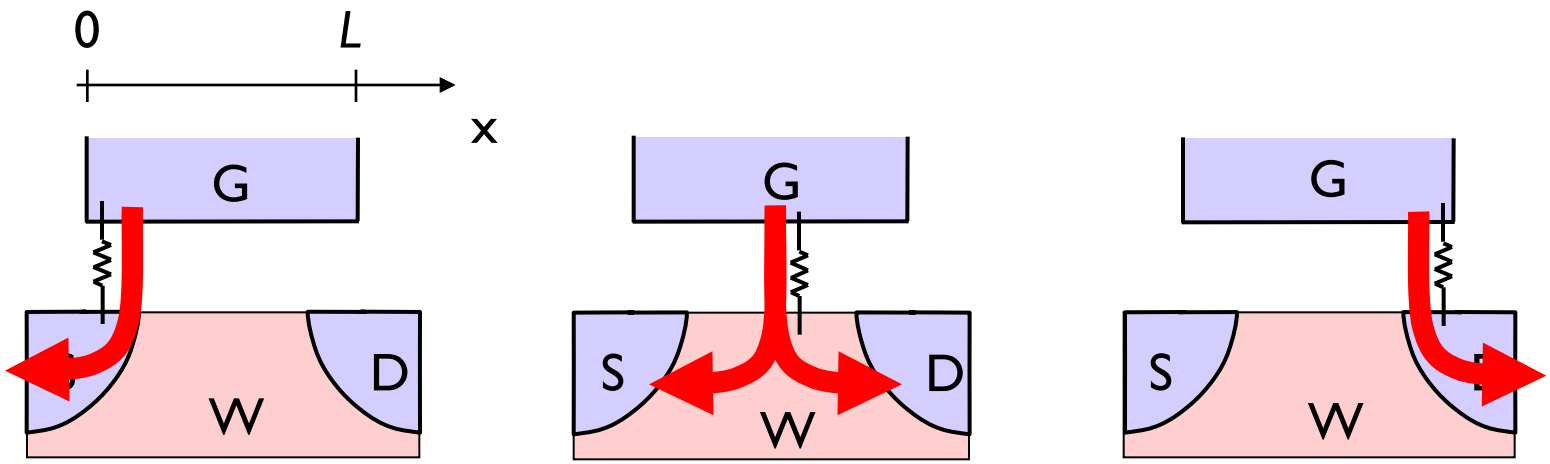
Center SBD



Yang et al., IEDM, p.453 (1999)

Refined BD position determination

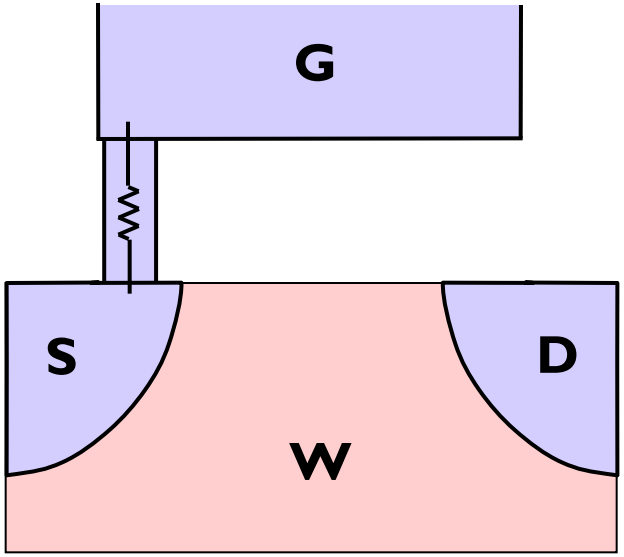
Define $$s \equiv \frac{I_D}{I_S + I_D} \quad @\ accumulation$$



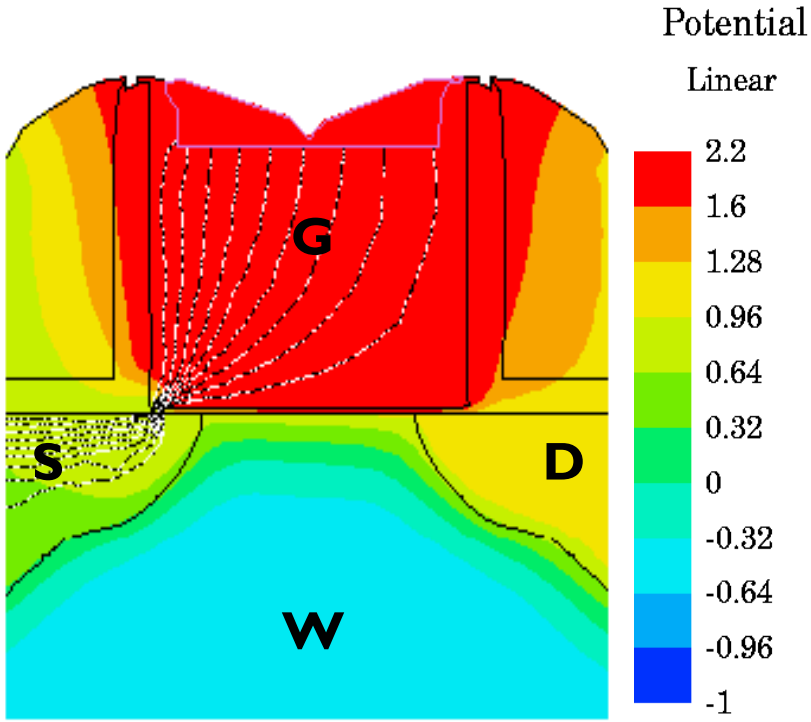
$$\frac{I_D}{I_S + I_D} = 0 \qquad 0 < \frac{I_D}{I_S + I_D} < 1 \qquad \frac{I_D}{I_S + I_D} = 1$$

Degraeve et al., IRPS, p. 360 (2001)

MEDICI modeling of post-breakdown currents



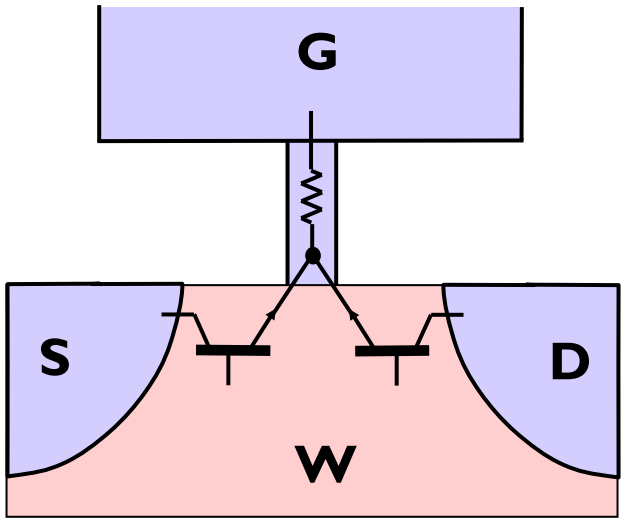
Hard breakdown path is modeled as a narrow inclusion of highly doped n-type silicon

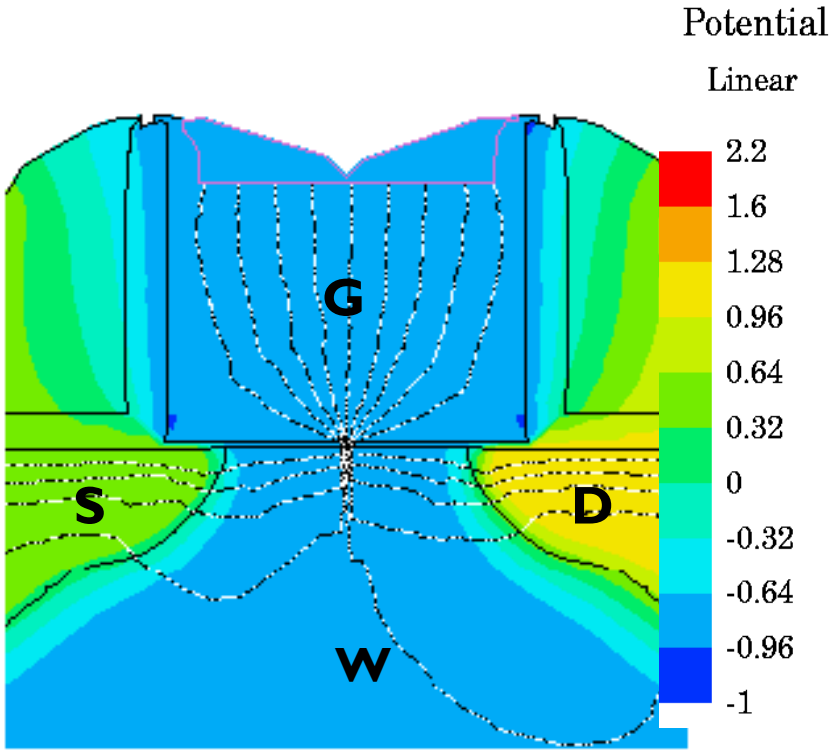


$V_G = 1.5V, \quad V_D = 0.5V$

Breakdown at the S/D extension: "pure" resistor
(+ hot carrier effects)

MEDICI modeling of post-BD nFET currents in accumulation





Bipolar effect @ V_G < 0V

BD-path = Emitter

Substrate = Base

S/D = Collector

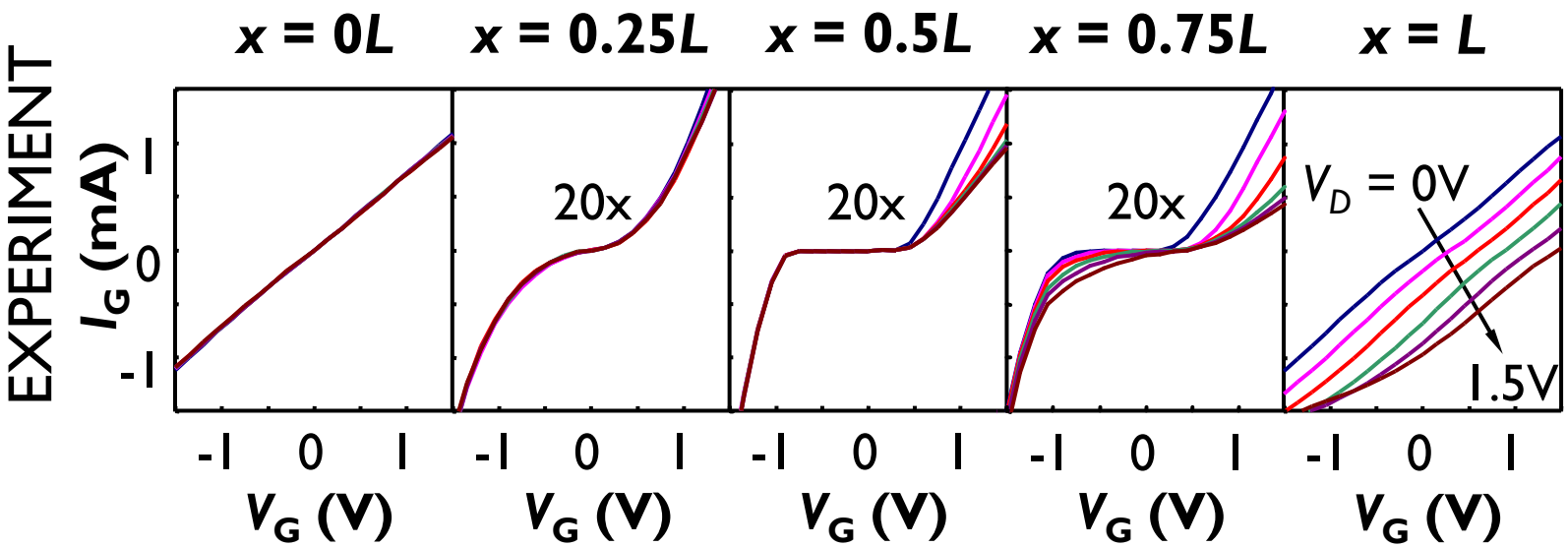
V_G=*1.5V*, V_D=*0.5V*

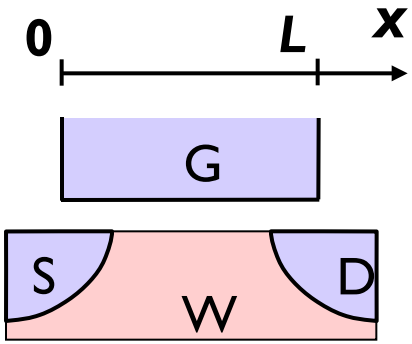
Gate-substrate breakdown + negative V_G ➡

BD-path acts as emitter of **2 bipolar transistors**

Kaczer *et al.*, Symp.VLSI, p. 121 (2001)

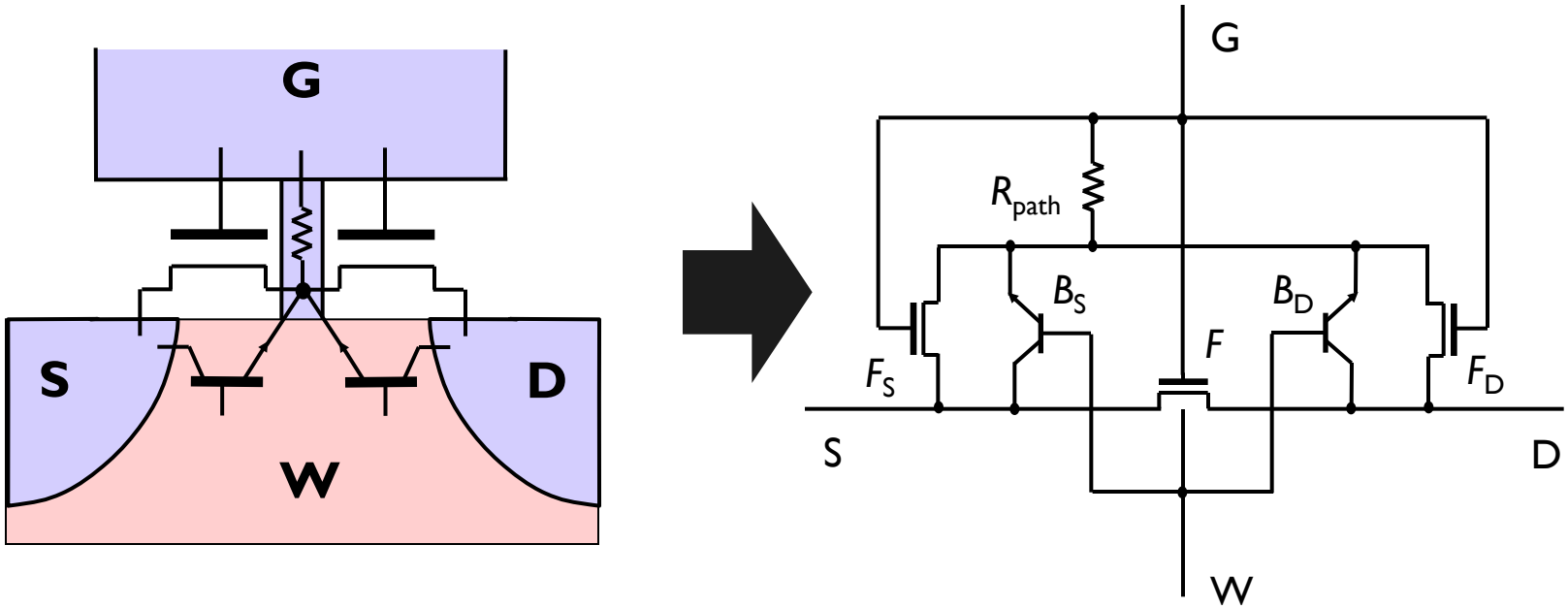
Post hard-breakdown characteristics depend strongly on breakdown position





*Kaczer et al., TED **49**, p. 507 (2002)*

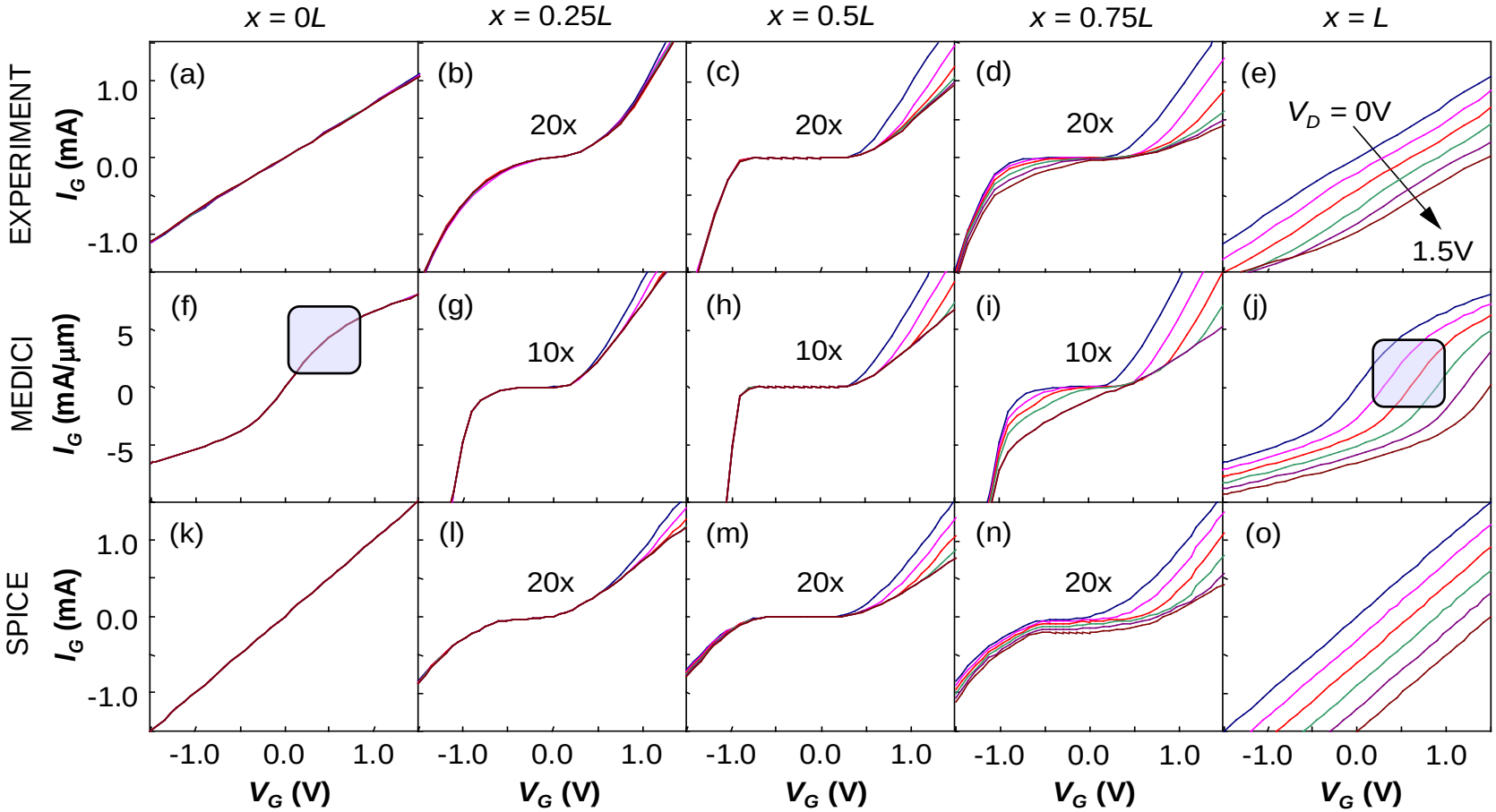
Equivalent electrical circuit for nFET after hard BD



F_S, F_D gate lengths, B_S, B_D base lengths a function of BD position

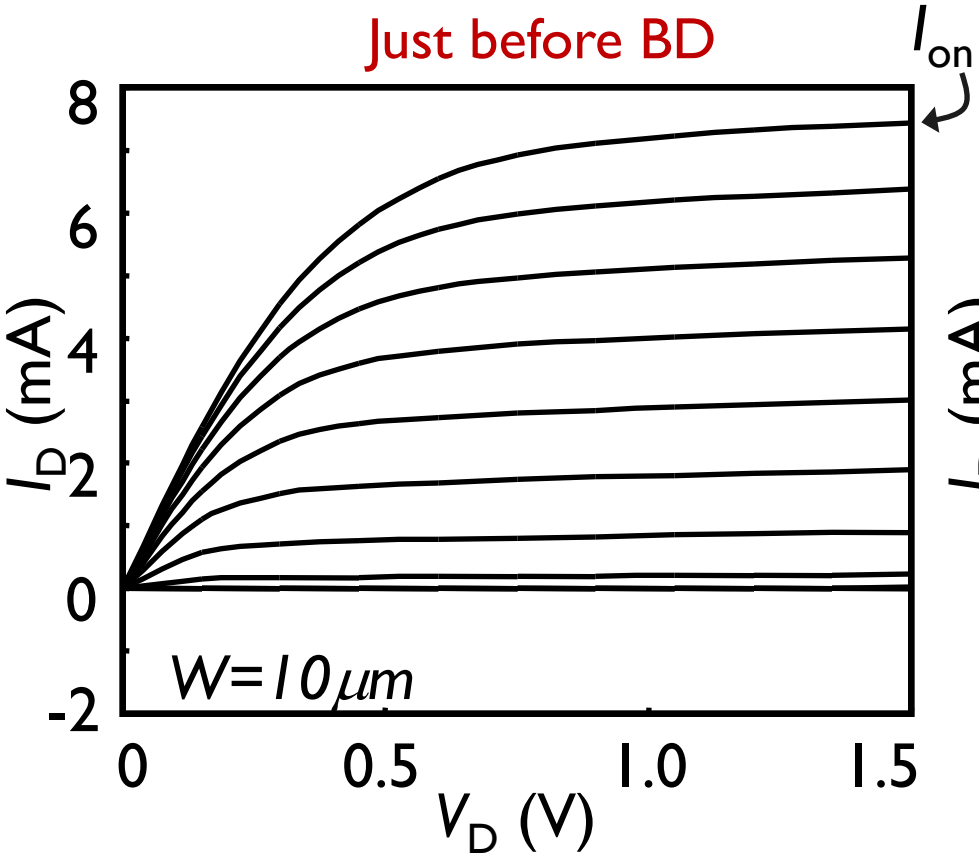
R_{path} independent of BD position

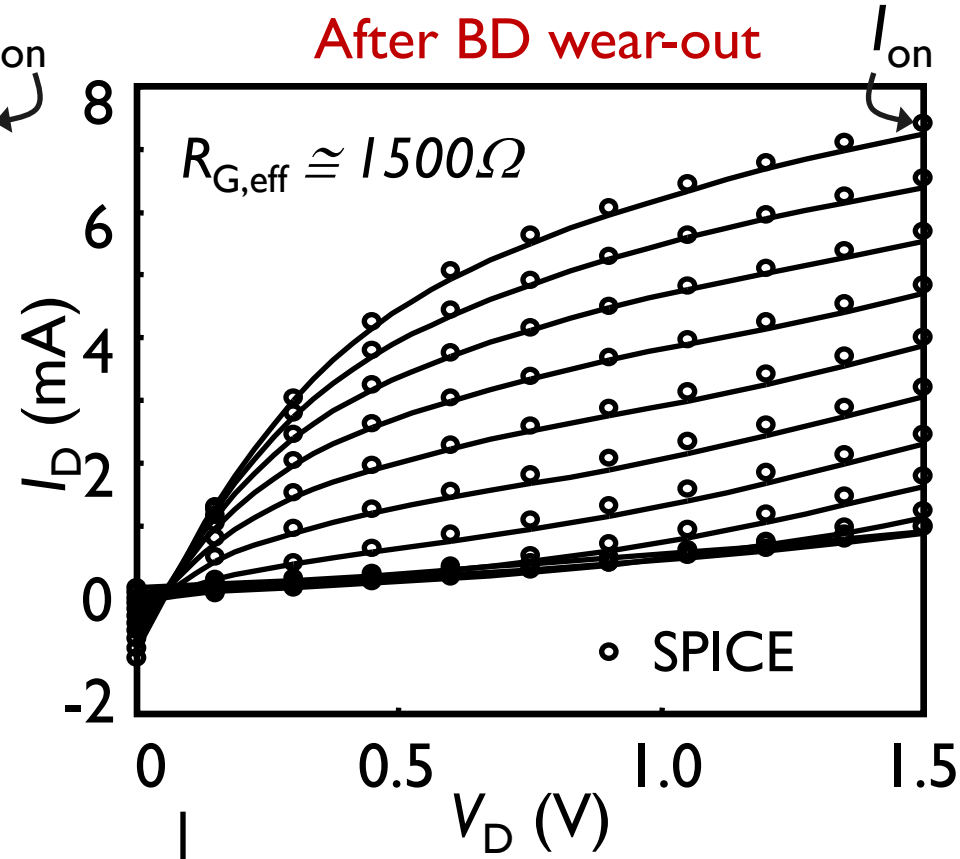
Post hard-breakdown gate currents

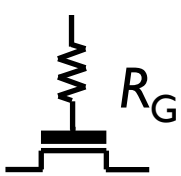


MEDICI and SPICE simulations explain gate current at all breakdown positions

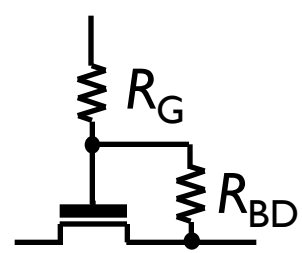
Hard BD appears to strongly influence wide nFET (purely due to gate leakage)







R_G poly line resistance

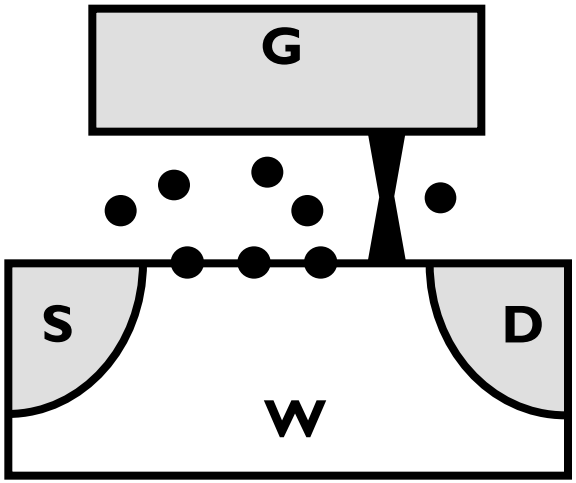


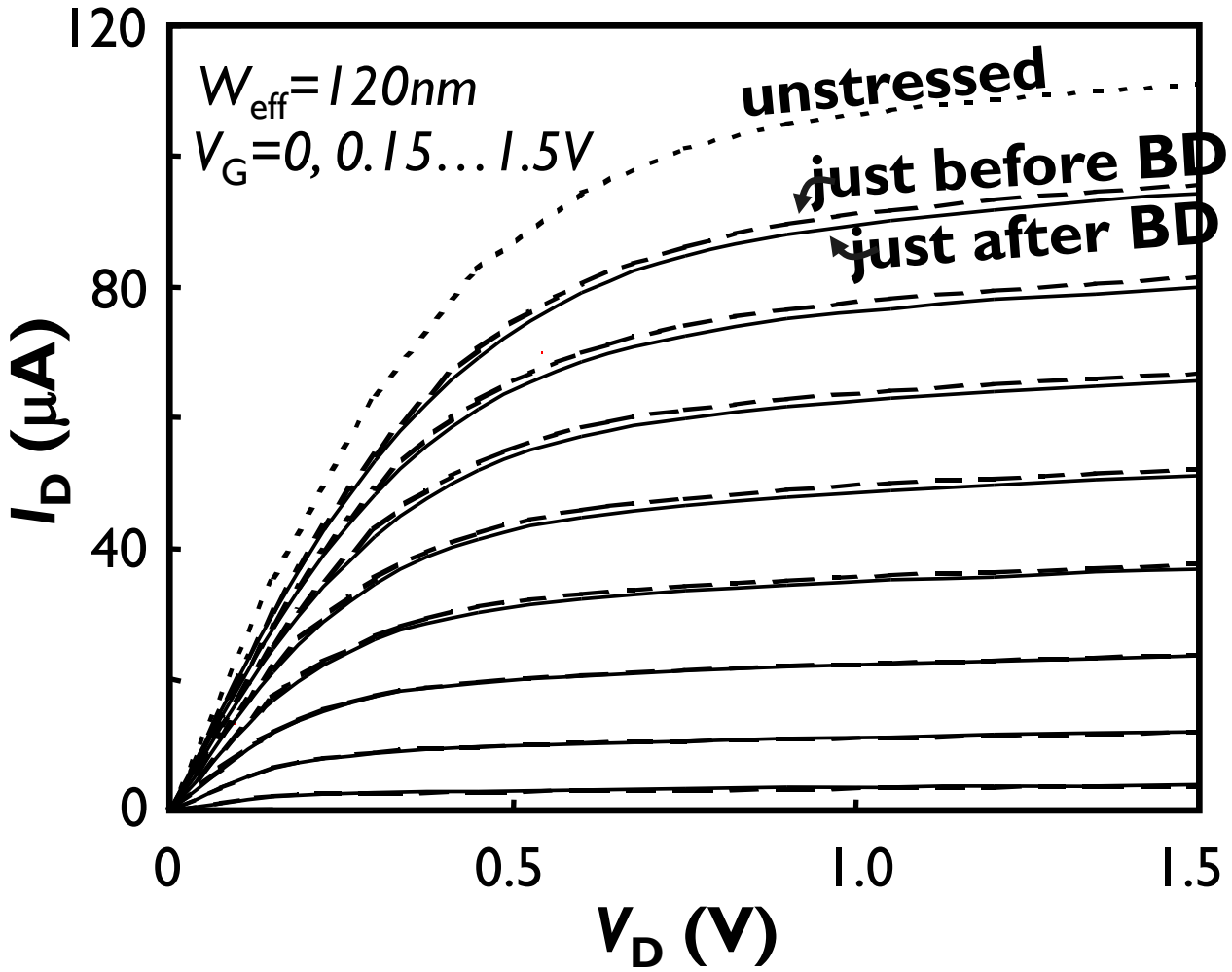
Post-BD char is explained by this equiv. circuit

Kaczer et al., IRPS, p. 79 (2004)

Note: I_{on} unaffected

No significant effect on FET characteristics at the moment of SBD!

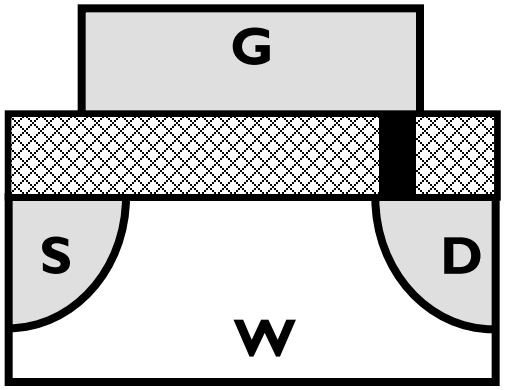




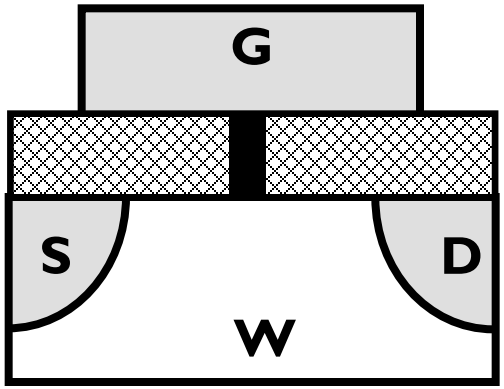
Kaczer et al., IRPS, p. 79 (2004)

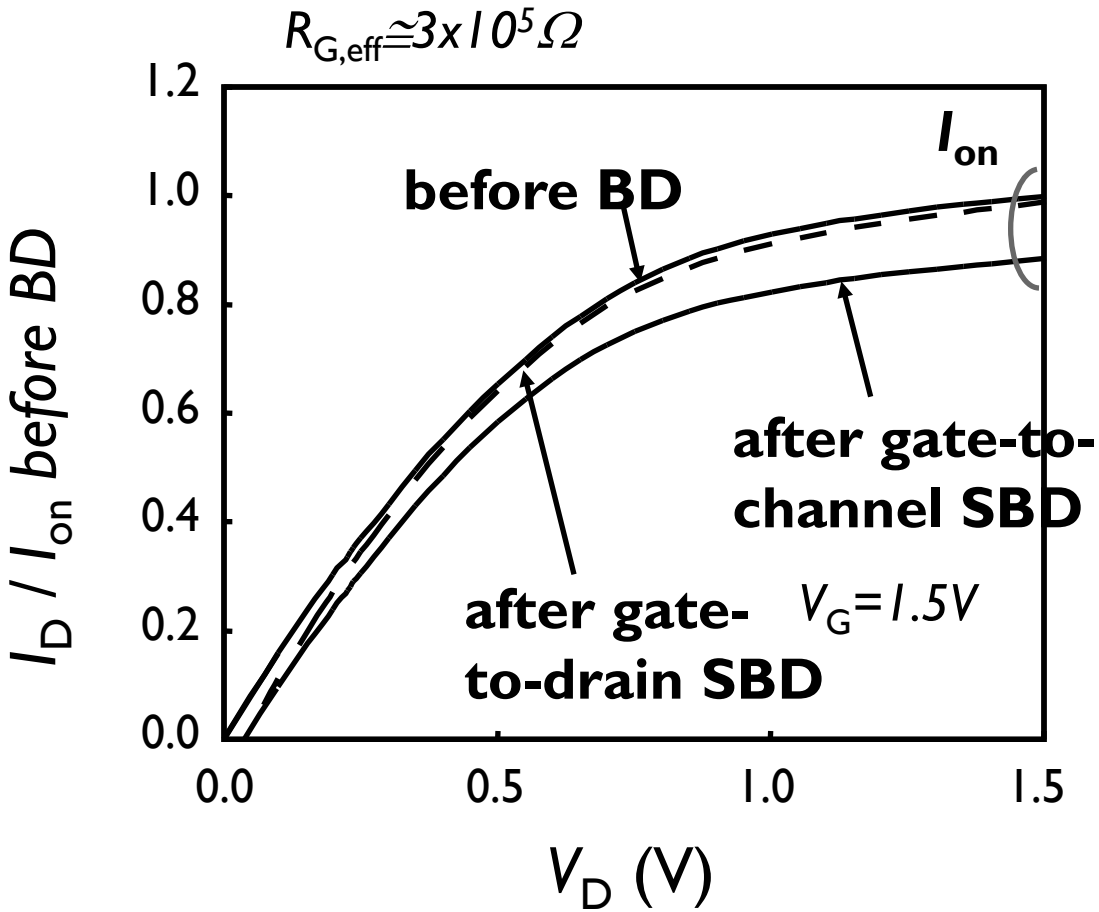
FET behavior affected by surrounding damage for gate-to-channel BD

Gate-to-drain SBD



Gate-to-channel SBD





- Negligible drop in I_{on} for gate-to-drain BD
- ~12% drop in I_{on} for gate-to-channel BD

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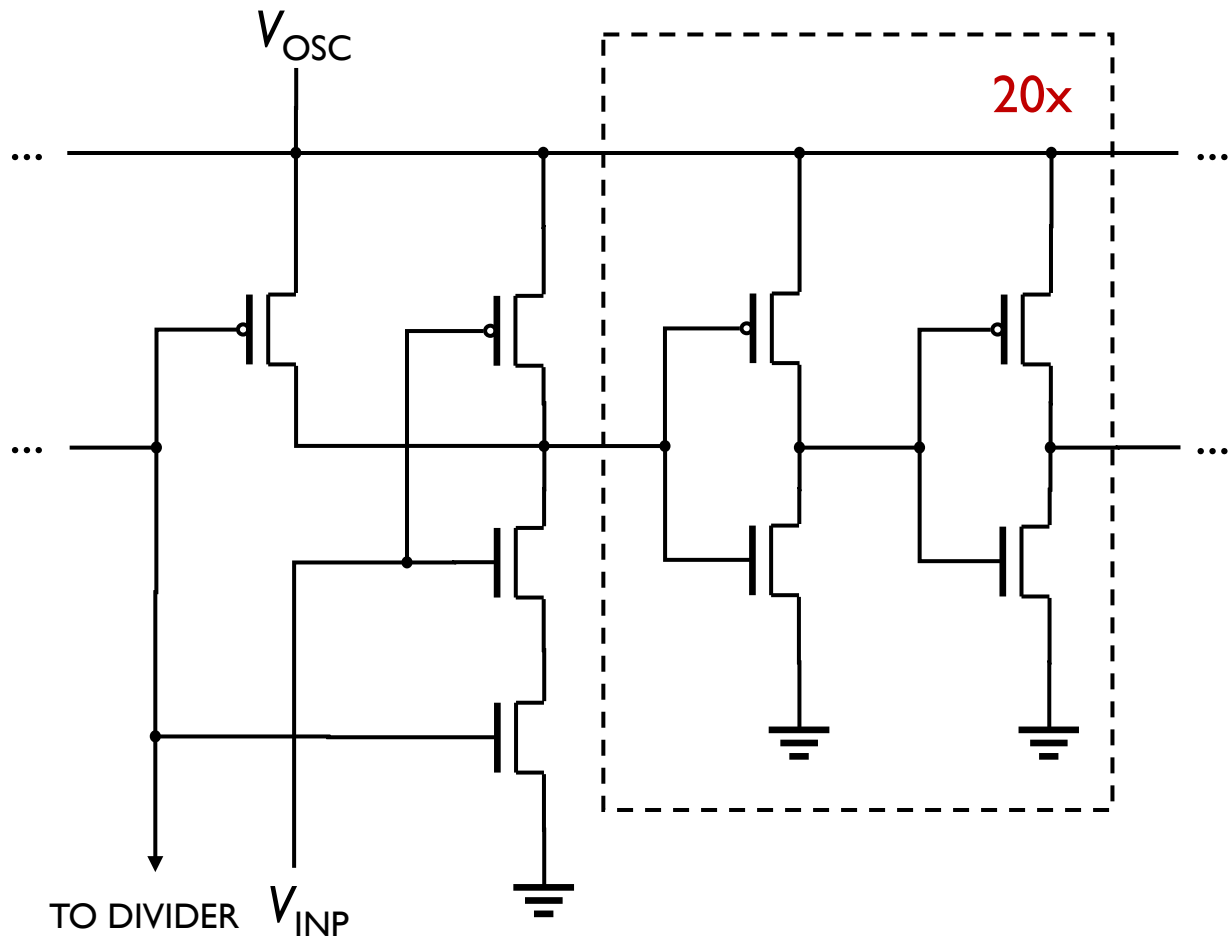
- ***Part 2* - Impact of breakdown on digital circuit operation**
  1. BD in ring oscillator
     - Advanced analysis of post-BD ring oscillator
  2. BD in SRAM cell
  3. Timing, BD into soft node

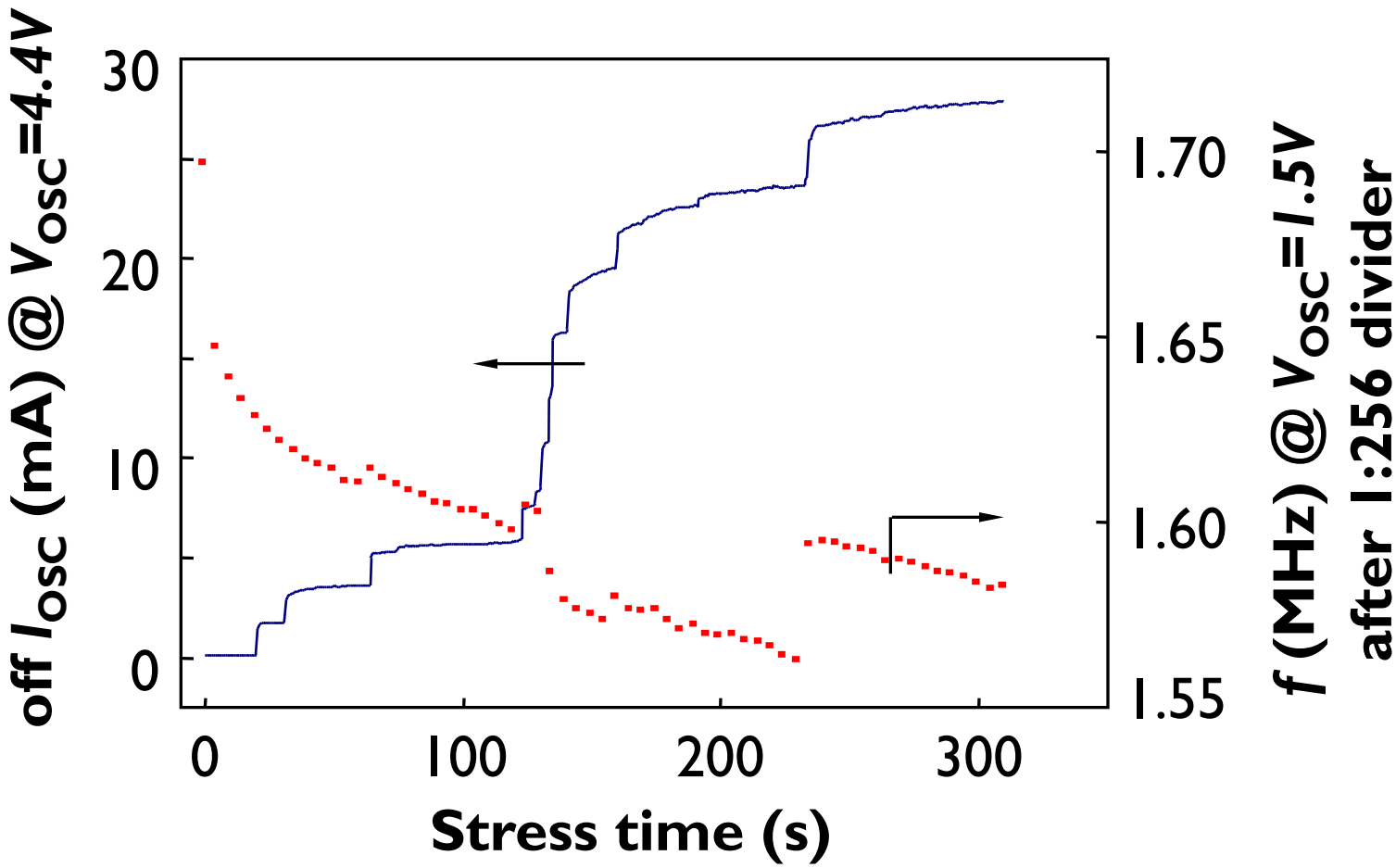
Ring oscillator : representative of CMOS circuits in both on and stand-by states



1 NAND + 40 inverters = 42 nFETs + 42 pFETs

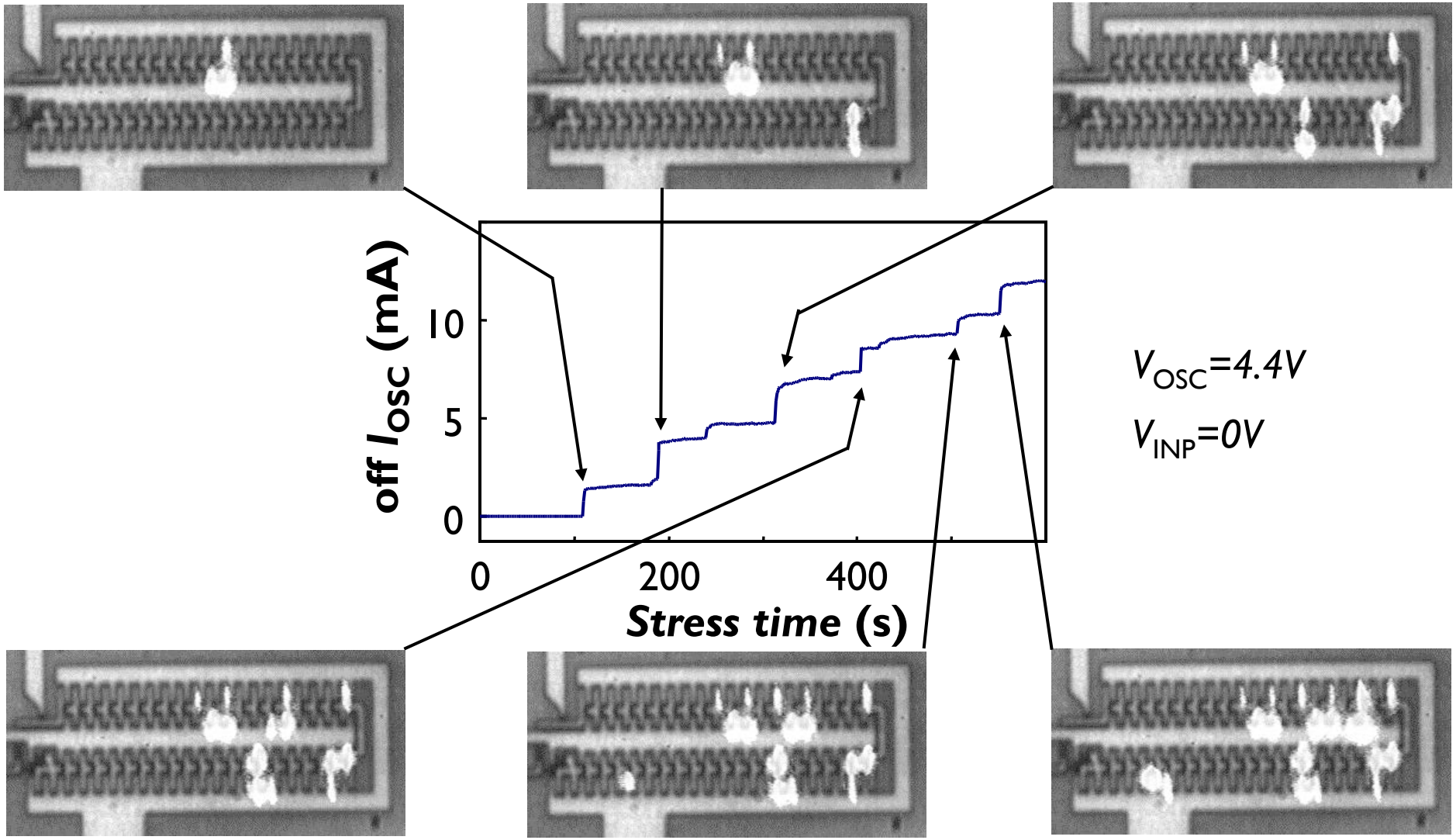
L = 0.18 μm, W_n = 1.3 μm, W_p = 2.5 μm, t_{ox} = 2.4 nm

After undergoing several breakdowns, the ring oscillator still functions



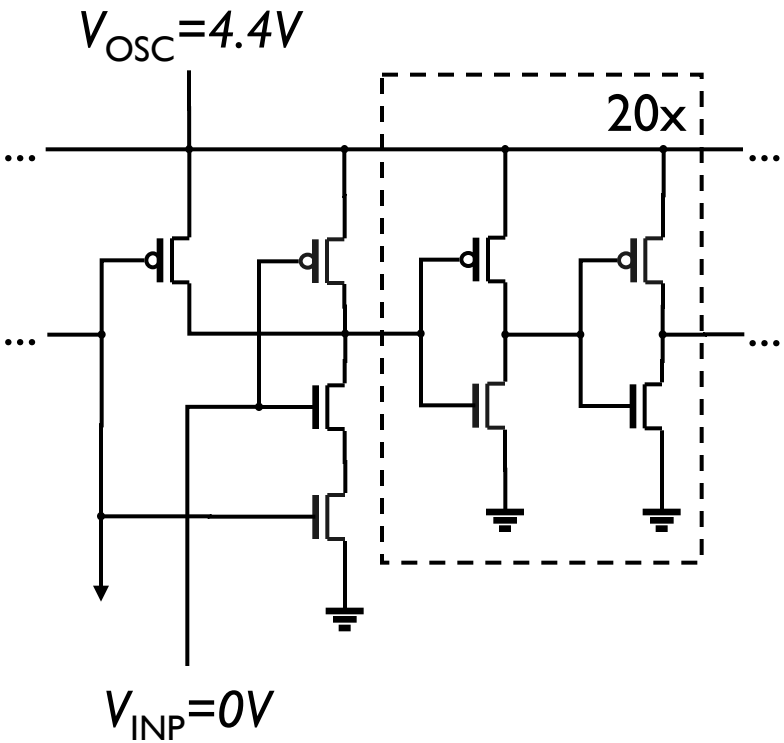
*Kaczer et al., TED **49**, p. 500 (2002)*

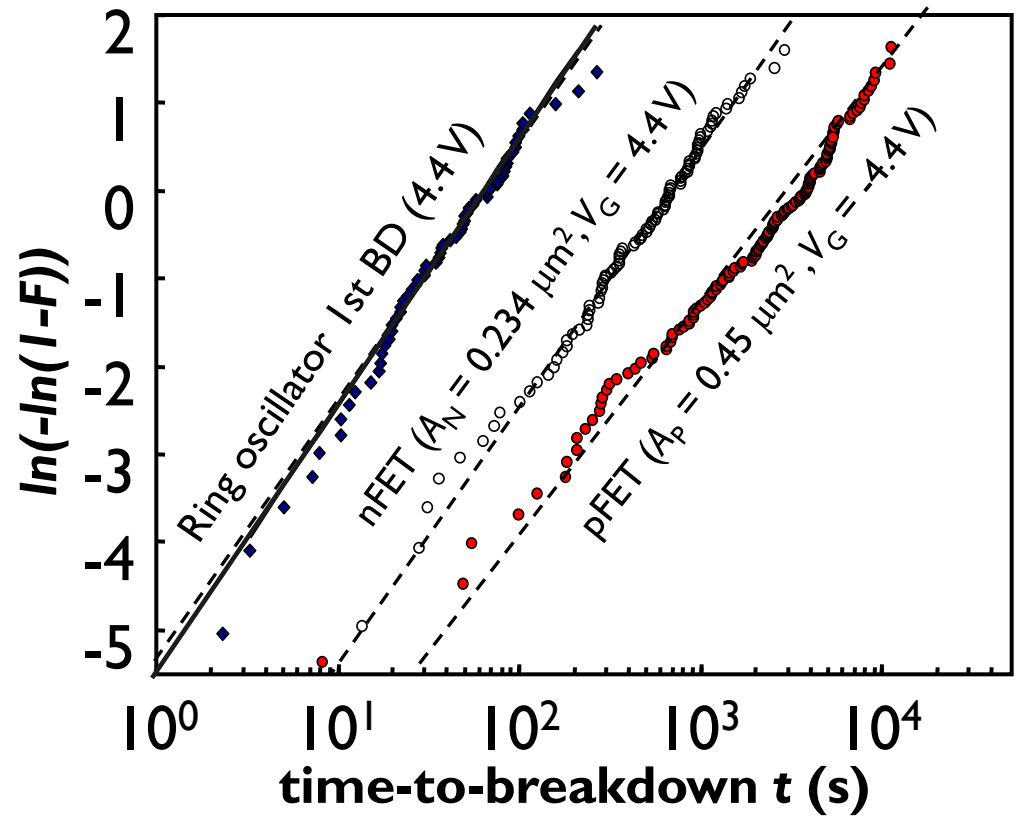
Current jumps correlated to gate oxide BDs



"Satellite" spots identified as hot carrier emission by spectral and SPICE analysis

Half of FETs stressed during static stress

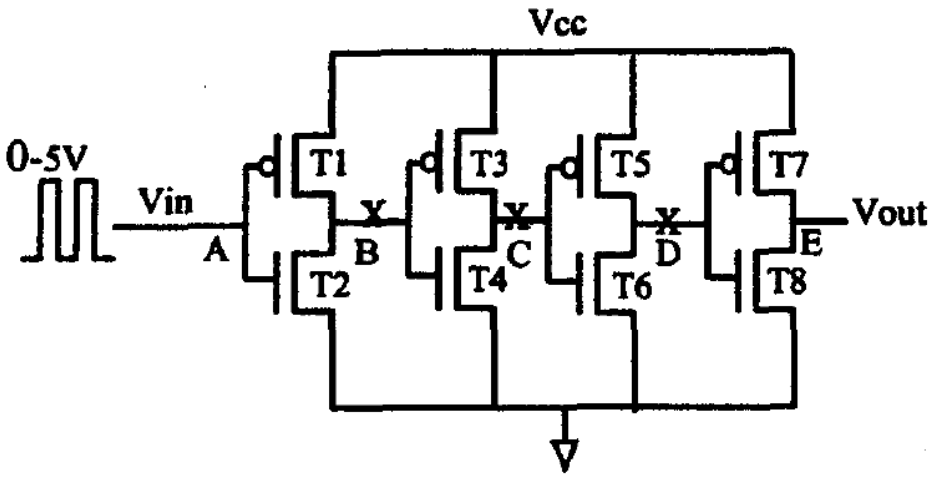




$$F_{osc}(t) = 1 - \left[1 - F_n(t)\right]^{N_n} \times \left[1 - F_p(t)\right]^{N_p}$$

t_{BD} distribution of individual n- and pFETs scales to ring oscillator time-to-1st-BD distribution

Simulating effect of BD on inverter chain



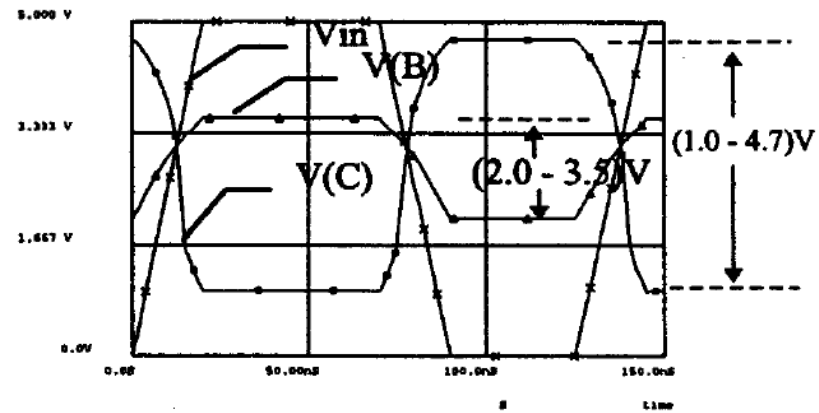


Figure 12a: SPICE simulation (nodes A, B, C) of n-channel gate to drain breakdown

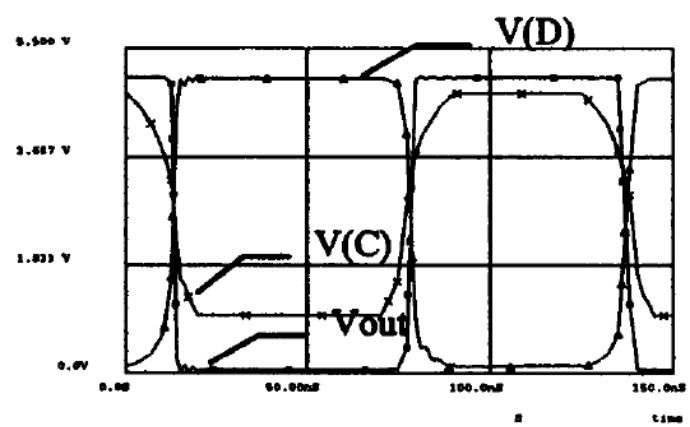
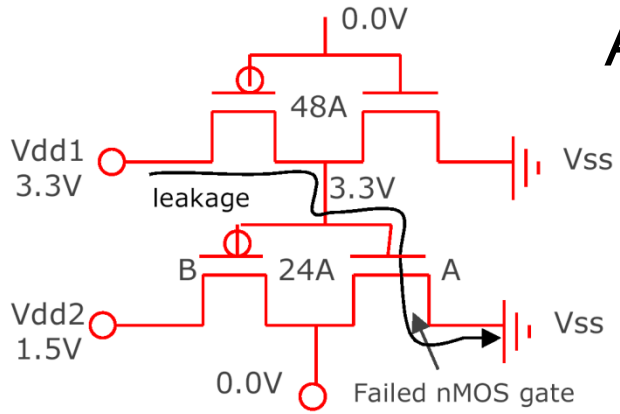


Figure 12b: SPICE simulation (nodes C, D, E) of n-channel gate to drain breakdown

Yeoh & Hu, IPFA, p. 149 (1995); ICSE, p. 59 (1998)

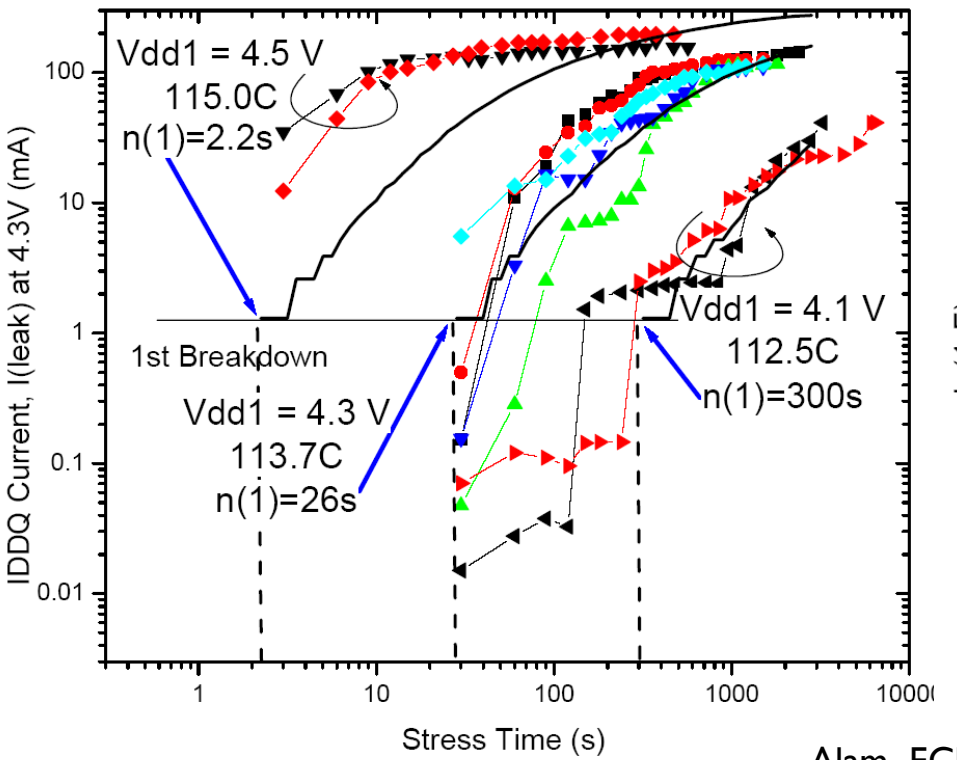
Multiple BDs studied on inverted chain

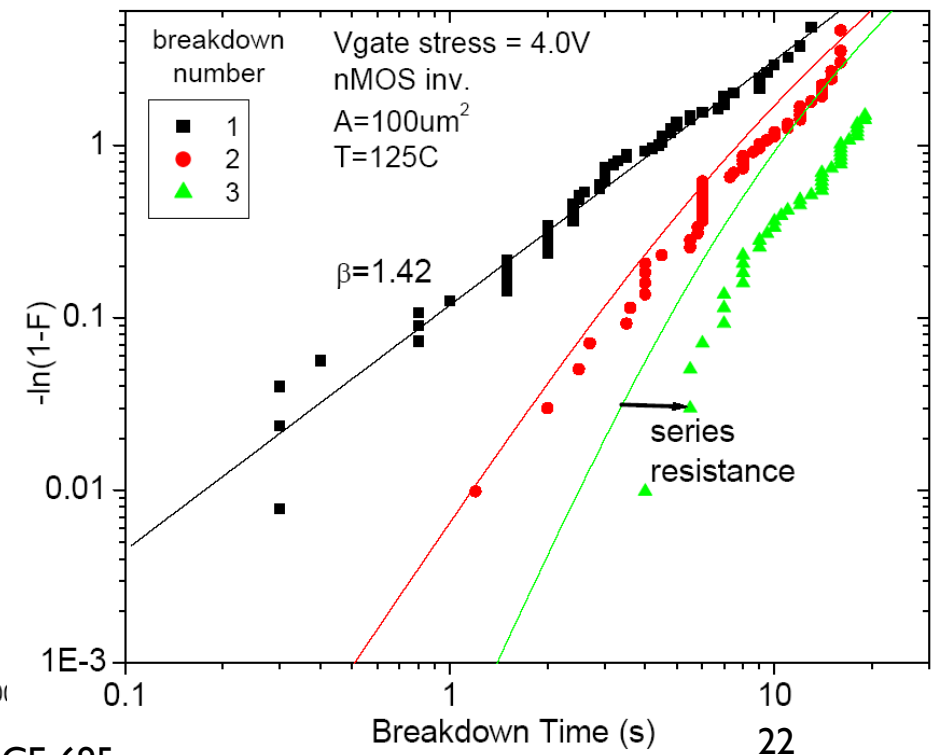


Assumed standby current time dependence :

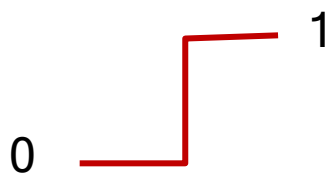
$$I_{leak} = I_o N_{bd} = I_o (t/\eta)^{\beta}$$

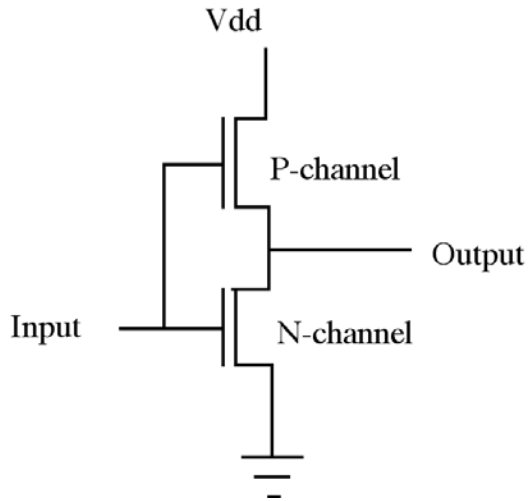
Mason et al., IRPS, p. 430 (2004)

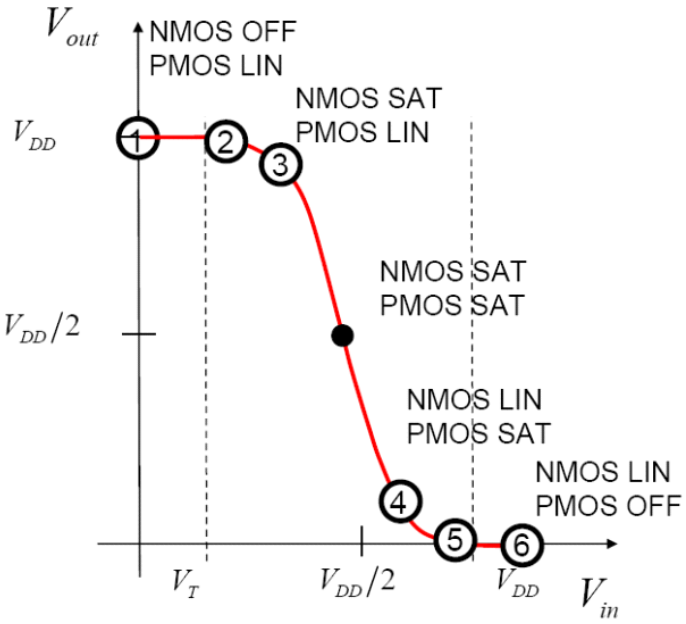


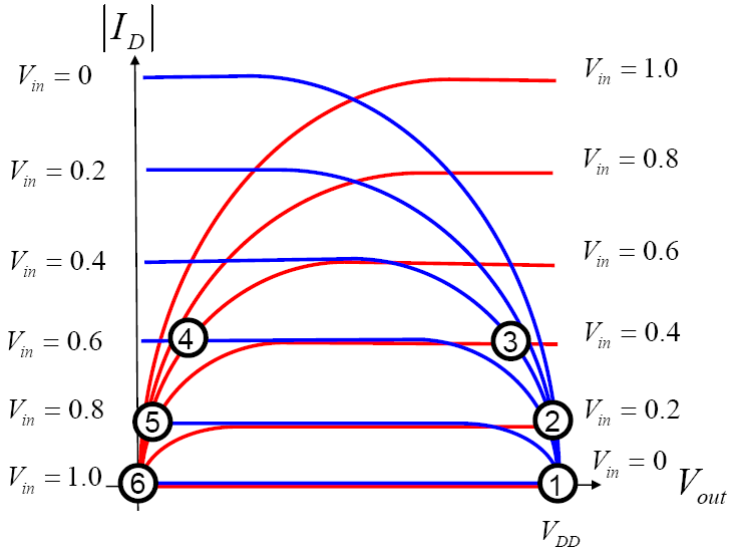


How does an invert work …

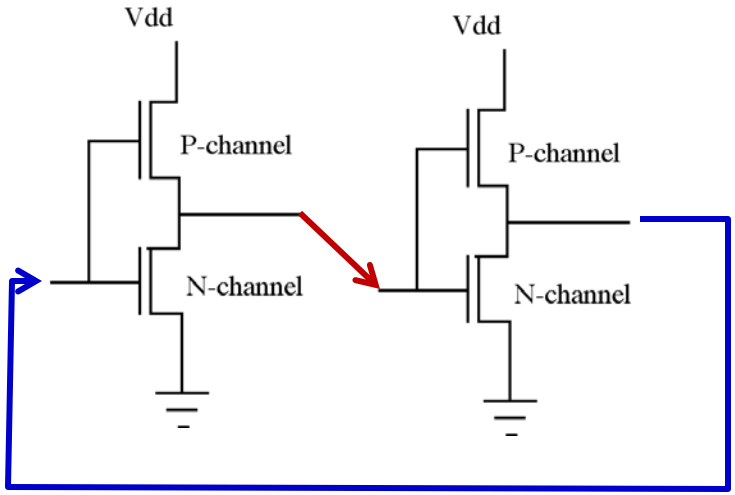


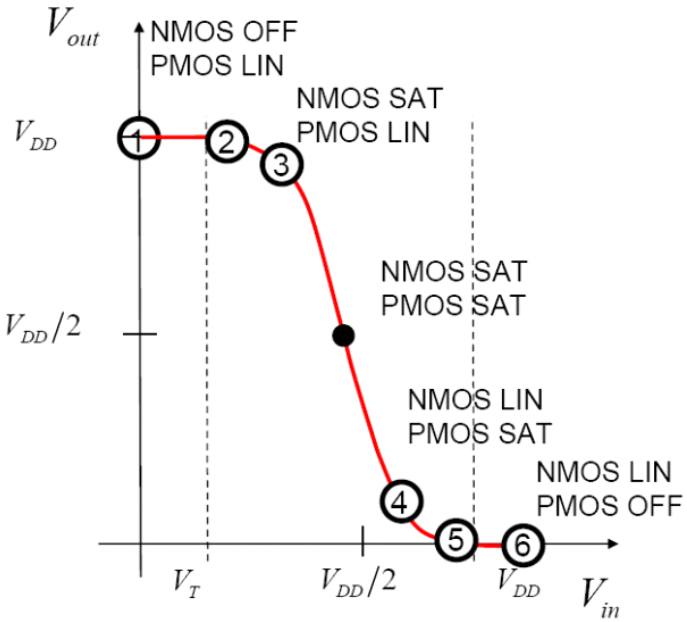


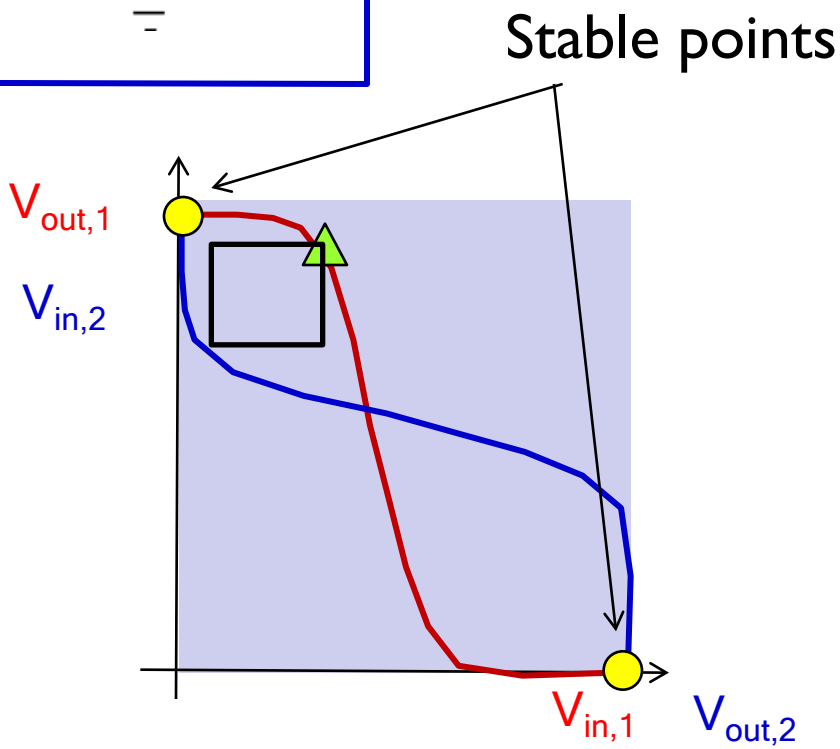




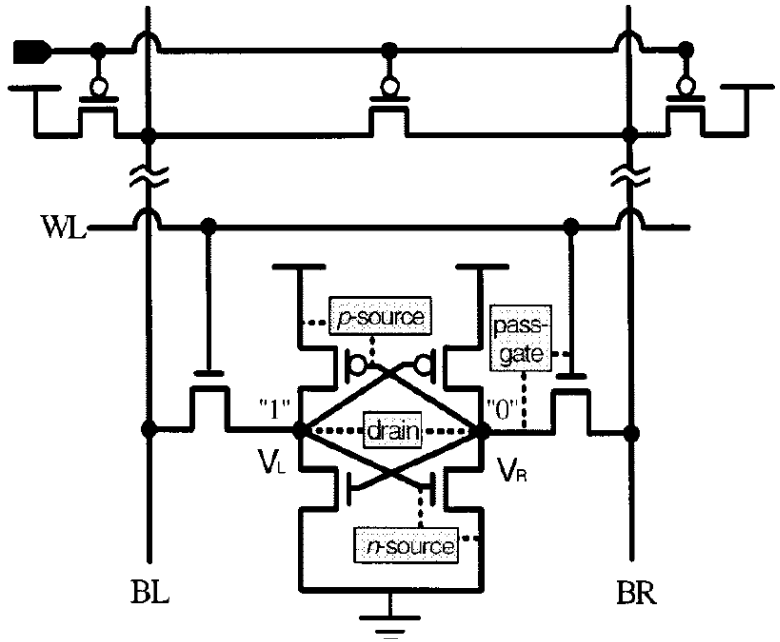
How does an invert work …

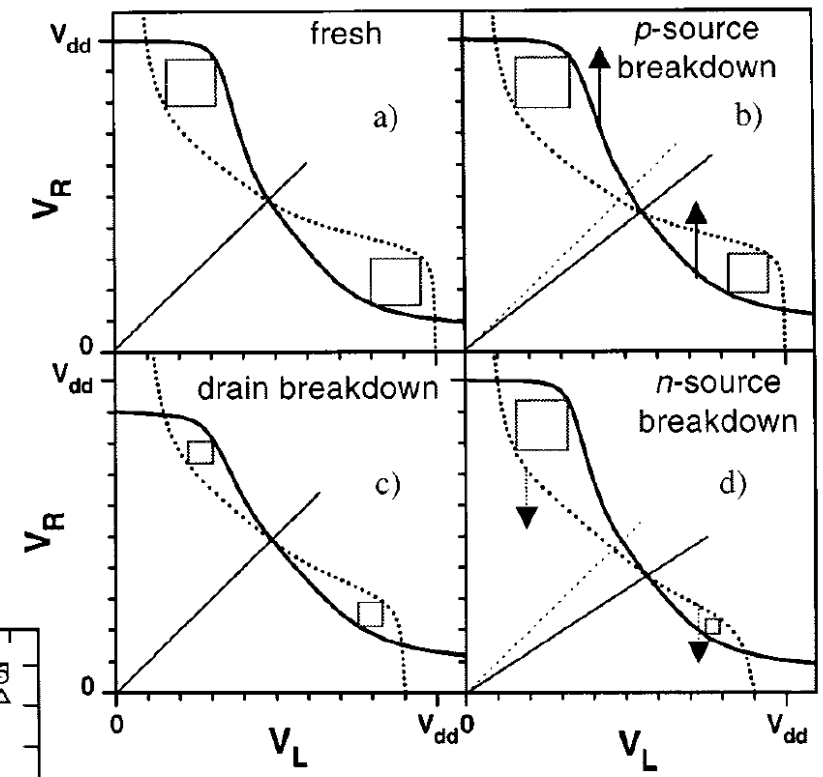


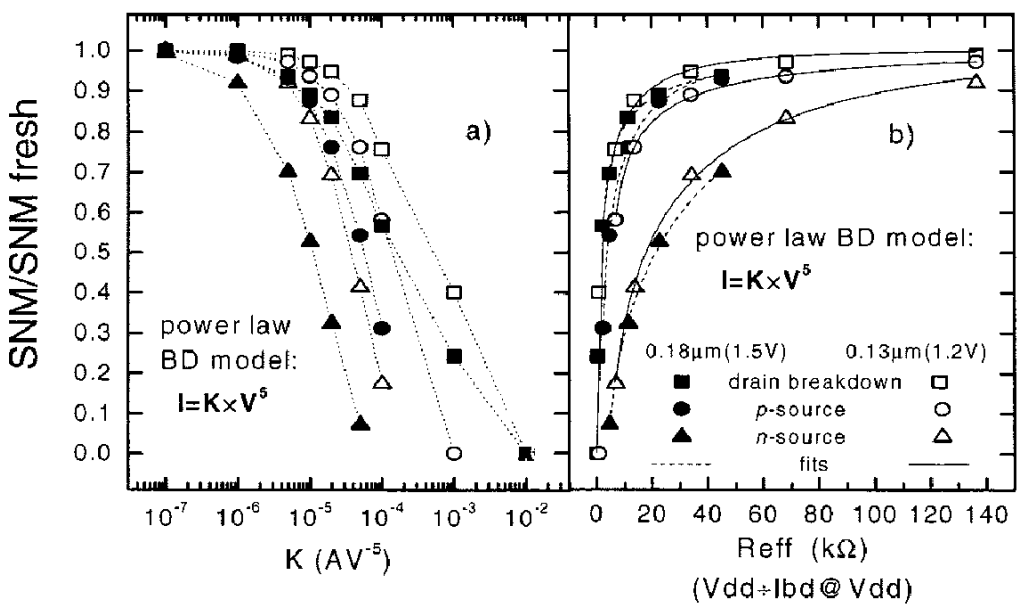




SRAM: nFET-source BD worst case



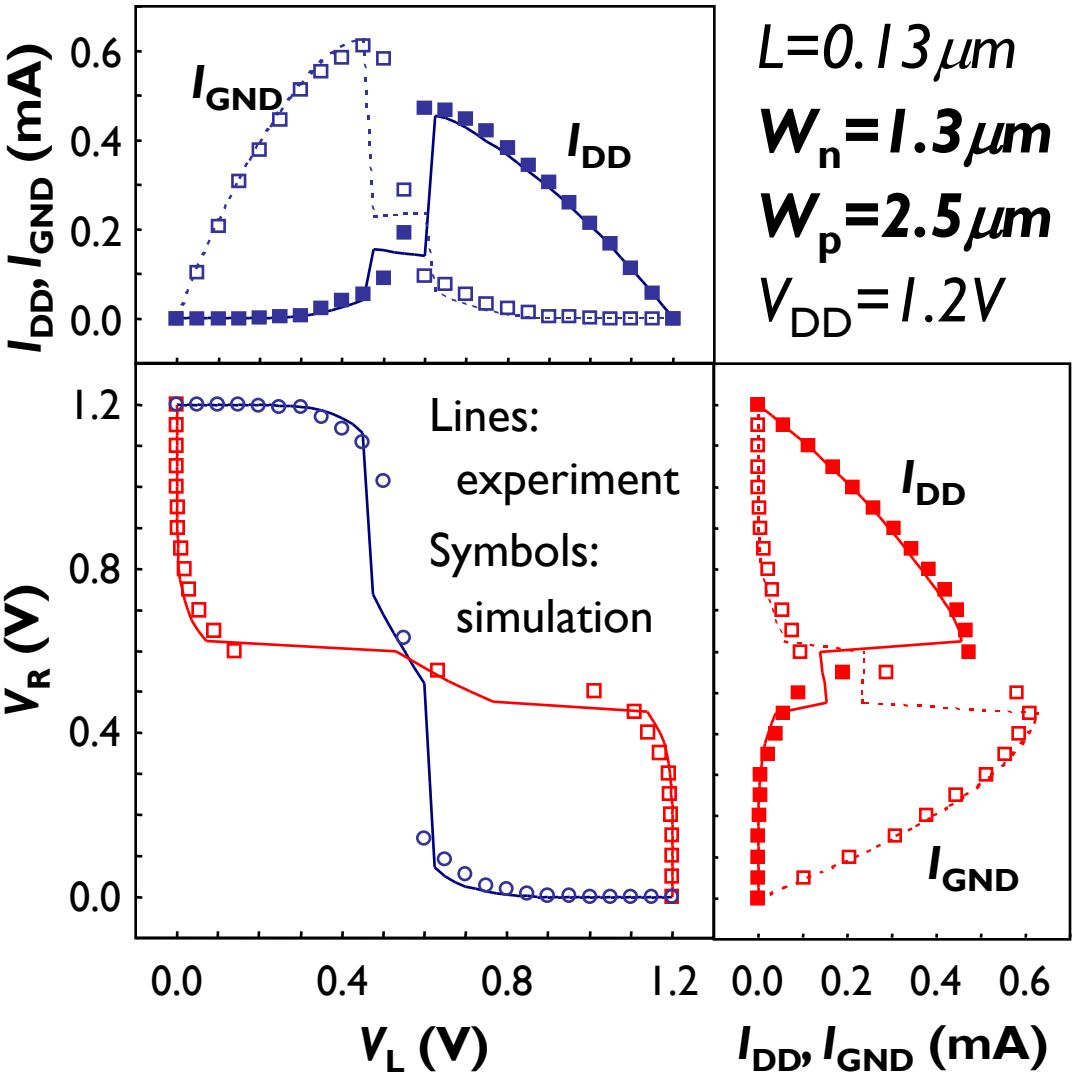


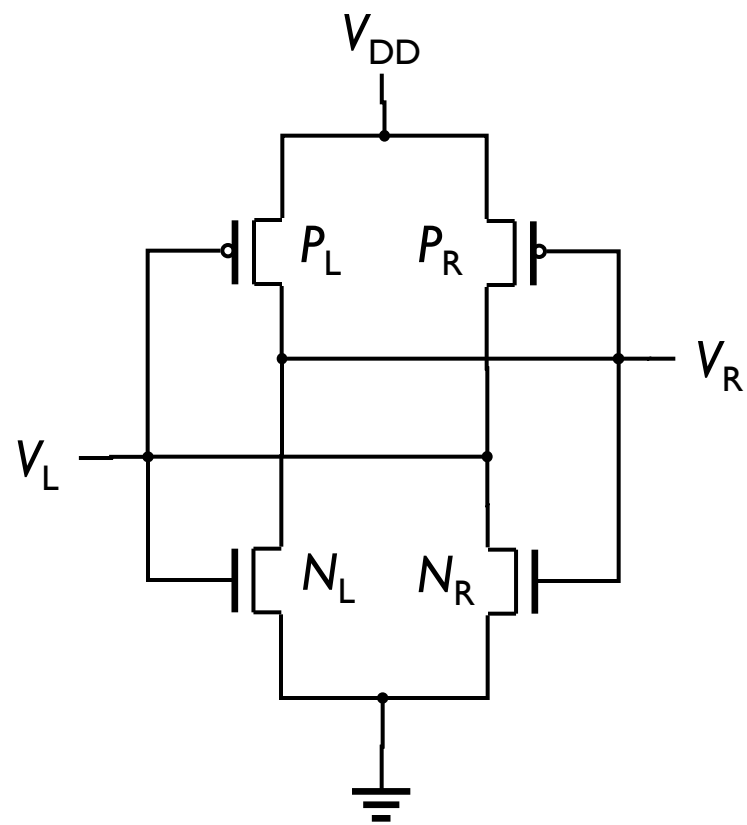


Non-linear SBD leakage:
$I=KV^5$

Rodriguez et al., EDL ***23****, p. 559 (2002)*

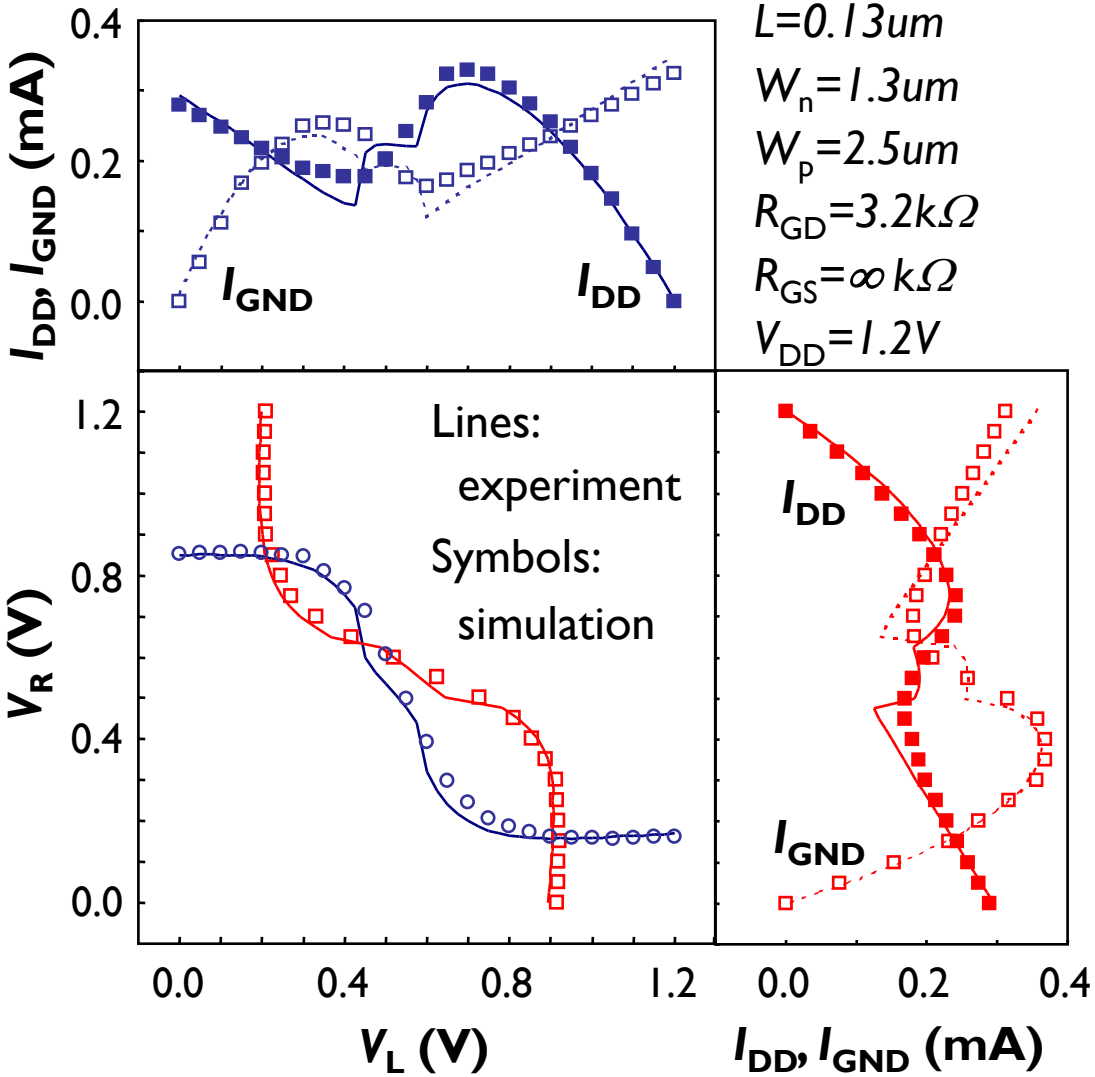
Experimental verification : as-fabricated "wide" SRAM : functioning



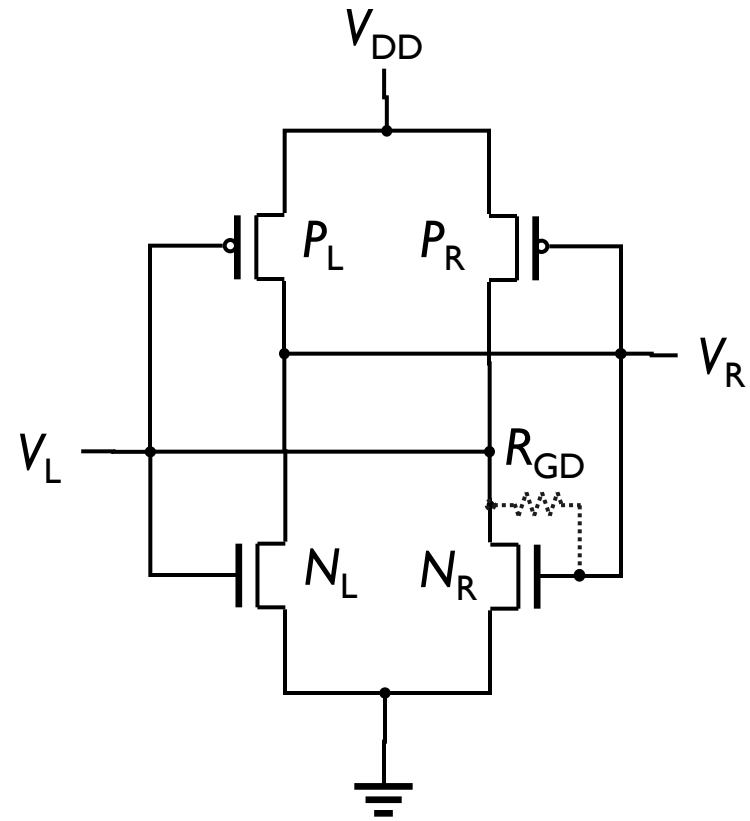


Kaczer et al., ESSDERC, p. 75 (2003)

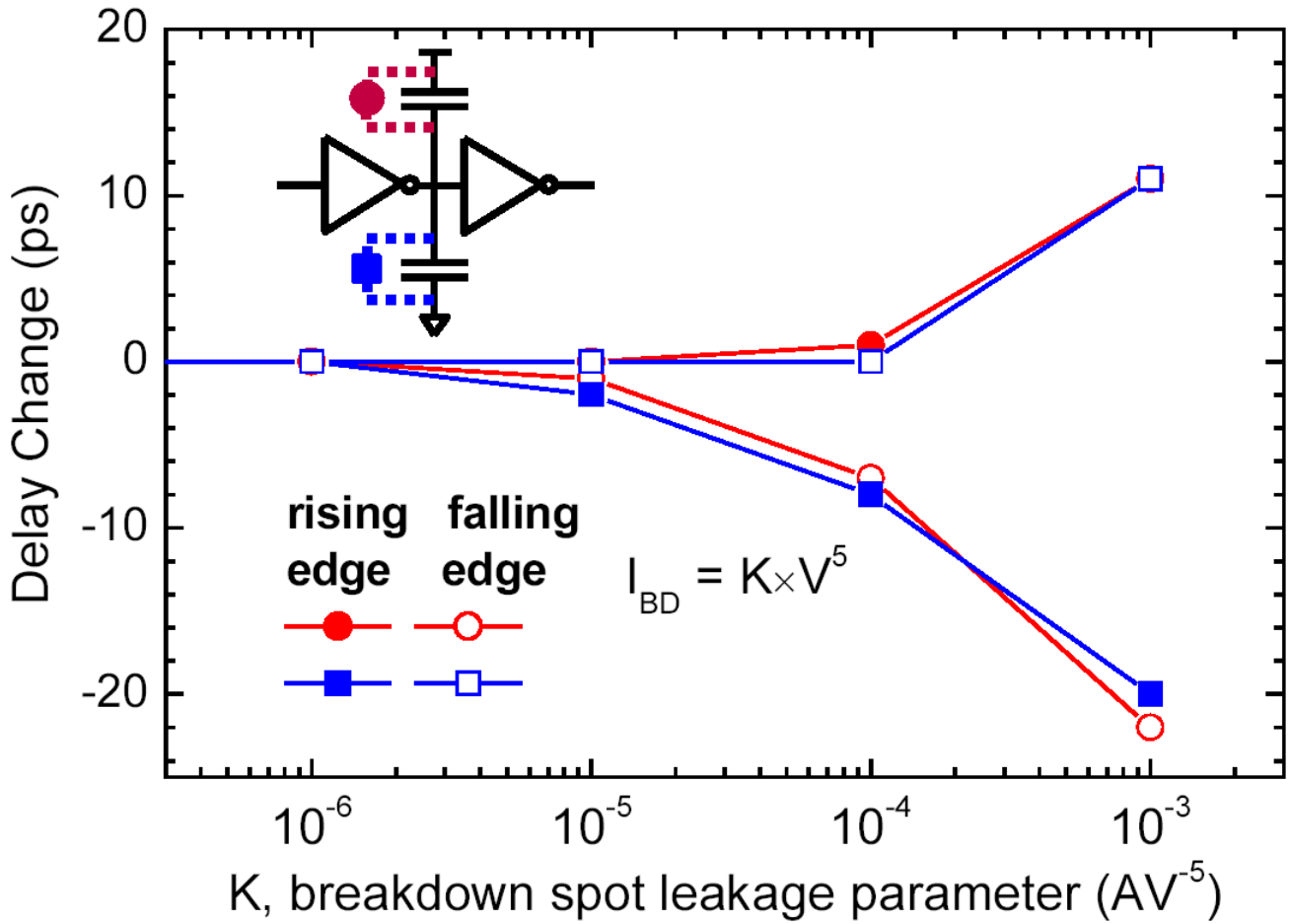
Wide SRAM after HBD at nFET drain: still functional with degraded SNM



$L=0.13um$
$W_n=1.3um$
$W_p=2.5um$
$R_{GD}=3.2k\Omega$
$R_{GS}=\infty\ k\Omega$
$V_{DD}=1.2V$

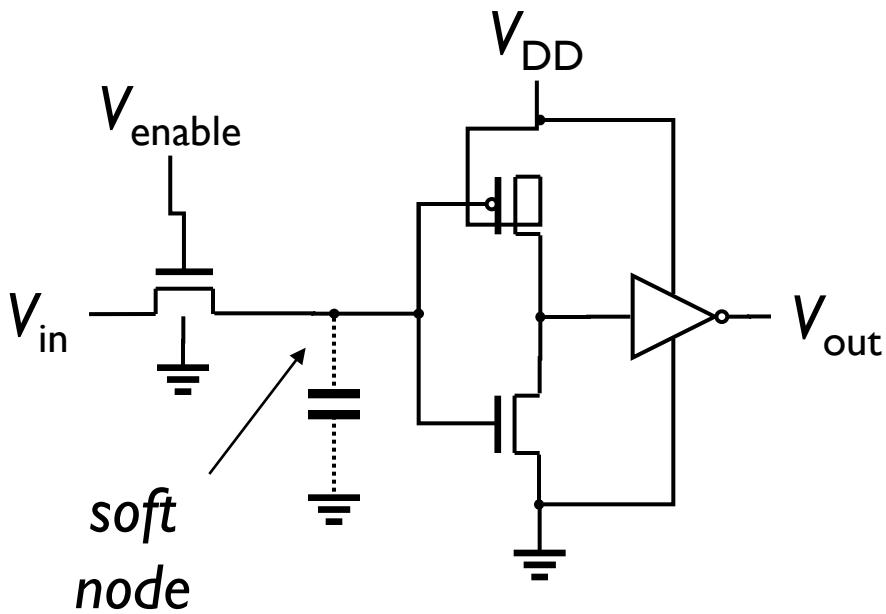


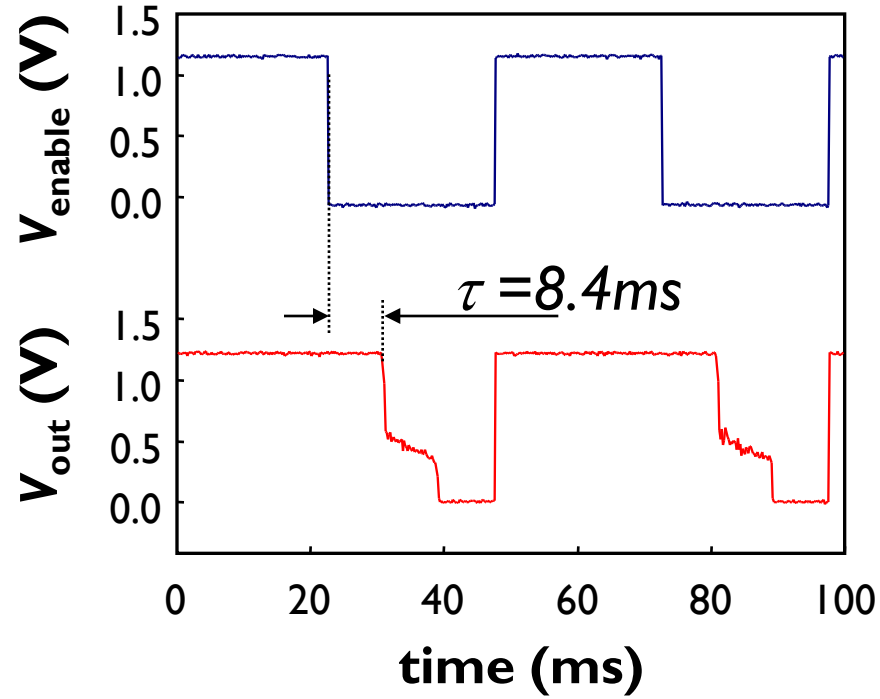
Effect of BD on circuit timing simulated



Stathis et al., Microel. Reliab. ***43****, p. 1193 (2003)*

Soft node : basis of dynamic logic, DRAM

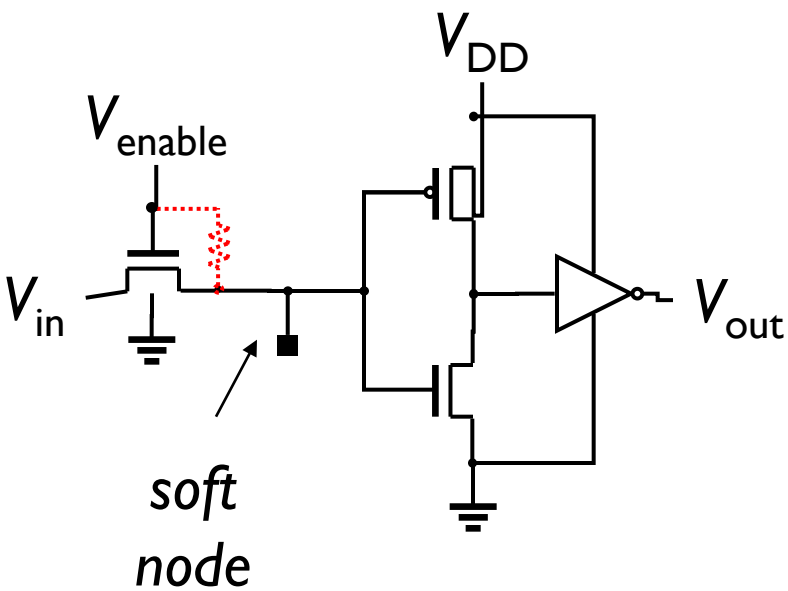


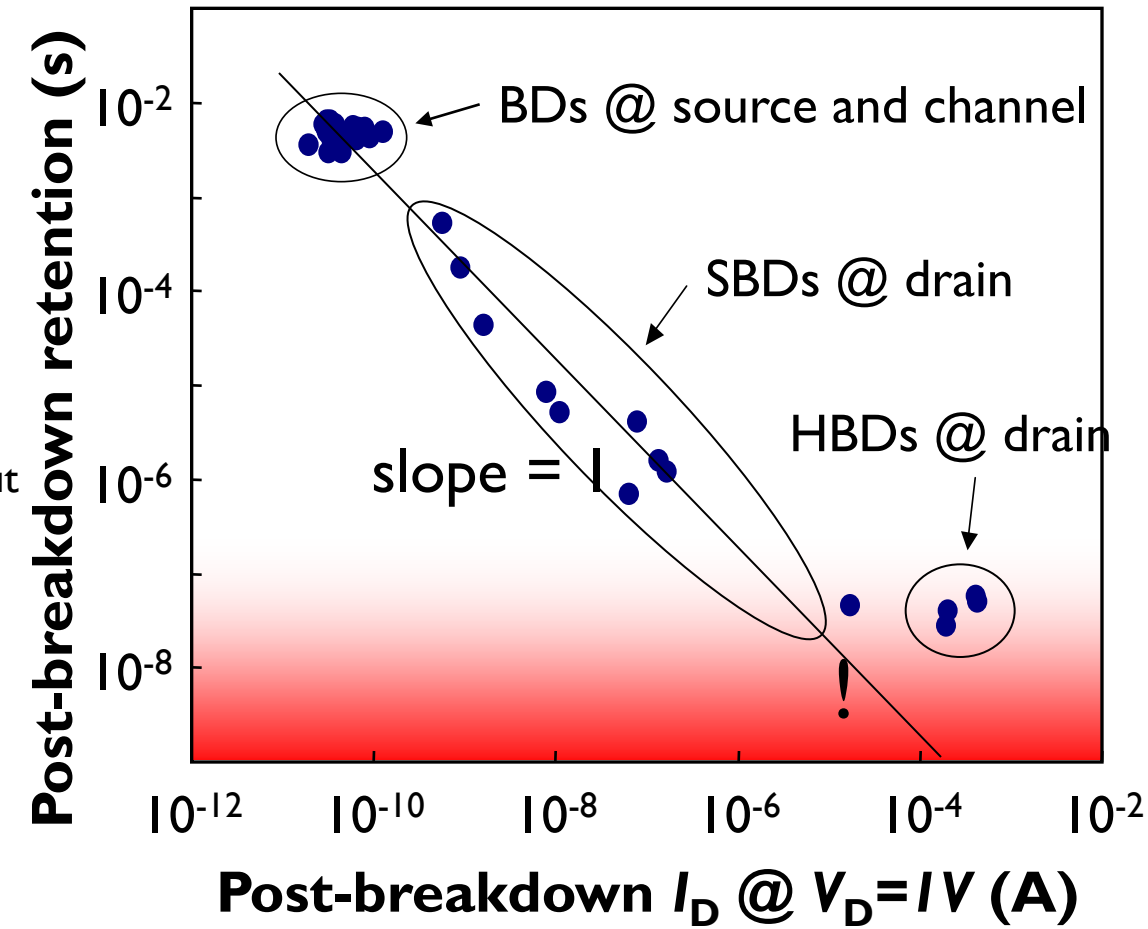


Circuit allows direct measurement of soft node retention time

*Kaczer et al., EDL **24**, p. 742 (2003)*

Post-BD retention proportional to I_D, i.e. soft node leakage

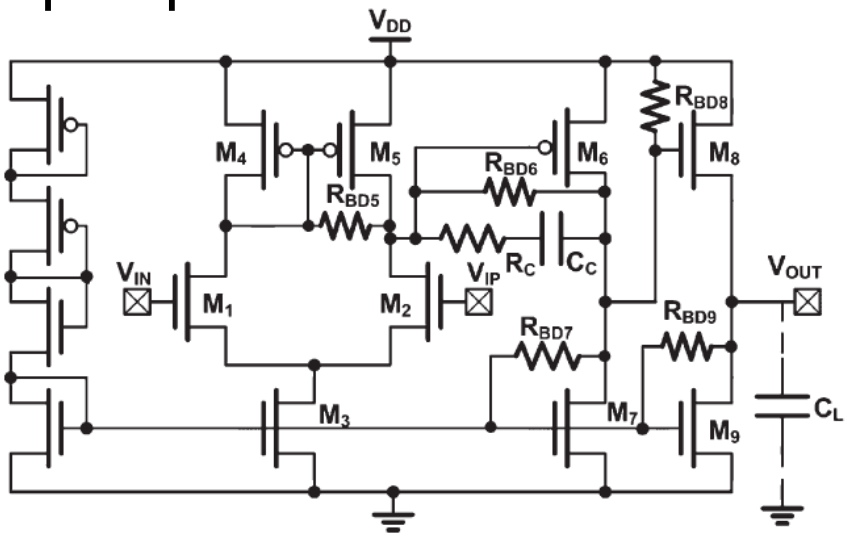


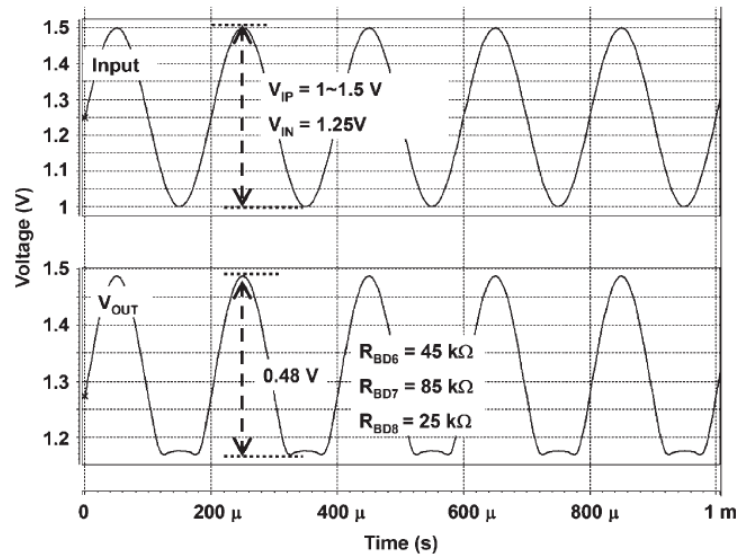


Dynamic logic, DRAM might be vulnerable even to SBD

BD in analog circuits

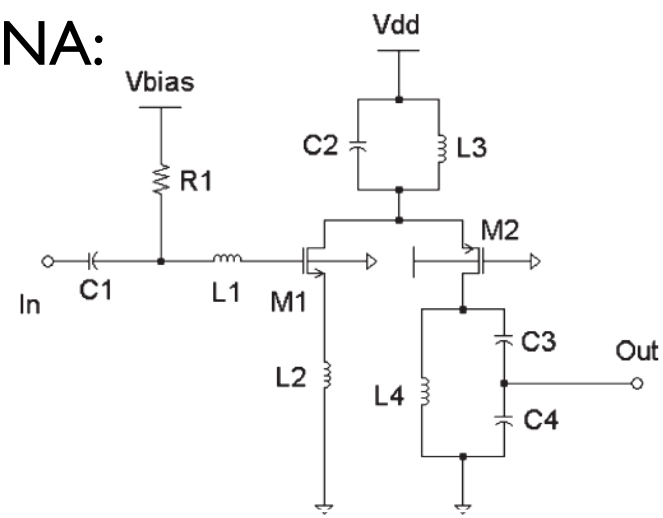
OpAmp: Two-Stage Operational Amplifier

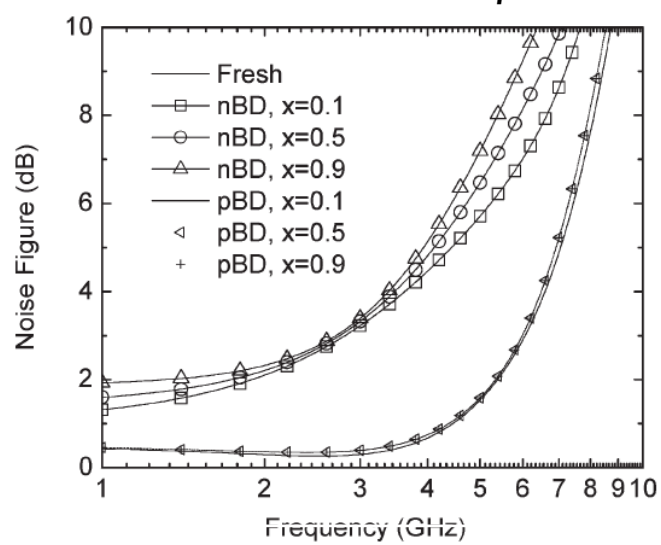




*Ker & Chen, TDMR **8**, p. 394*

LNA:





*Yu & Yuan, TED **54**, p. 59 (2007); also Yang et al., TDMR **3**, p. 93 (2003)*

Conclusions

- Post-BD circuit behavior can be successfully simulated if
  - ✓ pre-BD stress effects accounted for and
  - ✓ BD in affected FET(s) is well understood
    - ➢ BD position and conduction, FET parameter shifts
- In general, present circuits likely to remain functional after multiple SBD
  - ✓ "Wide" FETs can compensate even HBD
  - ✓ "Narrow" FETs can compensate SBD
  - ✓ On and standby currents, timing affected by BD
  - ✓ Some circuits (dynamic logic) might be vulnerable even to SBD

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