Course: **Semiconductor Device Fundamentals**
Level: **Undergraduate**
Module: **C**
Test: **C4**
Type: ***Open*** **Book,** ***Open*** **Notes**

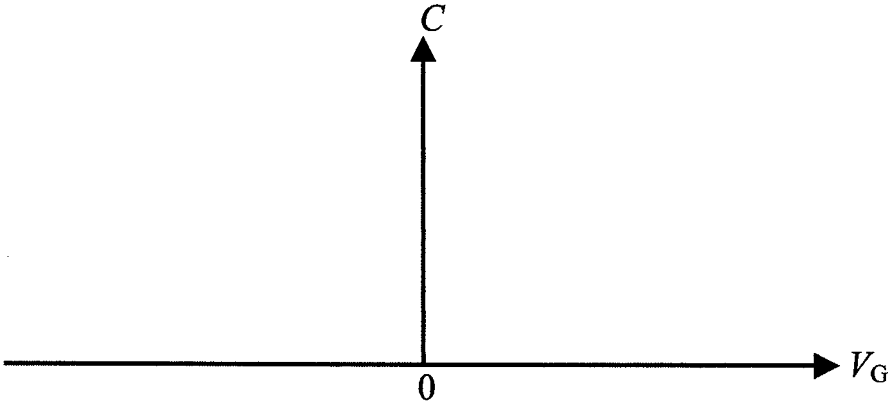
Problem Weighting---	**F-1...42 (6 each part)**
	F-2...18 (6 each part)
	F-3...24 (6 each part)
	F-4...16 (a,b,c,d–2; e,f–4)

F – 1

[Outcome–(vi)]

Given an ideal MOS-Capacitor maintained at room temperature with $x_o = 0.05\ \mu m$, $N_A = 5 \times 10^{15}/cm^3$, and $A_G = 5 \times 10^{-3}\ cm^2$;

(a) Sketch the expected shape of the high-frequency C–V_G characteristic to be obtained from the MOS-C.



(b) Determine the expected C_{MAX} value of the high-frequency C–V_G characteristic.

(c) Invoking the δ-depletion approximation, determine the expected C_{MIN} value of the high-frequency C–V_G characteristic. C_{MIN} must be determined to THREE SIGNIFICANT FIGURES.

(Continued)

(d) Determine V_T.

(e) Draw the energy band diagram characterizing the MOS-C when $V_G = V_T$. (Be sure to include the diagrams for all three components of the MOS-C, show the proper band bending in both the oxide and semiconductor, and properly position the Fermi level in the metal and semiconductor.)

(f) On the diagram completed in part (e), note the energy differences (in eV) on your diagram related to the applied gate voltage, ϕ_S, and the semiconductor doping.

(g) Draw the block charge diagram characterizing the MOS-C when $V_G = V_T$. Identify the physical cause of the charge blocks included in your diagram.

$\boxed{\text{F} - 2}$

[Outcome–(vi)]

Suppose instead of being grounded the *source* terminal of an ideal n-channel MOSFET is maintained at a constant voltage V_S, where $0 < V_S \le V_{Dsat}$.

(a) Appropriately modifying the text Square-Law derivation, obtain an expression for I_D below pinch-off as a function of V_G, V_D, and V_S.

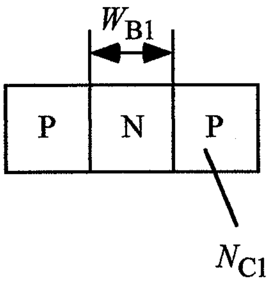
(b) What is V_{Dsat} for the specified situation? Record your reasoning.

(c) First sketch a representative I_D–V_D characteristic assuming V_G = constant > V_T and $V_S = 0$. Next, on the same set of coordinates, indicate how the characteristic would be modified if $V_S = V_{Dsat}/2$. Record your reasoning.

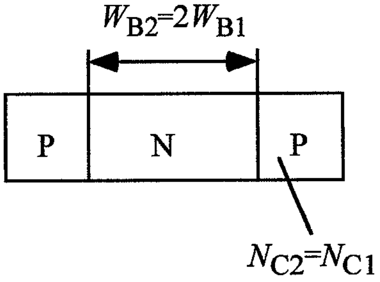
F – 3

[Outcome–(vii)]

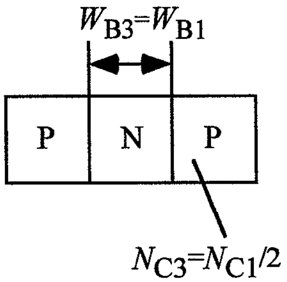
As pictured below, three BJTs are identical except that BJT #2 has a base width twice the base width of BJT #1, and BJT #3 has a collector doping one-half the collector doping of BJT #1. $N_E >> N_B >> N_C$ and $W/L_B << 1$ in all three BJTs.



BJT #1



BJT #2



BJT #3

For each of the following parameters...

- List *in order* the transistors with the highest, second highest, and lowest expected value of the cited parameter under comparable biasing. Use equal signs (=) to indicate equal expected values.
- Provide a clear math-based reason for the noted ordering.

(a) Emitter efficiency;
(b) Base transport factor;
(c) V_{CB0} if the BJTs are avalanche-breakdown limited;
(d) V_{CB0} if the BJTs are punch-through limited.

$\boxed{\text{F – 4}}$

[Outcome–(vii)]

Given the Ebers-Moll parameters $\alpha_F = 0.9950$, $\alpha_R = 0.4250$ and $I_{F0} = 5 \times 10^{-15}$A, determine (a) I_{R0}, (b) α_{dc}, (c) I_{CB0}.

(d) Circle the correct voltage polarity in the statements below.

...$V_{CB} > 0$ or $V_{CB} < 0$ if a *pnp* transistor is biased into saturation.

...$V_{CB} > 0$ or $V_{CB} < 0$ if a *pnp* transistor is active mode biased

(e) Suppose the d.c. operating point of a *pnp* transistor lies at the *boundary* between active mode and saturation mode biasing. Draw the appropriately simplified Ebers-Moll large signal equivalent circuit for the transistor at the specified operating point.

(f) Suppose a *pnp* transistor maintained at room temperature with the Ebers-Moll parameters given in part (a) is biased such that $V_{CB} = 0$ and $I_B = 1$ µA. Determine the emitter-base voltage (V_{EB}) being applied at the specified operating point.