Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**C**
Test:	**C7**
Type:	***Open* Book, *Open* Notes**

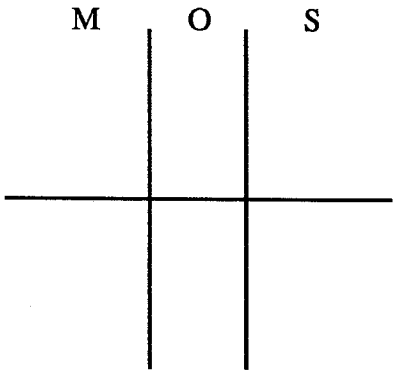
Problem Weighting is noted adjacent to each problem.

T3 - 1

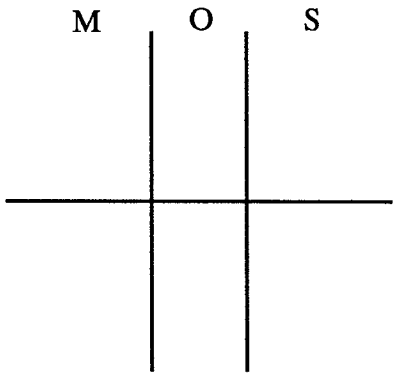
An ideal MOS capacitor is constructed on a substrate of **intrinsic** silicon with a 0.1μm thick insulating layer of silicon dioxide.

[6] (a) Sketch the energy band diagram for this capacitor under flat band conditions. Include the diagram for all three components of the MOS-C, properly position the Fermi level in the metal and semiconductor, and label the energy levels in your sketch.

[10] (b) Construct block charge diagrams representing the capacitor under the conditions of positive and negative gate bias.



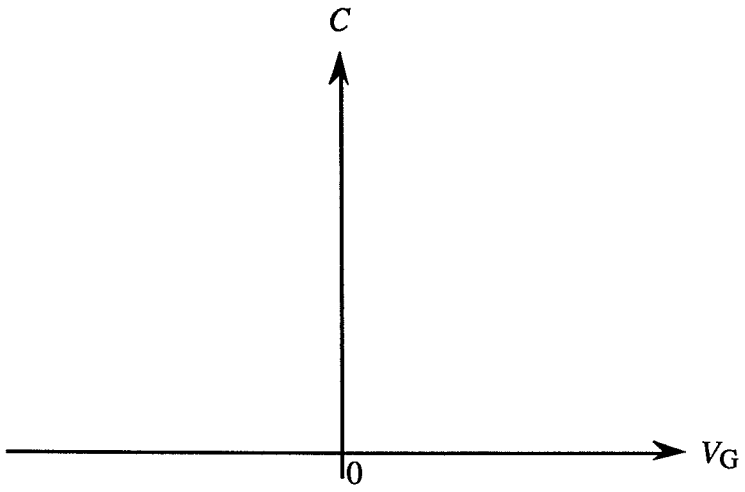
$V_G > 0$



$V_G < 0$

(Continued)

[12] (c) Invoking the delta-depletion theory, sketch the low-frequency *C–V* characteristic for the given MOS-C. Justify the form of your sketch in each region of operation.



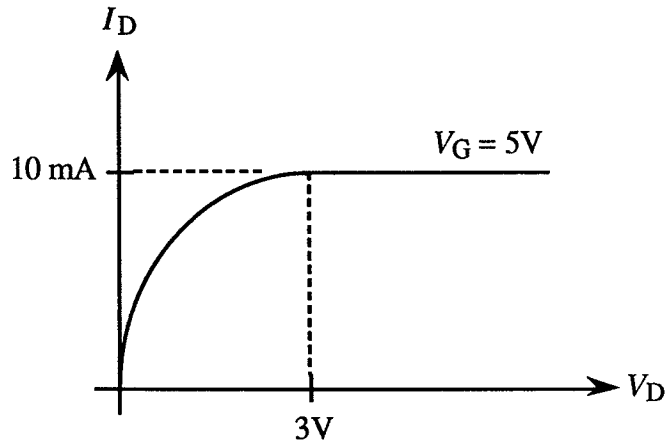
JUSTIFICATION:

[5] (d) Assuming that the gate area, A_G, is 2.9×10^{-3} cm^2, determine the maximum and minimum values of low frequency capacitance for this device.

C_{MAX} = pf	C_{MIN} = pf

T3 - 2

Shown below is an *I–V* characteristic for an ideal enhancement mode MOSFET with a substrate doping of $N = 10^{15}/cm^3$ ($n_i = 10^{10}/cm^3$) at room temperature.



[6] (a) Carefully sketch the inversion layer and depletion region inside the MOSFET corresponding to the bias point $V_G = V_D = 5V$ and label the doping types of the source, drain, and substrate.

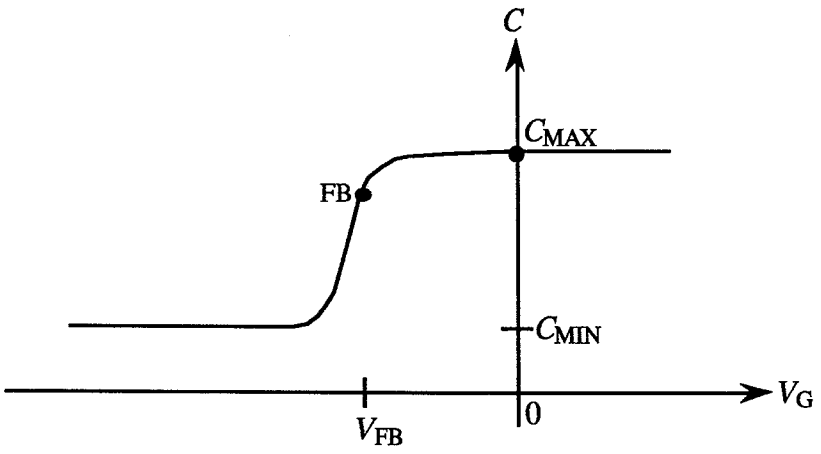
[5] (b) Determine the threshold voltage, V_T, for the given device.

[10] (c) A second ideal device is constructed having identical dimensions and material parameters except for the oxide thickness. If this device has an oxide twice as thick as the original, what is its threshold voltage?

[12] (d) If we assume that the threshold voltage for the second device introduced in part (c) is 2.5V (which it is not), what would be the value of the drain saturation current when $V_G = 5V$? NOTE: Base your result on the Square-Law Theory.

T3 - 3

The capacitance-voltage (C–V) characteristic exhibited by an Al-SiO_2-Si capacitor maintained at $T = 300K$ is reproduced below. Note that $C_{MAX} = 200pf$, $C_{MIN} = 67pf$, and the flat band voltage $V_{FB} = -0.71V$. There are no mobile ions in the oxide ($Q_M = 0$), the interfacial trap density is negligible ($Q_{IT} = 0$), and $A_G = 2.9 \times 10^{-3} cm^2$.



$C_{MAX} = 200$ pf
$C_{MIN} = 67$ pf
$V_{FB} = -0.71$ V

[3] (a) Is the semiconductor component of the MOS-C doped n-type or p-type? Indicate how you arrived at your answer.

[5] (b) Adding to the figure in the problem statement and using a dashed line, sketch the C–V curve one would expect from an IDEAL version of the given MOS-C. Also indicate the flat band point on the ideal-device characteristic.

[2] (c) In the delta-depletion C–V analysis, how is the minimum high-frequency capacitance (C_{MIN}) related to W_T?

(Continued)

[24] (d) Determine the fixed charge/cm^2, Q_F, in the given device.

HINT: Figs. 2.9 and 4.3 may be helpful in determining some of the device parameters required to complete this problem.

SUGGESTIONS: To receive the maximum possible partial credit, put a box around important intermediate results. Indicate in words what you are doing.

T3 - 4

EXTRA CREDIT

[2] (a) Indicate what the following acronyms stand for:

MESFET...

MODFET...

[2] (b) For a fixed channel length and channel width, *name* two other MOSFET parameters that can be adjusted to minimize small-dimension effects. Also indicate *how* the parameters must be adjusted to *reduce* small dimension effects.

[2] (c) How can you tell if velocity saturation is affecting the I_D–V_D characteristics of a MOSFET?

[2] (d) The field-aided injection and subsequent trapping of carriers in the gate oxide near the drain can lead to serious degradation of short-channel MOSFETs. *Describe* a popular approach for minimizing the problem.

[2] (e) Can *punch-through* occur in a MOSFET? Explain.