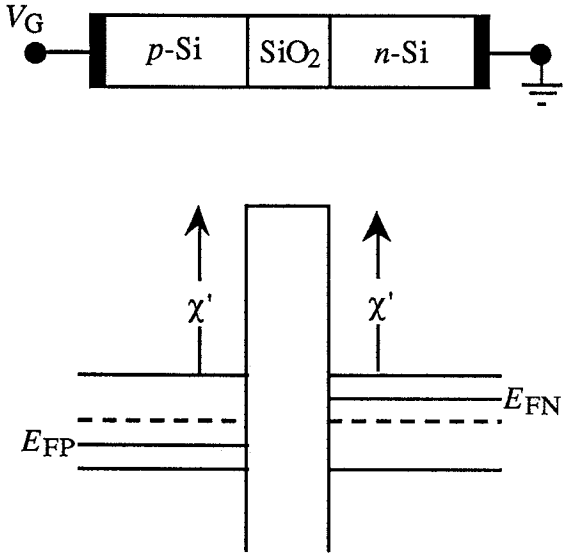
Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**C**
Test:	**C8**
Type:	***Open* Book, *Open* Notes**

Problem Weighting is noted adjacent to each problem.

T3 - 1

The energy band diagram for a ***p***-Si /SiO_2/ ***n***-Si (SOS) capacitor under *flat band* conditions is given below. To achieve the pictured state there must of course be a non-zero voltage applied to the SOS-C gate. The SOS-C is ideal except for a non-zero workfunction difference.
T = 300K, N_A(p-side) = $10^{15}/cm^3$, N_D(n-side) = $10^{15}/cm^3$, n_i = $10^{10}/cm^3$, $x_o = 5 \times 10^{-6}$cm, and $A_G = 10^{-3}$ cm^2.



[6] (a) What is the voltage being applied to the ***p***-Si /SiO_2/ ***n***-Si SOS-C to achieve the pictured flat band condition? Give both the polarity and magnitude of V_G.

[8] (b) Sketch the energy band diagram and the associated block charge diagram for the SOS-C when a *large positive* gate voltage (say $V_G > 5V$) is applied to the device. Add descriptive words to your sketches as necessary to forestall a misinterpretation of your answer.

[8] (c) Sketch the energy band diagram and the associated block charge diagram for the SOS-C when a *large negative* gate voltage is applied to the device.

[8] (d) Make a sketch of the *high-frequency* C–V_G characteristic to be expected from the SOS-C described in this problem. Explain how you arrived at your C–V_G sketch. (No explanation, no credit.)

[10] (e) Invoking the δ-depletion approximation, what will be the *minimum* capacitance exhibited by the device? Give both a symbolic and numerical answer.

T3 - 2

Fig. 3.10 from p.79 of Volume IV is reproduced below. For the purposes of this problem, consider the characteristics plotted in the figure to be experimental MOSFET characteristics.

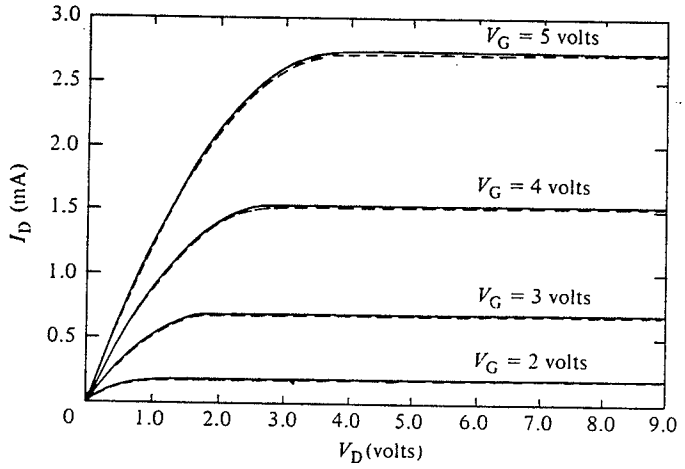


Fig. 3.10 Theoretical current-voltage characteristics of an n-channel MOSFET with x_o = 0.05 μm, $N_A = 10^{15}/cm^3$, $\overline{\mu}_n$ = 550 cm^2/V-sec, L = 7 μm, Z = 70 μm and T = 23°C. The solid-line curves were derived from the exact-charge result while the dashed-line curves were computed using the charge-sheet theory. (Reprinted with permission from *Solid-State Electronics*, R. F. Pierret and J. A. Shields, **26,** 143, © 1983, Pergamon Press plc.)

[6] (a) Carefully sketch the inversion layer and depletion region inside the MOSFET corresponding to the biasing point of $V_G = V_D = 5V$. Also insert the doping type of the source and drain islands.

[6] (b) Invoking the square-law relationships, and making use only of the plotted characteristics (ignore the figure caption information), what approximately is the MOSFET threshold voltage (V_T)? Explain how you arrived at your answer.

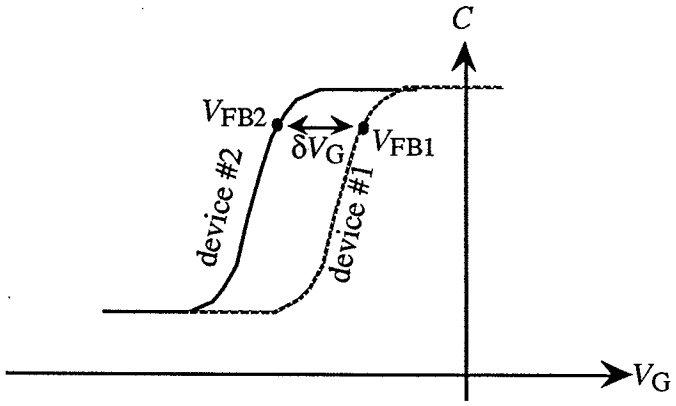
[6] (c) Given only the parametric values in the figure caption (ignoring the characteristics themselves), what is the expected MOSFET threshold voltage (V_T)?

[6] (d) Making use only of the plotted characteristics, estimate g_d if the quiescent operating point of the MOSFET is $V_G = 5V$, $V_D = 0$. Indicate how you arrived at your answer.

[6] (e) Determine g_m if the quiescent operating point of the MOSFET is $V_G = V_D = 5V$. Indicate how you arrived at your answer.

T 3 - 3

The three parts of this problem are similar. A pair of MOS-C's are taken to be identical except for one physical difference. The physical difference causes a voltage displacement of the C-V_G characteristics derived from the two devices as illustrated below. Defining $\delta V_G = V_{FB1} - V_{FB2}$, where V_{FB1} and V_{FB2} are the flat band gate voltages of devices #1 and #2 respectively, your job in each case will be to determine δV_G.



[10] (a) Two MOS-C's are identical in every way except device #1 has an aluminum (Al) gate while device #2 has a gate made of gold (Au). Determine the expected value of δV_G. Record your work.

(Continued)

[10] (b) Two MOS-C's are identical in every way except device #1 is fabricated on a (100)-oriented Si surface and device #2 is fabricated on a (111)-oriented Si surface. In both devices the interfacial trap charge is negligible ($Q_{IT} = 0$). Also, both devices were annealed in N_2 after a dry O_2 oxidation to minimize the fixed charge. Assuming $C_o = 3 \times 10^{-8}$ farads/cm^2, determine (approximately) the expected value of δV_G. Record your work.
HINT: See information item #2 on p.104 and Fig. 4.9(b) on p.105 of Volume IV .

[10] (c) Two MOS-C's are identical in every way except the Na^+ ions in device #1 are all piled up right at the *metal-oxide* interface, while in device #2 the Na^+ ions are all piled up right at the *oxide-semiconductor* interface. Taking $C_o = 3 \times 10^{-8}$ farads/cm^2 and $Q_M/q = 5 \times 10^{11}$/cm^2, determine the expected value of δV_G. Record your work.
NOTE: You are to assume δ-function type ionic distributions in working this problem.

T3 - 4
EXTRA CREDIT

[2] (a) Name the three most commonly cited indications of short-channel effects.

[2] (b) Other than the I_{Dsat} being reduced, in what other significant way do the experimental I_D–V_D characteristics presented in Fig. 5.8(a) on p.137 differ from standard MOSFET I_D–V_D characteristics?

[2] (c) What do **ELO** and **SOI** stand for?

[2] (d) What is the difference between a **MODFET** and a **HEMT**?

[2] (e) The Fig. 5.2 I_D–V_D characteristics on p.128 of Vol. IV exhibit severe short-channel effects. For one, with a $V_T < 0$, I_D should be identically zero for gate voltage $V_G > 0$. Instead, I_D is not zero, with a $I_D \propto V_D^2$ type dependence being observed. What is the cause of the noted effect?