Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**C**
Test:	**C10**
Type:	**Closed Book, Closed Notes**
Note:	**Available Info/Equation Sheets**

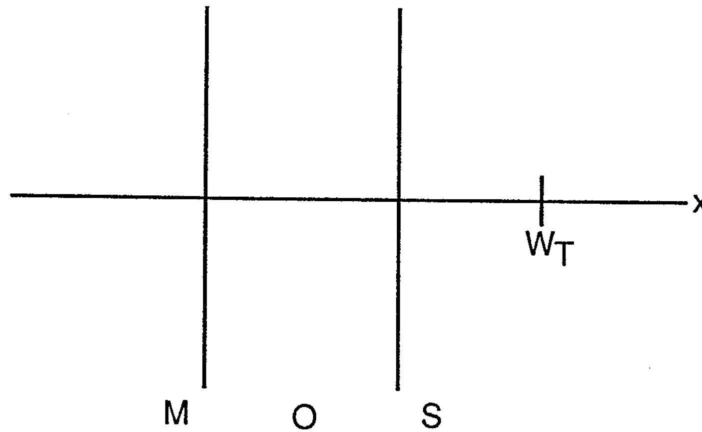
Problem Weighting is noted adjacent to each problem.

I. MOS Fundamentals

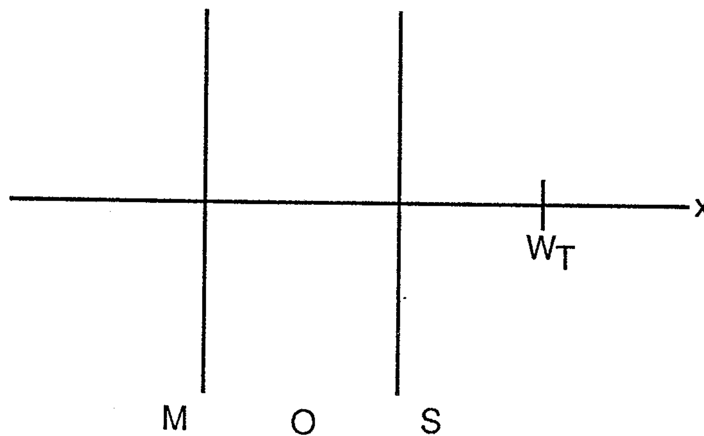
NOTE: In Questions (1)–(5) assume $T = 300\text{K}$, $kT/q = 0.026\text{V}$ and $n_i = 10^{10}/\text{cm}^3$.

4pts (1) An MOS-C has $\phi_F = -0.3$ volts. What is the doping in the silicon?

5pts (2) Sketch the block charge diagram for an ideal n-type MOS-C with $\phi_S = \phi_F$.



5pts (3) Sketch the block charge diagram for an ideal n-type MOS-C in total deep depletion.



6pts (4) An ideal silicon MOS-C is doped $N_A = 3 \times 10^{16}$ cm^{-3}. The oxide thickness is 0.1μm.

a) What is the oxide capacitance per unit area (F/cm^2)?

b) Compute the gate bias, V_G, at the onset of of inversion.

9pts (5) An ideal silicon MOS-C is doped $N_D = 3 \times 10^{16}$ cm^{-3}. The oxide thickness is 0.1μm. Invoking the δ-depletion approximation, compute the surface potential, ϕ_S, for each of the following cases.

a) Flat band

b) $V_G = 5$ volts

c) $V_G = -8$ volts

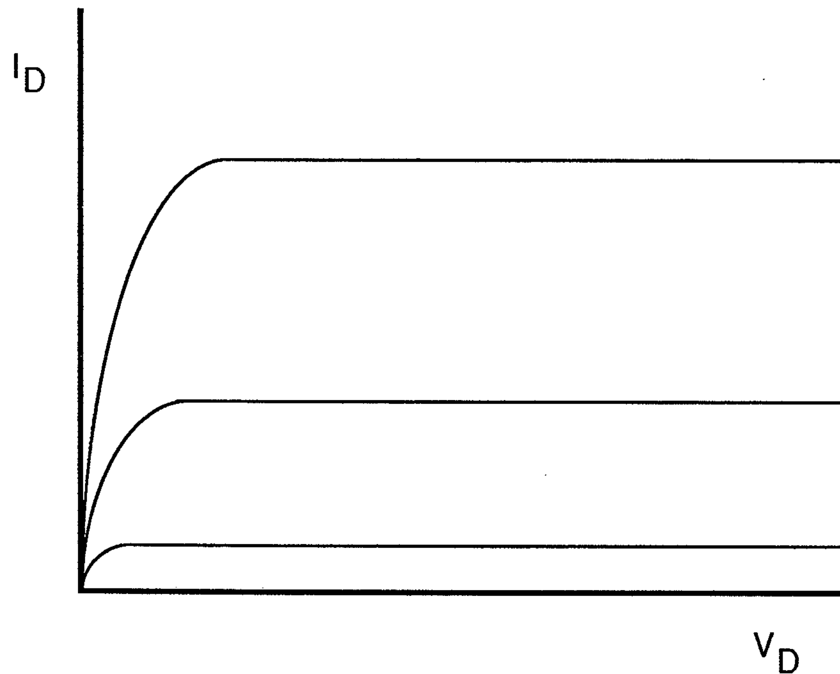
II. MOSFETs

5pts (6) What advantage does an *n*-channel MOSFET have over a *p*-channel MOSFET?

5pts (7) Sketch the structure of a standard *p*-channel MOSFET. Label the source, drain, gate, and back contacts. Show the direction of hole current in the channel when the device is in saturation.

5pts (8) Why does the effective mobility in the channel differ from the bulk mobility?

Use assumptions consistent with the Square Law Theory and the sketch shown below to help answer Questions 9 & 10.



3pts (9) In the saturation region, how does the drain current vary with the transconductance?

a) The drain current is independent of the transconductance.

b) The drain current increases as the transconductance increases.

c) The drain current decreases as the transconductance increases.

d) The drain voltage must be known to answer this question.

3 pts (10) In the saturation region, how does the channel conductance vary with the drain voltage?

a) The channel conductance increases as the drain voltage increases.

b) The channel conductance increases as the drain voltage decreases.

c) The channel conductance is zero in the saturation region.

d) The drain current must be known to answer this question.

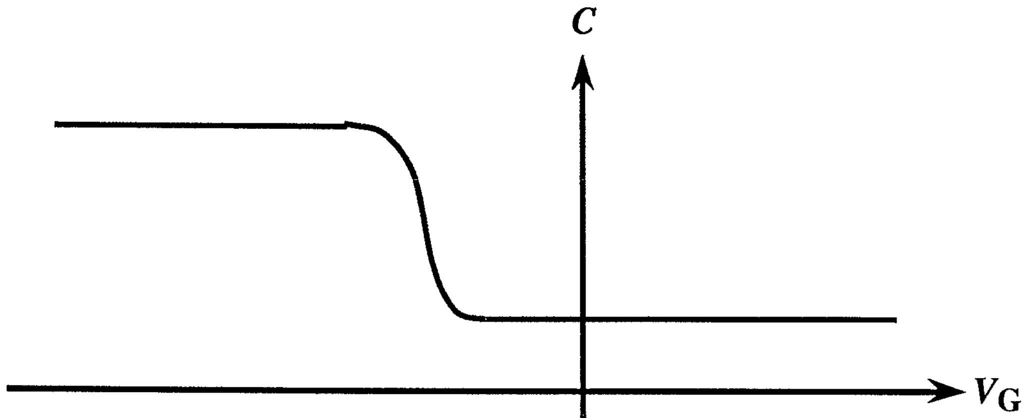
III. Nonideal MOS

4pts (11) Identify the physical cause of the listed oxide charges. Place the appropriate letter in the box preceding the charge.

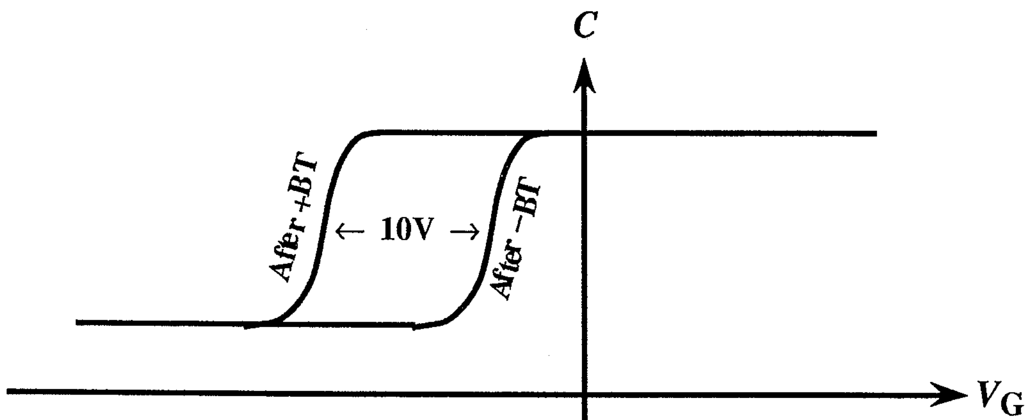
Oxide Charge	Physical Cause
☐ Mobile ion charge	(a) Phosphorus ions (P^+)
☐ Fixed charge	(b) Sodium ions (Na^+)
☐ Interfacial traps	(c) Hydrogen ions (H^+)
☐ Apparent fixed charge resulting from ionizing radiation	(d) Dangling bonds at the Si surface
	(e) Trapped electrons
	(f) Ionized Si waiting to be oxidized
	(g) Ionized oxygen waiting to be oxidized
	(h) Trapped holes

6pts (12) A researcher fabricates two MOS-C's which are *identical except for different oxide thicknesses*. Specifically, $x_{o1} = 0.05\mu m$ and $x_{o2} = 0.1\mu m$. The devices are free of mobile charges and interfacial traps. However, the Q_F (fixed charge) and ϕ_{MS} are both non-zero. Device #1 exhibits a flat band voltage of –2V and device #2 exhibits a flat band voltage of –3V. Determine ϕ_{MS} and Q_F.

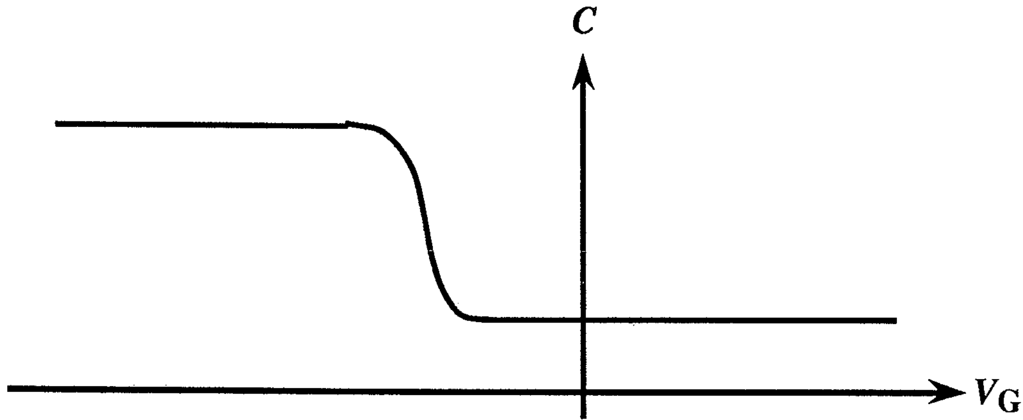
6pts (13) The as-fabricated C–V characteristic derived from an MOS-C is shown below. After fabrication, *precisely one-half* of the gate area is exposed to ionizing radiation which increases the apparent fixed charge (Q_F) in the exposed half of the device. The increase in interface trap density caused by the irradiation is negligible. Sketch the expected form of the C–V characteristic after irradiation. (Your sketch must appear on the same set of coordinates as the pre-irradiation characteristics. Also, it may be advisable to include a few words of explanation to forestall a misinterpretation of your sketch.)
HINT: Think capacitors in parallel.



6pts (14) The C–V characteristics of an MOS-C after positive bias-temperature (+BT) stressing and after negative bias-temperature (–BT) stressing are shown below. Assuming the mobile ion charge is all piled-up right at the oxide-semiconductor interface after +BT stressing, and all piled-up right at the metal-oxide interface after –BT stressing, determine the total mobile ion charge/cm^2 (Q_M) inside the MOS-C. The MOS-C has an oxide thickness of $x_o = 0.1\mu$m.



6pts (15) The C–V characteristics of an MOS-C are measured before and after performing a post-metallization anneal to eliminate interfacial traps. The AFTER C–V characteristics exhibited by the device is traced below. Assuming *acceptor-like* interfacial traps, sketch the C–V characteristics of the device BEFORE annealing on the same set of coordinates. (It may be advisable to include a few words of explanation to forestall a misinterpretation of your sketch.)



4pts (16) By circling the appropriate letters, identify those procedures which are commonly used to adjust the threshold voltage of MOSFETs.

(a) Forward bias the drain relative to the back contact.

(b) Employ {110} oriented substrates.

(c) Implant a precisely controlled number of either boron or phosphorus ions into the near-surface region of the semiconductor.

(d) Irradiate the MOSFET to increase Q_F.

(e) Use chrome-gold gate material to decrease ϕ_{MS}.

(f) Reverse bias the back contact of the MOSFET relative to the source.

IV. Modern FET Structures

Answer the following questions as concisely as possible.

4pts (17) What is the physical difference between a "buried-channel" MOSFET and a standard MOSFET?

4pts (18) Indicate what the following stand for:

LDD...

MODFET...

4pts (19) Describe what happens inside a MOSFET affected by the hot carrier phenomenon known as "oxide charging".

(Continued)

6pts (20) Qualitatively explain why the magnitude of the threshold voltage in a narrow-width MOSFET increases with decreasing channel width.