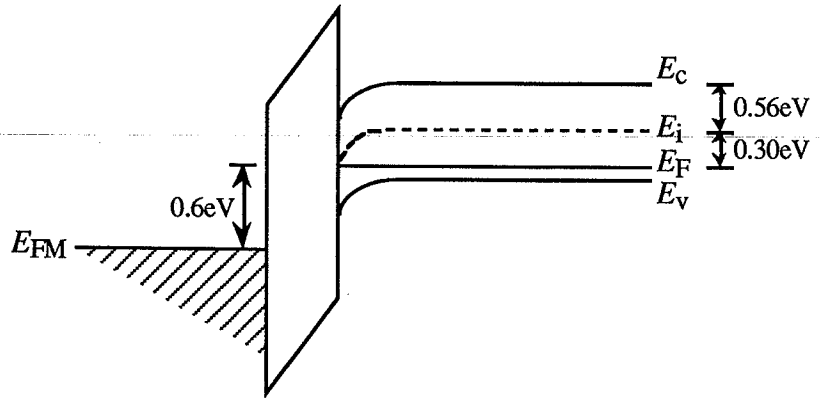
Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**C**
Test:	**C11**
Type:	**Closed Book, Closed Notes**
Note:	**Available Info/Equation Sheets**

The 25 questions have an equal weighting of 4 points each.

I. MOS Fundamentals

A dimensioned energy band diagram for an *ideal* MOS-C under a specific gate bias is reproduced below. The device is maintained at $T = 300\text{K}$, $kT/q = 0.026\text{V}$, $n_i = 10^{10}/\text{cm}^3$, $K_S = 11.8$, and $K_O = 3.9$. Also note that $E_i = E_F$ at the surface of the semiconductor. Use the energy band diagram and the specified parametric values in answering Questions 1–10.



(1) Do equilibrium conditions prevail *inside the semiconductor*?

(a) Yes (b) No (c) Can't be determined

(2) The semiconductor is doped...

(a) *n*-type (b) *p*-type (c) Can't be determined

(3) ϕ_F = ?

(a) –0.30V (b) –0.26V (c) 0.26V (d) 0.30V (e) 0.86V

(4) ϕ_S = ?

(a) –0.60V (b) –0.30V (c) 0.30V (d) 0.60V (e) 0.86V

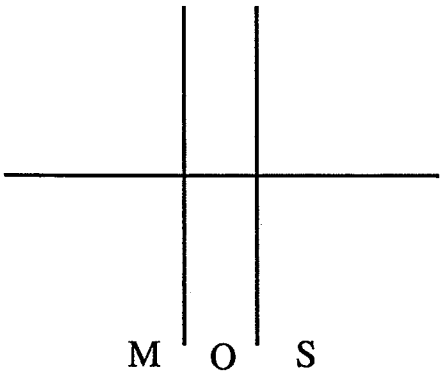
(5) V_G = ?

(a) –1.16V (b) –0.6V (c) 0 (d) 0.6V (e) 0.9V

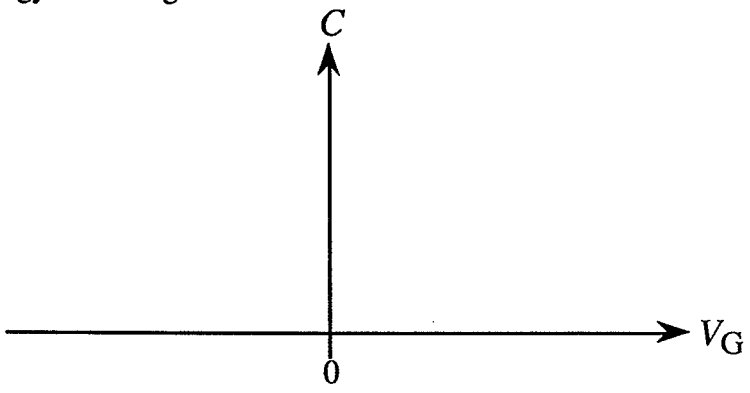
(6/7) x_o = ? (x_o is the oxide thickness.)

(a) 0.05μm (b) 0.10μm (c) 0.15μm (d) 0.20μm (e) 0.25μm

(8) Draw the *block charge diagram* corresponding to the state pictured in the energy band diagram. (For reference purposes, include the maximum equilibrium depletion width, W_T, on your diagram.)



(9) Sketch the general shape of the *low-frequency C–V* characteristic to be expected from the given MOS-C. Place an × on the *C–V* characteristic at the point which corresponds to the state pictured in the energy band diagram.

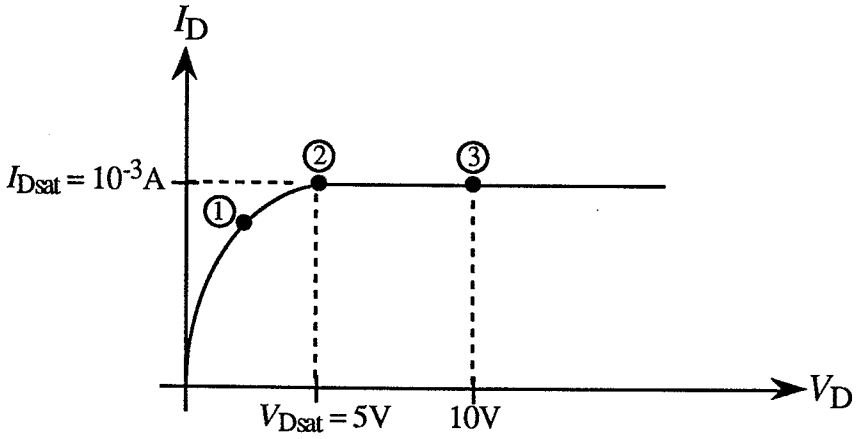


(10) For the specific bias point pictured in the energy band diagram, which of the following is the correct expression for the capacitance exhibited by the structure?

(a) $C = C_O$ (b) $C = \dfrac{C_O}{1+\dfrac{K_O W_T}{K_S x_o}}$ (c) $C = \dfrac{C_O}{\sqrt{1+\dfrac{V_T}{2V_\delta}}}$ (d) $C = \dfrac{C_O}{1+\dfrac{1}{\sqrt{2}}\dfrac{K_O W_T}{K_S x_o}}$ (e) $C = \dfrac{C_O}{\sqrt{1+\dfrac{V_T}{V_\delta}}}$

II. Basic MOSFET

An I_D–V_D characteristic derived from an ideal MOSFET is shown below. Note that $I_{Dsat} = 10^{-3}$A and $V_{Dsat} = 5$V for the given characteristic. Answer Questions 11-18 making use of the *Square-Law* theory and the information conveyed in the figure.



(11/12) Carefully sketch the inversion layer and depletion region inside the MOSFET corresponding to point (1) on the pictured characteristic. *Show and label all parts of the transistor.*

(13) Given a turn-on voltage of $V_T = 1$V, what is the gate voltage one must apply to the MOSFET gate to obtain the pictured characteristic?

V_G =

(14) If $K_O = 3.9$ and $x_o = 0.1\mu$m, what is the inversion-layer charge/cm^2 at the drain end of the channel when the MOSFET is biased at point (2) on the characteristic?

$Q_N(L)$ =

(15) Suppose the gate voltage is readjusted so that $V_G - V_T = 3V$. For the new condition, determine I_D if $V_D = 4V$.

(a) 2.5×10^{-4}A (b) 3.6×10^{-4}A (c) 6.0×10^{-4}A (d) 10^{-3}A

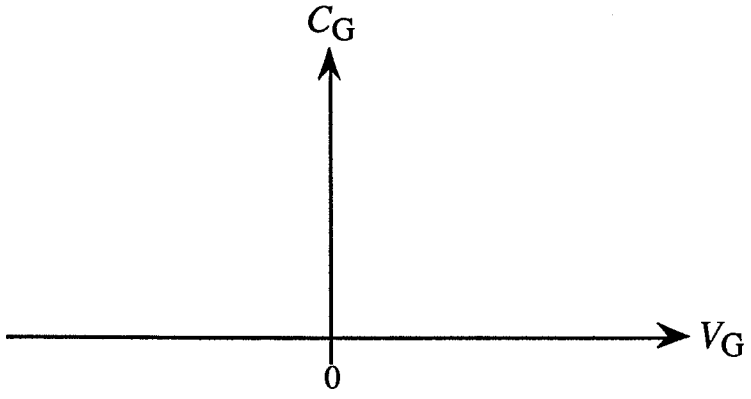
(16) Determine g_d if the quiescent operating point of the MOSFET is point (3) on the pictured characteristic. [Note: the unit for conductance is Siemens (S).]

(a) 0 (b) 10^{-4} S (c) 2×10^{-4} S (d) 4×10^{-4} S

(17) Determine g_m if the quiescent operating point of the MOSFET is point (3) on the pictured characteristic.

(a) 0 (b) 10^{-4} S (c) 2×10^{-4} S (d) 4×10^{-4} S

(18) If $V_D = 0$ (i.e., the drain is shorted to the source and back), sketch the general shape of the C_G (gate capacitance) versus V_G characteristic to be expected from the MOSFET.



III. Modern FET Structures

Answer the following questions as concisely as possible.

(19) Small-dimension effects are generally undesirable and are minimized or avoided in commercial structures through the proper scaling of device dimensions or modifications in device design.

(a) True (b) False

(20) Qualitatively explain why the magnitude of the threshold voltage in a short-channel MOSFET descreases with decreasing channel length.

(21) Explain how punch-through can lead to abnormal behavior in short-channel MOSFETs.

(22) What is "velocity saturation" and how does it affect the observed MOSFET I_D–V_D characteristics?

(Continued)

(23) What is special about an LDD transistor?

(24) What is a "DMOS" structure?

(25) What is the difference between a MODFET and a HEMT?