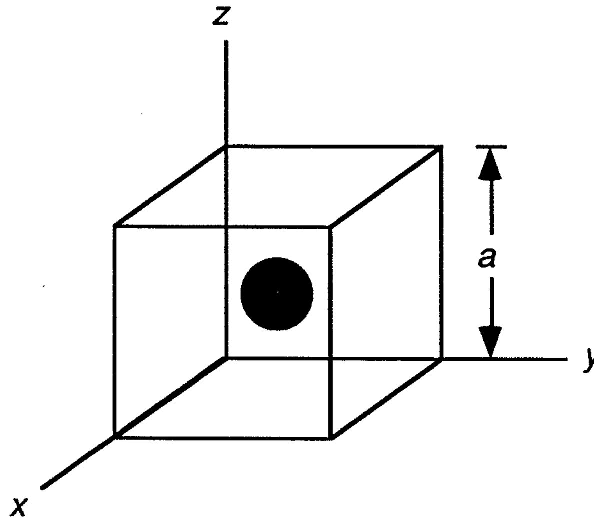
Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**C**
Test:	**C12**
Type:	**Closed Book, Closed Notes**
Note:	**Available Info/Equation Sheets**

The test has a 200 point maximum. Questions numbered 1-20 have an equal weighting of 5 points each. The weightings of the remaining questions are noted adjacent to the question numbers.

■ A crystalline lattice is characterized by the cubic unit cell pictured below. The cell has a single atom positioned at the center of the cube. Refer to the unit cell in answering Questions (1)–(4).



(1) What is the standard name of the lattice characterized by the above unit cell?

(a) Simple cubic
(b) Body-centered cubic
(c) Face-centered cubic
(d) Diamond
(e) Center cubic

(2) The density (number per unit volume) of atoms in the crystal is:

(a) a^3
(b) $1/a^3$
(c) $8/a^3$
(d) $a^3/8$

(3) Suppose the crystal has a (110) surface plane. The number of atoms per unit area whose centers lie on the (110) surface plane is:

(a) a^2
(b) $1/a^2$
(c) $a^2/\sqrt{2}$
(d) $1/(\sqrt{2}\, a^2)$
(e) $\sqrt{2}\,/a^2$
(f) $1/(\sqrt{3}\, a^2)$

(4) What are the Miller indices of the direction vector which passes through the center of the atom in the unit cell?

(a) [100]
(b) [110]
(c) [111]
(d) (100)
(e) (110)
(f) (111)

(5/6) In a nondegenerate Germanium sample maintained under equilibrium conditions at room temperature it is known that $n_i = 10^{13}/\text{cm}^3$, $n_o = 2p_o$, and $N_A = 0$.

- Determine n_o.
  - (a) $n_o = 0.707 \times 10^{13}/\text{cm}^3$
  - (b) $n_o = 10^{13}/\text{cm}^3$
  - (c) $n_o = 1.414 \times 10^{13}/\text{cm}^3$
  - (d) $n_o = 1.732 \times 10^{13}/\text{cm}^3$
  - (e) $n_o = 2 \times 10^{13}/\text{cm}^3$

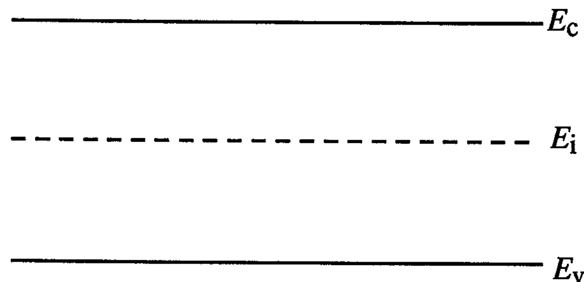
- Relate n_o to the donor doping concentration (N_D).
  - (a) $n_o = N_D/2$
  - (b) $n_o = N_D$
  - (c) $n_o = 3N_D/2$
  - (d) $n_o = 2N_D$
  - (e) $n_o = N_D/2 + \sqrt{2}\, N_D$

(7) On the equilibrium energy band diagram included below:

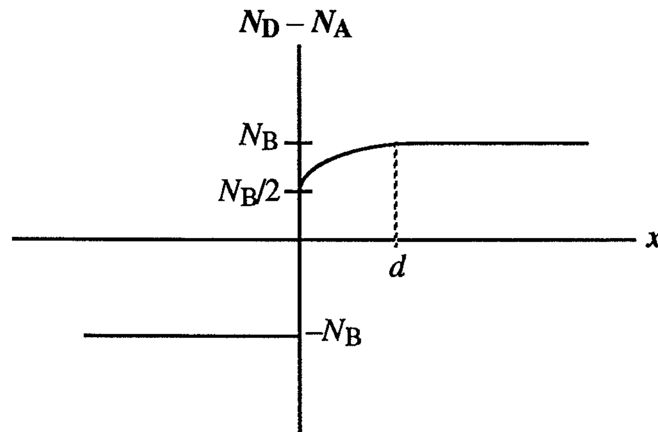
(a) Add and appropriately label a solid line which identifies the sample to be a *degenerately* doped *n*-type semiconductor.

(b) Use a dashed line to indicate the approximate energy positioning of R–G centers. Label the dashed line E_T.

(c) Use a dashed line labeled E_A to indicate the approximate energy position of acceptor levels.

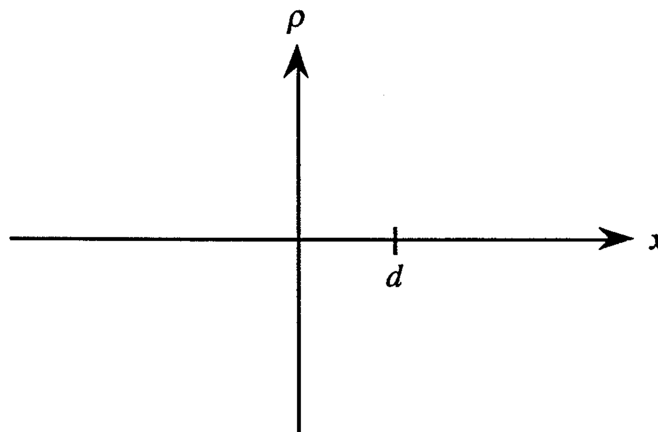


■ The doping profile inside a Si *pn* junction diode maintained at room temperature is pictured below. In the statement of Questions (8)–(12) x_n is understood to be the depletion width on the *n*-side of the junction.



$$N_D - N_A = \begin{cases} -N_B & \ldots x < 0 \\ \dfrac{N_B}{2}\left[1 + \sqrt{\dfrac{x}{d}}\right] & \ldots 0 < x \le d \\ N_B & \ldots x \ge d \end{cases}$$

(8) Invoking the depletion approximation, and assuming $x_n > d$, sketch ρ versus x inside the diode.



(9) Determine the built-in voltage assuming $x_n > d$ under equilibrium conditions.

(a) $V_{bi} = (kT/q)\ \ln(N_B/n_i)$

(b) $V_{bi} = (2kT/q)\ \ln(N_B/n_i)$

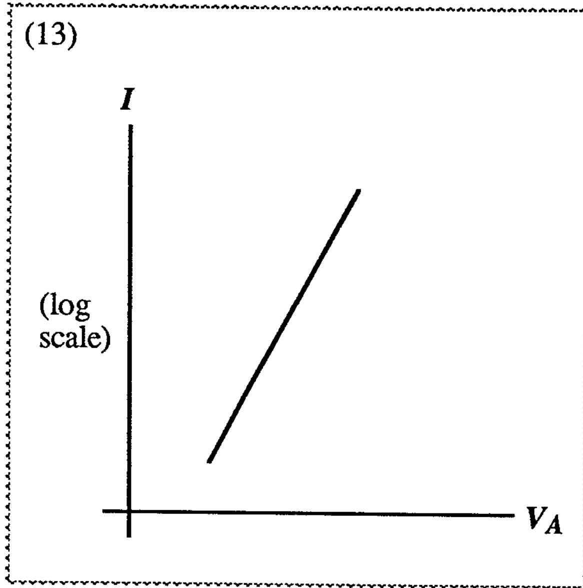
(c) $V_{bi} = (kT/q)\ \ln(N_B/2n_i)$

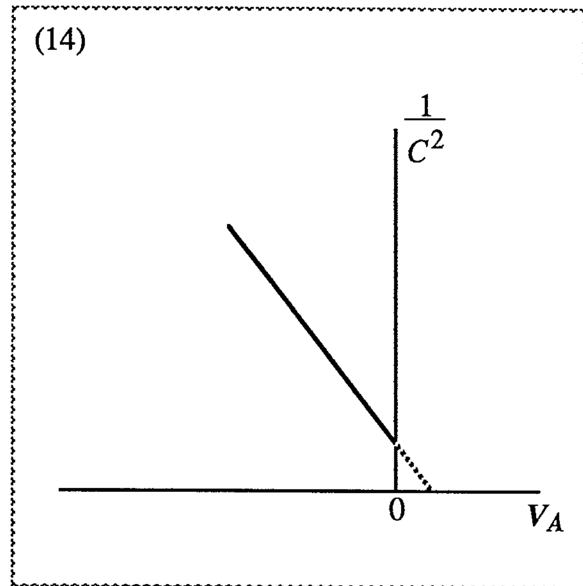
(d) $V_{bi} = (kT/q)\ \ln(2N_B/n_i)$

(10–12) If $x_n > d$ for all biases of interest, and invoking the depletion approximation, derive an expression for the electric field ($\mathcal{E}$) in the $0 \le x \le d$ region. *Show all your work on this page and clearly identify your final answer.*

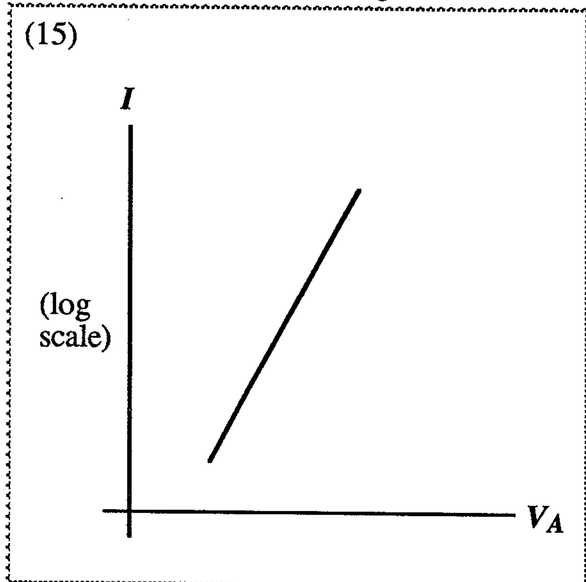
■ The forward-bias current-voltage (I–V_A) and the reverse-bias capacitance-voltage (C–V_A) data from a p^+-n step junction diode are presented below. Take the I–V_A characteristics to be those of an *ideal* diode.

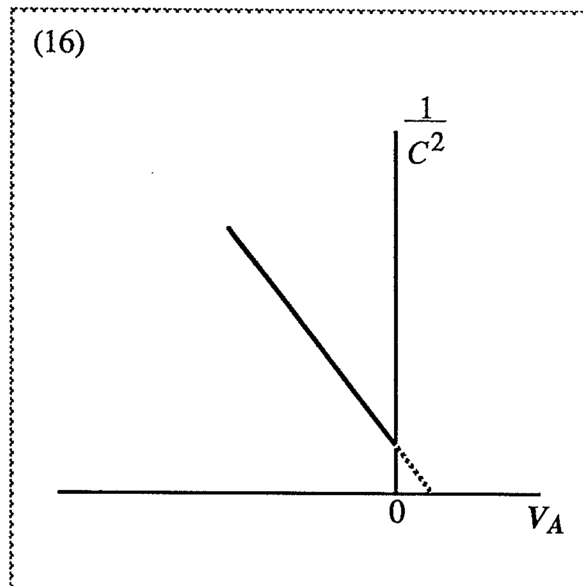
— Using a dashed line, roughly indicate what effect an increased n-side doping (increased N_D) would have on the observed characteristics. Write "NO EFFECT" if the characteristic remains unchanged.



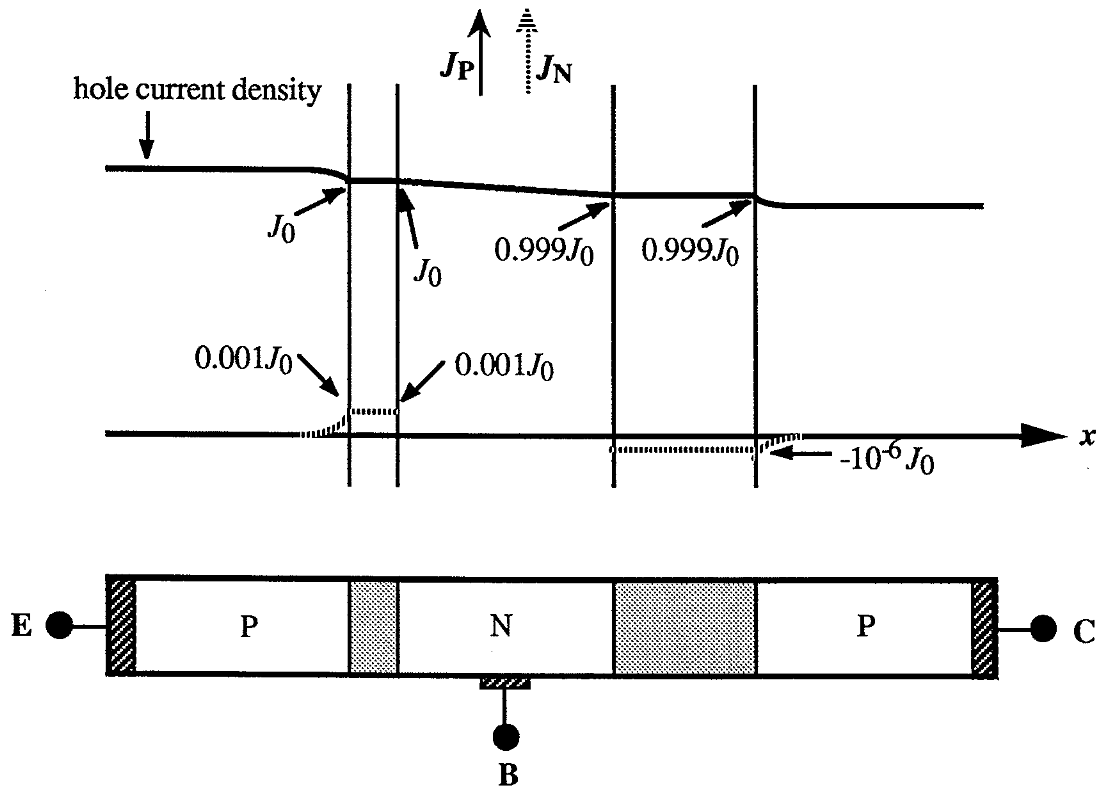


— Using a dashed line, roughly indicate what effect an *increase* in the R–G center concentration (N_T) would have on the observed characteristics. Write "NO EFFECT" if the characteristic remains unchanged.





■ The electron and hole current densities in a BJT biased in the forward-active mode are plotted below. All current densities are referenced to J_0, the hole current density injected into the base. Use the current density plot in answering Questions (17)–(20).



(17) Determine the base transport factor.

(a) 0.001 (c) 0.998 (e) 1.000
(b) 0.002 (d) 0.999 (f) 1.001

(18) Determine the emitter efficiency.

(a) 0.001 (c) 0.998 (e) 1.000
(b) 0.002 (d) 0.999 (f) 1.001

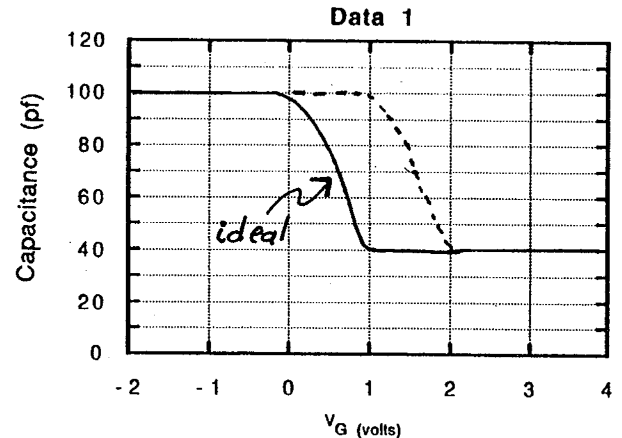
(19) Determine the common emitter d.c. gain.

(a) 0.998 (c) 1.000 (e) 500
(b) 0.999 (d) 1.001 (f) 1000

(20) From the current density plot one concludes the recombination–generation current arising from the depletion regions

(a) is negligible (c) $\cong 0.001\ J_0$
(b) $\cong 10^{-6}\ J_0$ (d) cannot be determined from the information provided.

(24 pts) 21. Shown as a solid line is the CV characteristic of an ideal MOS-C. The dashed line is the CV characteristic of an MOS-C which is identical in every way to the ideal MOS-C except that it has a "fixed" charge at the Si–SiO_2 interface. The oxide thickness of the MOS-C is 1.00×10^{-5}cm^2, $K_{ox}\epsilon_0 = 3.9\,\epsilon_0$, and $K_s\epsilon_0 = 11.8\,\epsilon_0$.



(3 pts) 21–1) Is the semiconductor n- or p-type?

(3 pts) 21–2) Are these high or low frequency CV characteristics?

(6 pts) 21–3) What is the area of the gate?

A) 2.9×10^{-3}cm^2

B) 3.4×10^{2}cm^2

C) 9.5×10^{-4}cm^2

D) none of the above

(6 pts) 21–4) What is the value of the "fixed" charge density at the Si–SiO_2 interface which results in the dashed CV characteristics?

A) $-3.45 \times 10^{-8}\,\frac{\text{coul}}{\text{cm}^2}$

B) $3.45 \times 10^{-8}\,\frac{\text{coul}}{\text{cm}^2}$

C) $-1.04 \times 10^{-7}\,\frac{\text{coul}}{\text{cm}^2}$

D) $+1.04 \times 10^{-7}\,\frac{\text{coul}}{\text{cm}^2}$

E) none of the above

(6 pts) 21–5) The capacitors whose CV characteristics are shown in the figure have aluminum gates. The metal work function of aluminum is 4.1 eV. We now replace the aluminum gates with gold, whose metal work function is 5.0 eV. What does the flat band voltage shift to for the MOS-C in the figure whose flat band voltage is originally $V_{FB} = 0.0$ volts?

A) –0.9 V

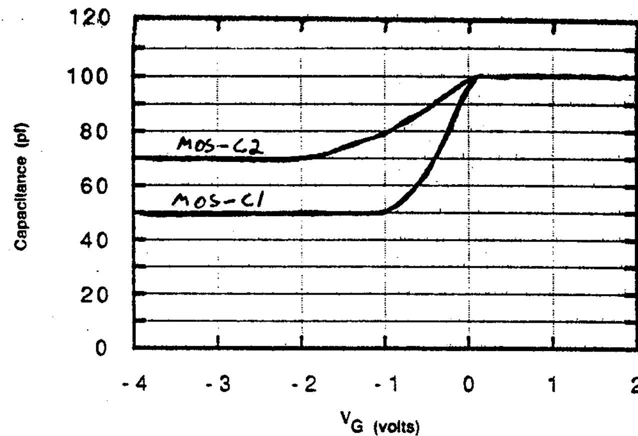
B) 0.9 V

C) 5.0 V

D) –5.0 V

E) gold is too expensive to use as the gate of an MOS capacitor.

(15 pts) 22. You are given the CV characteristics shown for two ideal MOS-capacitors, MOS-C1 and MOS-C2. The gate areas of the two capacitors are the same. Answer the following true false questions.



(3 pts) 22-1) The oxide thickness of MOS-C2 is greater than that of MOS-C1. T F

(3 pts) 22-2) The doping in the semiconductor of MOS-C2 is greater than that of MOS-C1. T F

(3 pts) 22-3) If the oxide thickness of MOS-C2 were increased, V_{T2} would shift to a more negative voltage. T F

(3 pts) 22-4) Bias-temperature stressing is a test to determine the breakdown characteristics of the oxide of an MOS-capacitor T F

(3 pts) 22-5) In an MOS-capacitor equilibrium biased into inversion, the source of the inversion charge is thermal generation T F

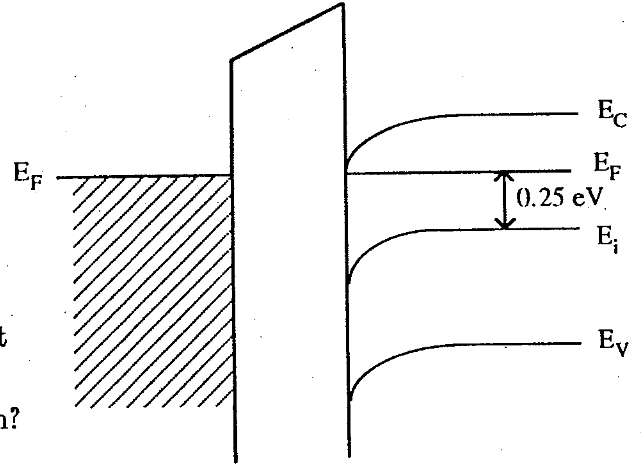
(6 pts) 23. Deep depletion is,

A) a condition where the depletion region has punched through to the back of the substrate

B) a condition where the electric field in the semiconductor is large enough to cause avalanching

C) a nonequilibrium condition where there is a deficit of minority carriers in the inversion layer and a depletion width in excess of the equilibrium value.

(9 pts) 24. You are given the shown energy band diagram for an MOS-capacitor.



(3 pts) 24–1) What is the bias from gate to substrate?

A) 0 volts

B) 0.5 volts

C) –0.5 volts

D) none of the above

(6 pts) 24–2) Assuming the substrate is grounded, what will be the voltage at the Si–SiO_2 interface at the point of onset of inversion?

A) –0.25 V

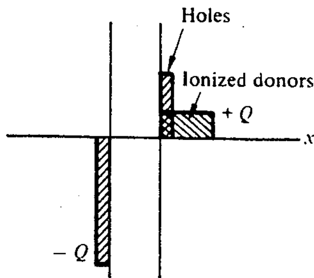
B) +0.25 V

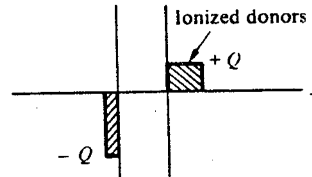
C) –0.5 V

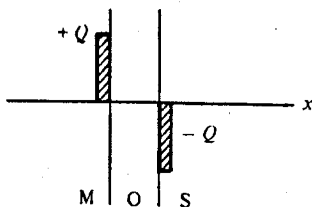
D) +0.5 V

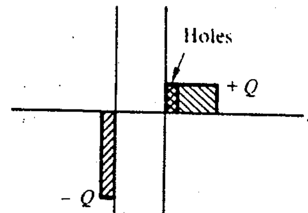
(8 pts) 25. Given the following block charge diagrams for an MOS-capacitor identify them by placing the appropriate letter in the box,

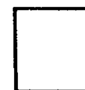
A - inversion
B - accumulation
C - onset of inversion
D - depletion











(6 pts) 26. The effective mobility of electrons in an inversion layer of an MOSFET decreases with increased gate bias because

A) There are more electrons in the channel which impedes their motion from source to drain.

B) The increased voltage heats the MOSFET causing an increase in scattering due to lattice vibration.

C) There is an increase in electric field which drifts the electrons into the Si–SiO_2 interface where they scatter.

D) None of the above.

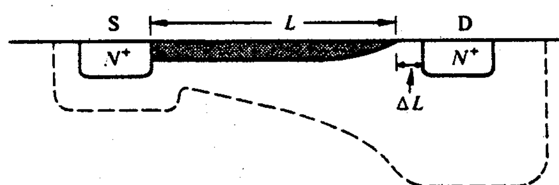
(8 pts) 27. Identify the phases of MOSFET operation depicted in the figure below by placing the appropriate letter in the box provided. The MOSFET is an n-channel enhancement mode device

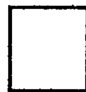
A) pinch-off, $V_D = V_{DSAT}$

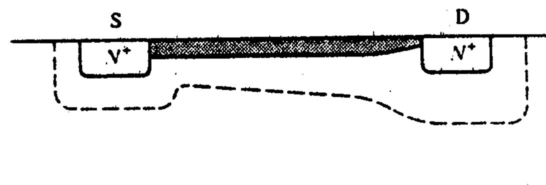
B) post pinch-off, $V_D > V_{DSAT}$

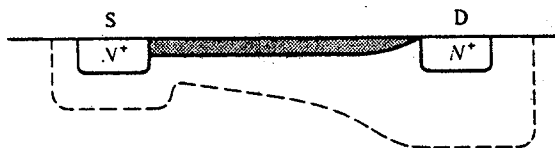
C) channel inversion with $V_D = 0$

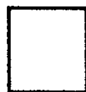
D) channel inversion with $0 < V_D < V_{DSAT}$

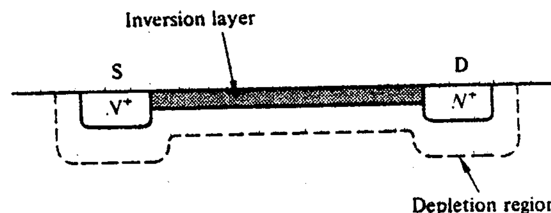


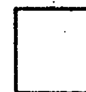




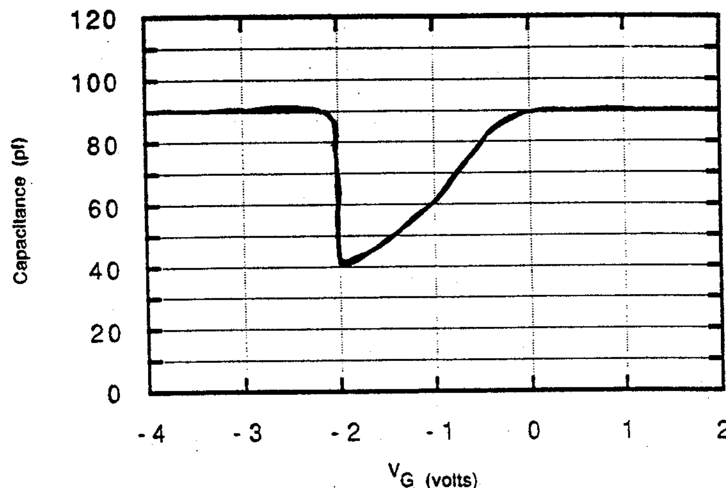








(18 pts) 28. You are given the shown $C_G - V_G$ characteristic of a MOSFET.



(3 pts) 28–1) Is the MOSFET an enhancement or depletion mode device?

(3 pts) 28–2) Is the MOSFET an n-channel or p-channel device?

(6 pts) 28–3) Invoking the square law theory, what is V_{DSAT} if the gate voltage is −5 volts?

A) −3 volts

B) 0 volts

C) −2 volts

D) −7 volts

E) +3 volts

F) +2 volts

(6 pts) 28–4) The same CV curve shown for the MOSFET is obtained whether one is using a very high or very low ac signal frequency. The reason is,

A) the generation-recombination rate must be fast

B) the source of the inversion charge is the source and drain contacts which can add or remove carriers quickly from the inversion layer

C) the substrate must be thin so that inversion charge can be added or removed quickly from the back contact

D) it is impossible to have the same CV characteristic at low and high ac signal frequencies

(6 pts) 29. The major flaw with the square law theory of the MOSFET $I_D - V_D$ relationship is

A) it is assumed that the depletion region width is fixed at W_T from source to drain even when $V_D \neq 0$.

B) a poor approximation to the effective mobility, $\bar{\mu}_n$, is used.

C) the finite generation-recombination rate of the inversion layer is not taken into account.

D) there are no major flaws with the square law theory.