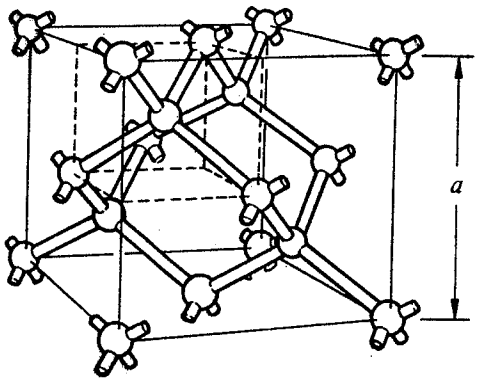
Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**C**
Test:	**C14**
Type:	**Closed Book, Closed Notes**
Note:	**Available Info/Equation Sheets**

The 40 questions to be answered have an equal weighting of 2.5 points each.

[1 - 4] The diamond lattice unit cell is reproduced below. For Si at room temperature a = 5.43 X 10^{-8} cm.



(1) The number of Si atoms/cm^3 at room temperature is:

(a) 2.50 X 10^{22}/cm^3 (c) 5.00 X 10^{22}/cm^3

(b) 6.25 X 10^{21}/cm^3 (d) 3.00 X 10^{22}/cm^3

(2) The number of Si atoms/cm^2 on a {100} surface is:

(a) 5.09 X 10^{14}/cm^2 (c) 3.39 X 10^{14}/cm^2

(b) 6.78 X 10^{14}/cm^2 (d) 1.36 X 10^{15}/cm^2

(3) Donor doping of Si is accomplished by replacing Si atoms in the pictured lattice with

(a) column III atoms such as Boron

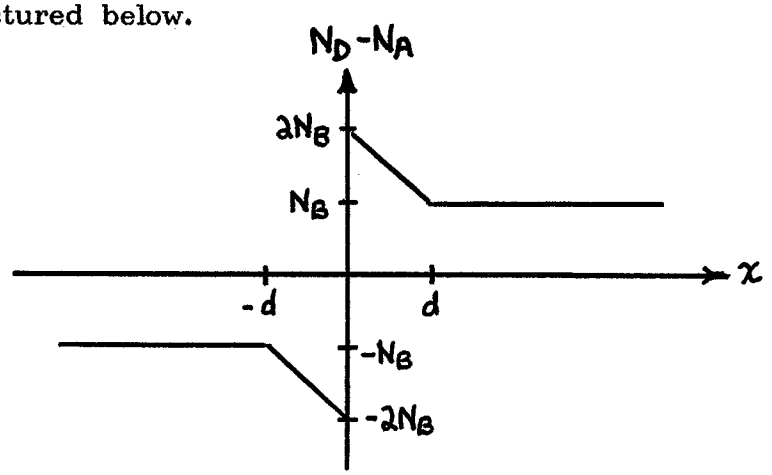
(b) column IV atoms such as Germanium

(c) column V atoms such as Phosphorus

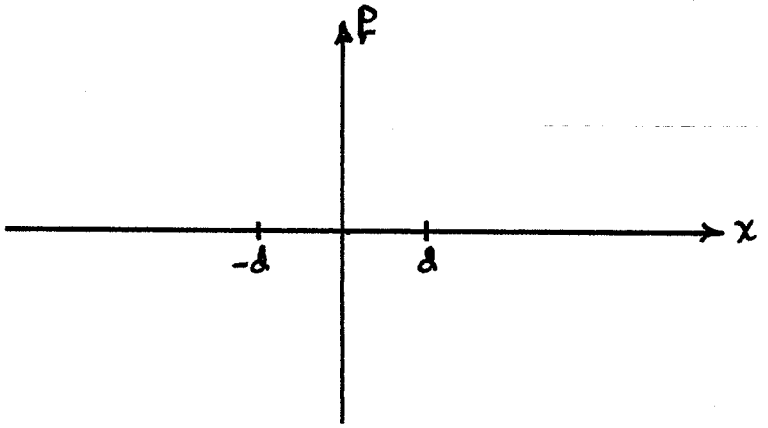
(d) None of the above; dopants occupy sites between the pictured atoms.

(4) Using the diamond lattice unit cell reproduced above, indicate how one visualizes an R-G center.

[5 - 7] The doping profile inside a Si pn junction diode maintained at room temperature is pictured below.



(5) Invoking the depletion approximation, sketch ρ versus x inside the diode. Assume $-x_p < -d$ and $x_n > d$.



(6) Determine the built-in voltage assuming $-x_p < -d$ and $x_n > d$ under equilibrium conditions.

(a) $V_{bi} = (kT/q)\ln(N_B/n_i)$

(b) $V_{bi} = (2kT/q)\ln(N_B/n_i)$

(c) $V_{bi} = (4kT/q)\ln(N_B/n_i)$

(d) $V_{bi} = (kT/q)\ln(4N_B^2/n_i^2)$

(7) Which of the following statements is INCORRECT?

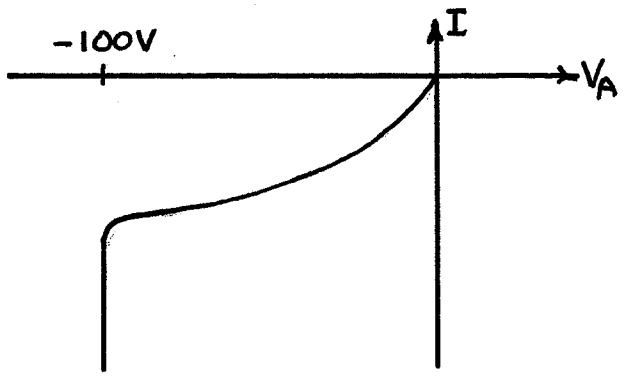
(a) Because of the doping symmetry, a plot of the electric field (ℰ) versus position is expected to be symmetrical about x = 0.

(b) The maximum magnitude of the electric field occurs at x = 0.

(c) The electric field will be discontinuous at x = 0.

(d) For $x < -d$ and $x > d$ one expects a linear ℰ vs. x relationship.

[8 - 11] The reverse bias I - V_A characteristic derived from a Si pn junction diode maintained at room temperature is sketched below. Answer the questions which follow using the information conveyed in the figure.



(8) Breakdown in the diode is caused by

(a) The Early effect

(b) Avalanche multiplication

(c) The Zener process

(d) Can't be determined

(9) The dominant current component flowing in the diode under reverse bias conditions is:

(a) The diffusion current

(b) The ideal diode current

(c) The R-G current

(d) The channel current

(10) If $-100V \leq V_A \leq -$(few kT/q), the junction capacitance (C_J) of the diode will be inversely proportional to the reverse bias current.

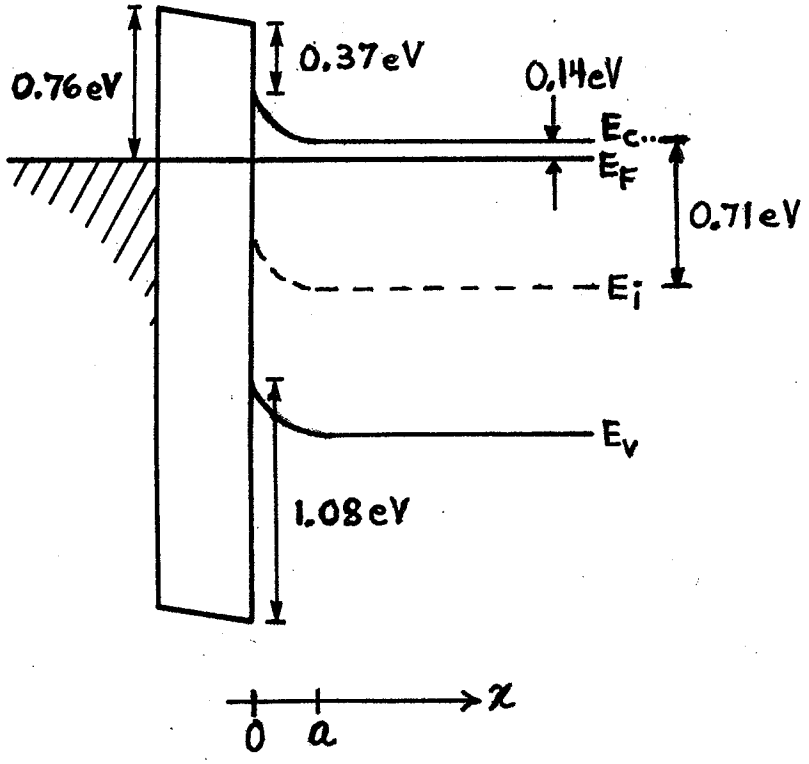
(a) True (b) False (c) No way to determine.

(11) A decrease in the carrier lifetime would simultaneously (i) increase the magnitude of the reverse bias current shown above, and (ii) reduce the storage delay time exhibited by the diode in switching applications.

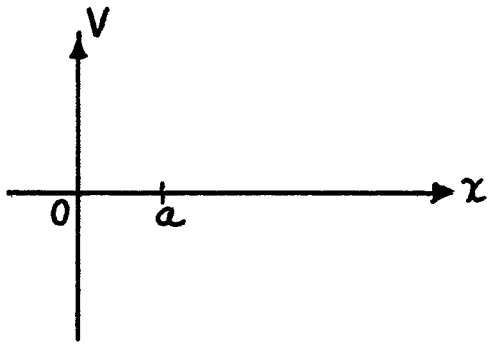
(a) True (b) False (c) No way to determine.

[12 - 22] A totally dimensioned energy band diagram for an M"O"S-C recently fabricated in our laboratory is shown below. (The "O" is actually ZnSe and the semiconductor is GaAs.) The device is maintained at T = 300K, $kT/q = 0.0258V$, $n_i = 2.25 \times 10^6/cm^3$, $K_S = 12.85$, $K_O = 9.0$, and $x_o = 10^{-5}$ cm. It has also been established that $Q_{IT} = 0$, $Q_F = 0$, and $Q_M = 0$.

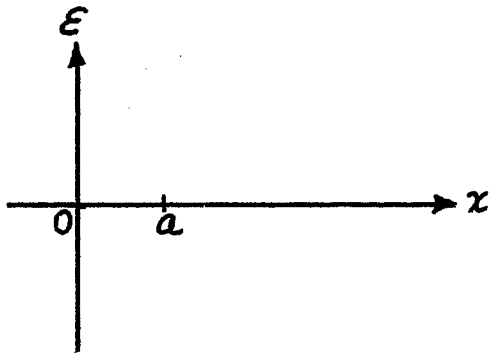
Use the cited energy band diagram and the given information in answering questions 12 - 22.



(12) Sketch the electrostatic potential (V) inside the semiconductor as a function of position. (Let V = 0 in the semiconductor bulk.)



(13) Roughly sketch the electric field inside the semiconductor as a function of position.



(14) Do equilibrium conditions prevail <u>inside the semiconductor</u>?

(a) Yes (b) No (c) Can't be determined

(15) The semiconductor is degenerate:

(a) Near x = 0. (b) For $x \geq a$ (c) Nowhere

(16) N_D = ?

(a) $3.93 \times 10^{19}/cm^3$ (c) $1.00 \times 10^{15}/cm^3$

(b) $8.85 \times 10^{15}/cm^3$ (d) $5.12 \times 10^{8}/cm^3$

(17) V_G = ?

(a) -0.57V (b) -0.39V (c) 0V (d) 0.39V (e) 0.57V

(18) For the pictured condition the M"O"S-C is

(a) accumulated (b) depleted (c) inverted

(d) biased at the depletion-inversion transition point.

(19) What is the metal-semiconductor workfunction difference (ϕ_{MS})?

(a) -0.39V (b) -0.25V (c) 0V (d) 0.25V (e) 0.39V

(20) What voltage must be applied to the gate to achieve flat-band conditions?

(a) -0.39V (b) -0.25V (c) 0V (d) 0.25V (e) 0.39V

(21) Invoking the delta-depletion approximation, determine the normalized small signal capacitance, C/C_0, at the pictured bias point.

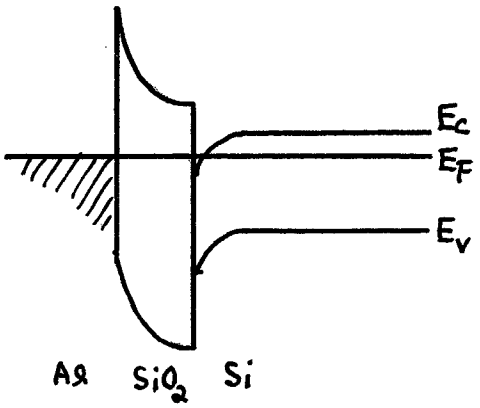
(a) 0.25 (b) 0.41 (c) 0.58 (d) 1.00

(22) As noted in the energy band figure, a is the distance from the "oxide"-semiconductor interface to the quasi-neutral semiconductor "bulk". Determine the length of a at the pictured bias point.

(a) $a \simeq 1.03 \times 10^{-5}$ cm (c) $a \simeq 4.28 \times 10^{-5}$ cm

(b) $a \simeq 2.06 \times 10^{-5}$ cm (d) $a \simeq 8.13 \times 10^{-5}$ cm

[23/24] The energy band diagram for an MOS-C is shown below. It is known that $Q_{IT} = 0$.



(23) From the diagram one concludes (choose one):

(a) $Q_F = 0$ (b) $Q_F \neq 0$ [Q_F is the fixed charge.]

EXPLAIN (required for credit)...

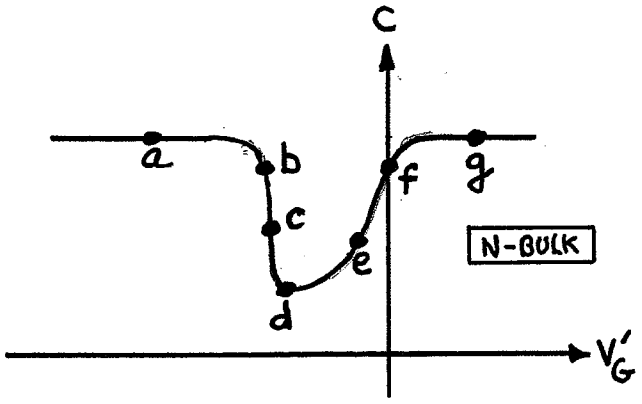
(24) From the diagram one concludes (choose one):

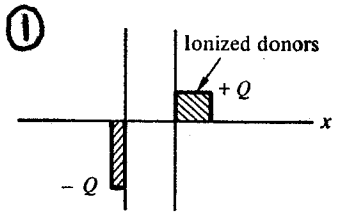
(a) $Q_M = 0$ (b) $Q_M \neq 0$ [Q_M is the mobile ion charge.]

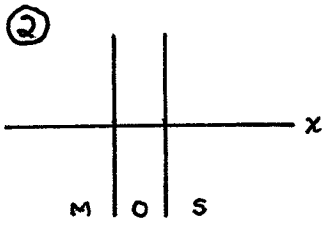
EXPLAIN (required for credit)...

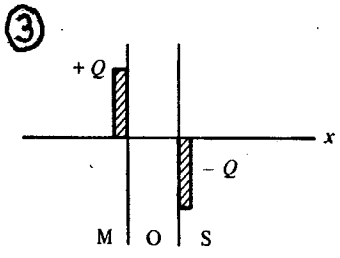
[25/26] Complete the following table making use of the ideal-structure C-V characteristic and the block charge diagrams included below the table. Specifically, for each of the biasing conditions named in the table, identify (i) the corresponding bias point(s) on the ideal MOS-C C-V characteristic employing letters (a - g) and (ii) the associated block charge diagram using a number (1 - 5).

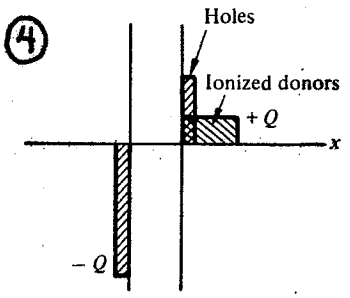
Bias Condition	Capacitance (a-g)	Block Charge Diagram (1-5)
accumulation		
depletion		
inversion		
flat band		
threshold		

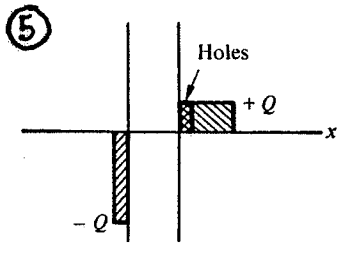












[27 - 32] A MOSFET is fabricated with $\phi_{MS} = -0.98V$, $Q_M = 0$, $Q_{IT} = 0$, $Q_F/q = 5 \times 10^{10}/cm^2$, $x_o = 5 \times 10^{-6}$ cm, $A_G = 10^{-3}$ cm^2, and $N_A = 10^{15}/cm^3$. Take T = 23°C and assume the source and substrate are always grounded.

(27) Determine the flat band gate voltage, V_{FB}.

(a) -1.49V (b) -1.10V (c) - 0.86V (d) 0V

(28/29) Determine the gate voltage at the onset of inversion, V_T.

(a) -1.01V (b) -0.30V (c) 0.80V (d) 1.31V

(30) The given MOSFET is

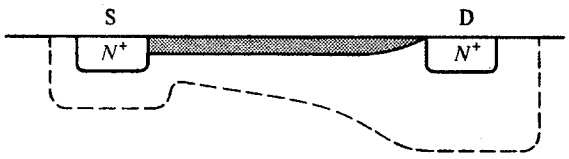
(a) an enhancement-mode MOSFET

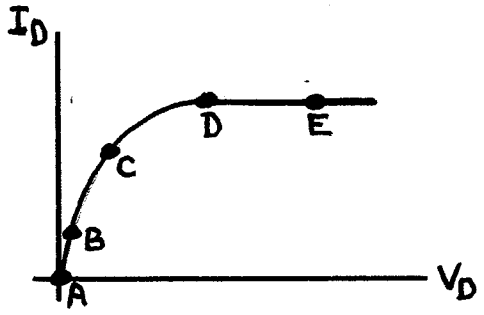
(b) a depletion-mode MOSFET

(c) a built-in channel MOSFET

(31) If the internal condition inside the MOSFET is as shown below to the left, identify the corresponding operational point on the $I_D - V_D$ characteristic at the right.

OPERATIONAL POINT (Circle One): A, B, C, D, E





(32) At $V_G - V_T = 3V$ and $V_D = 1V$ the MOSFET exhibits a drain current of $I_D = 2.5 \times 10^{-4}$ amp. Using the "Square-Law" formulation, determine the drain current if $V_G - V_T = 3V$ and $V_D = 4V$.

(a) 3.5×10^{-4} amp (c) 4.5×10^{-4} amp

(b) 4.0×10^{-4} amp (d) 1.0×10^{-3} amp

[33 - 42] MOS True or False Quiz.

Answer ONLY 8 of the following 10 questions.
Only the FIRST 8 you answer will be graded.

(33) The "field effect" is the phenomenon where carriers are accelerated by an electric field impressed parallel to the surface of the semiconductor.

(a) TRUE (b) FALSE

(34) The electron affinity (χ) of a semiconductor is the difference in energy between the vacuum level and E_c at the surface of the semiconductor.

(a) TRUE (b) FALSE

(35) The "quasi-static technique" is employed in measuring the low-frequency MOS-C C-V characteristics.

(a) TRUE (b) FALSE

(36) The nonequilibrium condition where there is a deficit of minority carriers and a depletion width in excess of the equilibrium value is referred to as "Deep Inversion".

(a) TRUE (b) FALSE

(37) The voltage shift due to mobile ions in the oxide is at a minimum when the ions are located midway between the gate and semiconductor.

(a) TRUE (b) FALSE

(38) Both the fixed charge and interfacial trap density are greater on {100} Si surfaces than on {111} surfaces.

(a) TRUE (b) FALSE

(39) The "Bulk-charge" theory for the d.c. characteristics of a MOSFET derives its name from the fact that, in this theory, one properly accounts for changes in the "bulk" or depletion region charge beneath the MOSFET channel.

(a) TRUE (b) FALSE

(40) Let g_d be the drain or channel conductance of a MOSFET. By definition, at low frequencies $g_d = \partial I_D/\partial V_G|_{V_D}$.

(a) TRUE (b) FALSE

(41) The mobility of carriers in surface inversion layers or channels is typically lower than the bulk mobility of the same carriers because of the added scattering associated with the depletion region charge.

(a) TRUE (b) FALSE

(42) In modern-day MOS structures the "M" in MOS is often heavily-doped polycrystalline Si.

(a) TRUE (b) FALSE