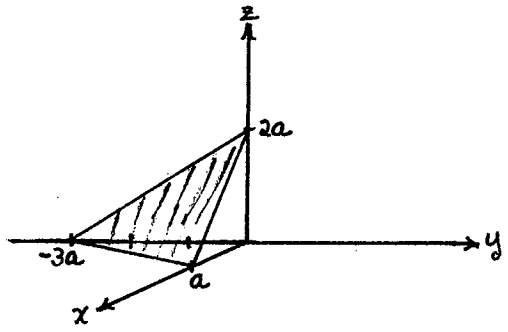
Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**C**
Test:	**C15**
Type:	**Closed Book, Closed Notes**
Note:	**Available Info/Equation Sheets**

The 40 questions to be answered have an equal weighting of 2.5 points each.

[1] What is a semiconductor? (A short essay-type answer is required here.) Do NOT give examples.

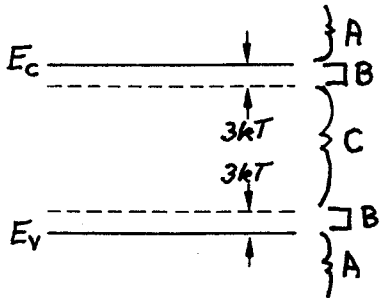
[2] Given:



Determine the Miller indices of the pictured crystalline plane.

(a) $(6\ \bar{2}\ 3)$
(b) $(1\ \bar{3}\ 2)$
(c) $(1, 1/3, 1/2)$
(d) $(1\ \bar{2}\ 3)$

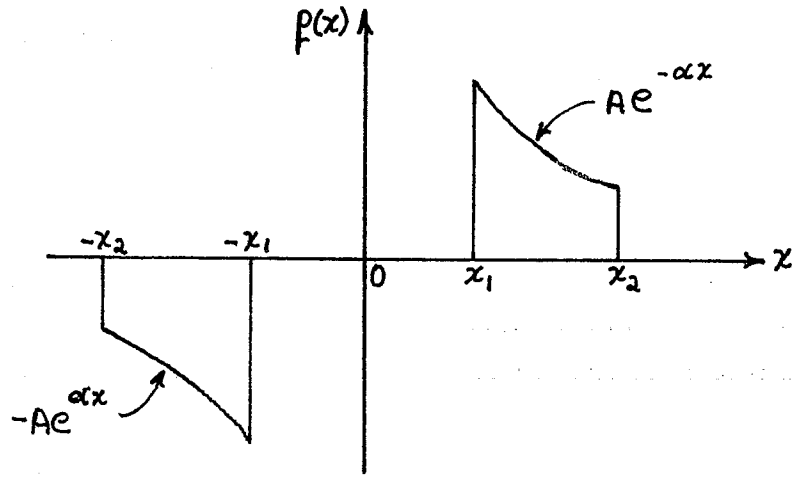
[3] Let the energy regions A, B, and C be defined as shown below.



A semiconductor is considered degenerate if the Fermi level lies in region(s)?

(a) A
(b) B
(c) C
(d) A and B
(e) B and C

[4/5] The charge density distribution shown below is to be used in answering questions 4 and 5. "A" and "α" are constants.



(4) Determine the electric field as a function of x for $x_1 \leq x \leq x_2$.

(a) $\mathcal{E}(x) = -(A/K_S\varepsilon_o\alpha)\, e^{-\alpha(x_2 - x)}$

(b) $\mathcal{E}(x) = -(A/K_S\varepsilon_o\alpha)\, e^{-\alpha(x - x_1)}$

(c) $\mathcal{E}(x) = -(A/K_S\varepsilon_o\alpha)(e^{-\alpha x} - e^{-\alpha x_2})$

(d) $\mathcal{E}(x) = -(A/K_S\varepsilon_o\alpha)(e^{-\alpha x} - e^{-\alpha x_1})$

(e) $\mathcal{E}(x) = -(A/K_S\varepsilon_o\alpha)\, e^{-\alpha x}$

(5) The electric field at x = 0 is

(a) $\mathcal{E}(x=0) < 0$

(b) $\mathcal{E}(x=0) = 0$

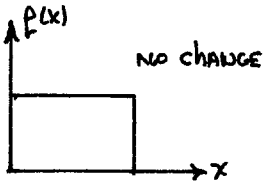
(c) $\mathcal{E}(x=0) > 0$

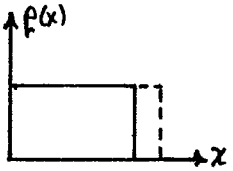
[6] In a real pn junction diode, the current measured when the diode is slightly forward biased is greater than that predicted by the ideal diode equation. This deviation occurs because of

(a) Recombination in the depletion region.
(b) Generation in the depletion region.
(c) Recombination in the quasi-neutral regions.
(d) Generation in the quasi-neutral regions.

[7/8] If the minority carrier lifetime is increased on the n-side of a reverse-biased p^+-n diode, what effect will the lifetime increase have on the charge distribution and the minority carrier density?

charge distribution

(a)


(b)


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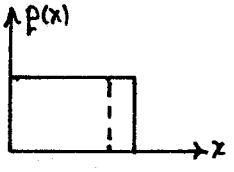
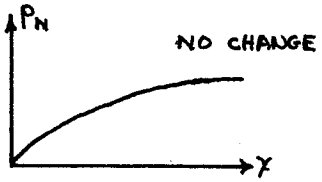
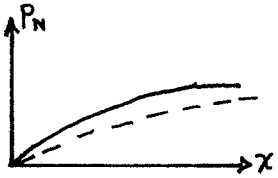


minority carrier density

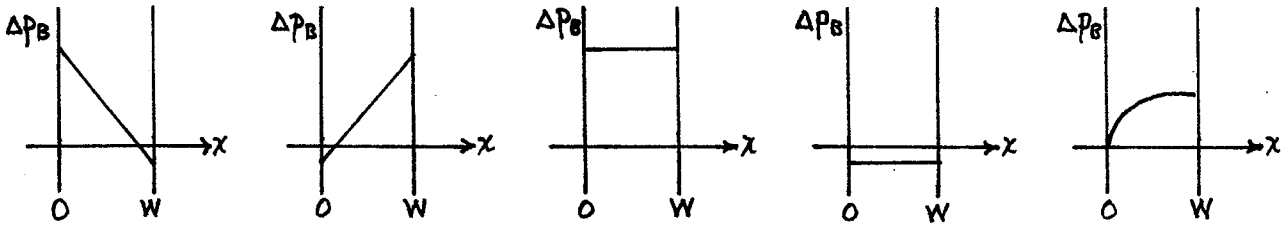
(a)


(b)


(c)


[9/10] The polarity (forward or reverse) of the bias being applied to the emitter-base and collector-base junctions of a BJT are specified by citing the biasing "mode". Complete the table below indicating (1) the polarity specified for each of the biasing modes and (2) the minority carrier distribution plot (a - e) associated with the given biasing mode. NOTE: There are really only four BJT biasing modes. Identify the "false" mode with "X" entries in the table.

Biasing Mode	Polarity of Bias emitter-base	collector-base	Minority Carrier Distribution in base (a-e)
Active			
Cut-Off			
Saturation			
Inversion			
Inverted Active			



(a) (b) (c) (d) (e)

[11] The condition in real BJT's where more current flows near the edges of the emitter than in the middle of the emitter is referred to as

(a) Punch-through

(b) Base-width modulation

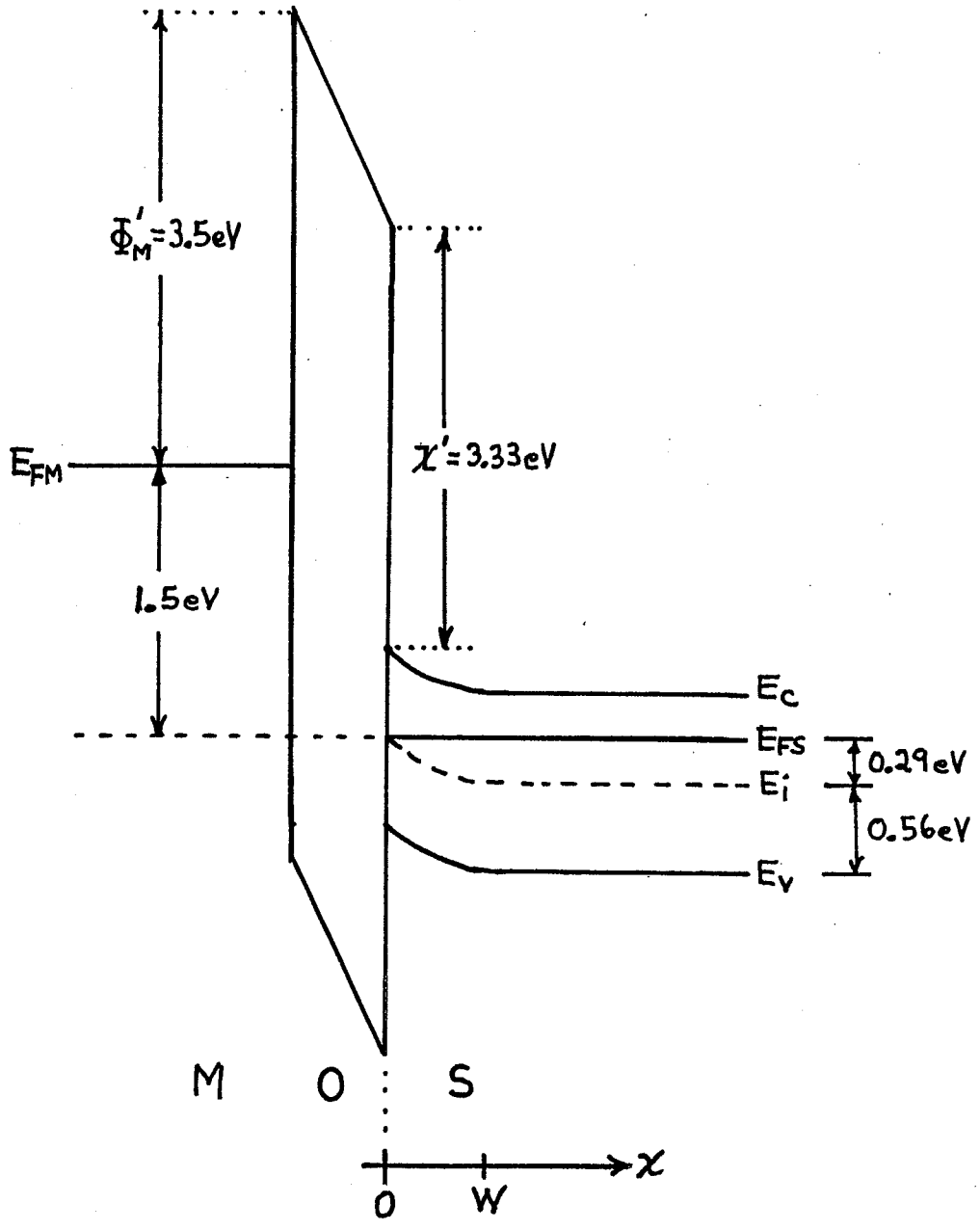
(c) Emitter flexing

(d) Emission or current crowding

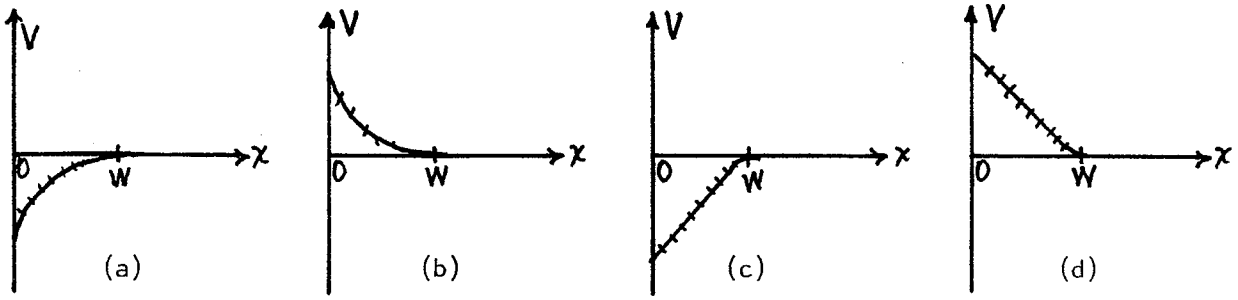
(e) Injection efficiency

[12-24] A totally dimensioned energy band diagram for an MOS-C under a specific gate bias is shown in the figure below. The device is maintained at T = 300K, $kT/q = 0.026V$, $n_i = 10^{10}/cm^3$, $K_S = 11.8$, $K_0 = 3.9$ and $x_o = 0.2\mu m = 2 \times 10^{-5} cm$. Also, $Q_{IT} = 0$ and $E_F - E_i = 0$ at the surface of the semiconductor.

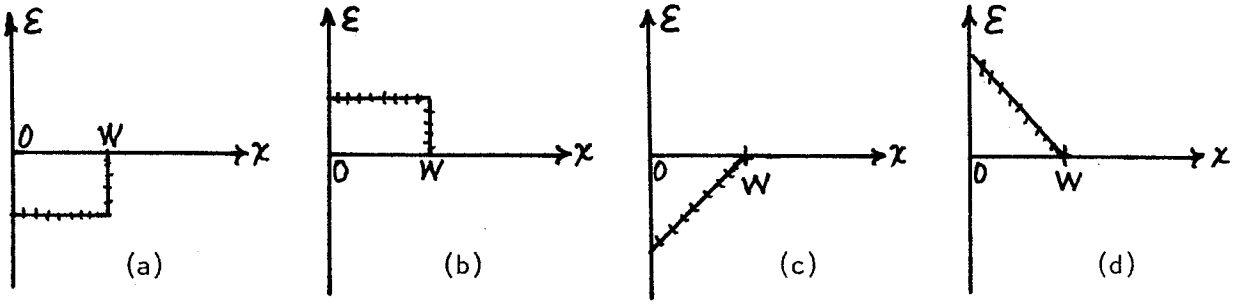
Use the cited energy band diagram and the given information in answering questions 12 - 24.



(12) The electrostatic potential (V) inside the semiconductor is as sketched below.



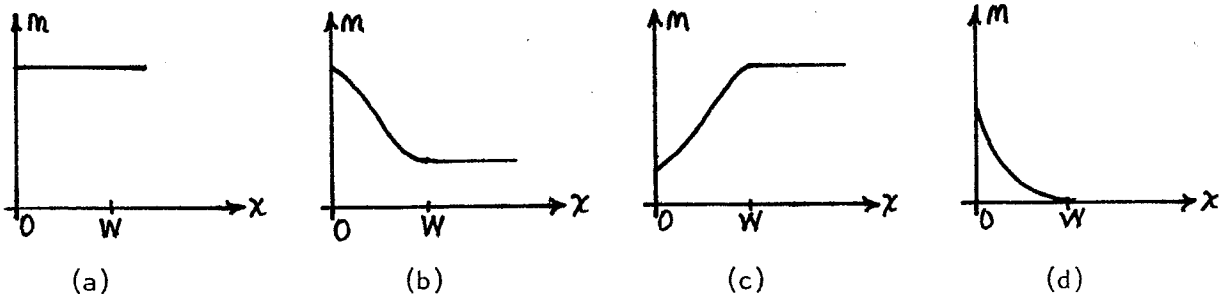
(13) The electric field inside the semiconductor is roughly as sketched below.



(14) Do equilibrium conditions prevail inside the semiconductor?

(a) Yes (b) No (c) Can't be determined.

(15) On a semilog plot the electron concentration versus position inside the semiconductor is roughly as sketched below.



(16) Let $\mathcal{E}_S$ be the electric field in the semiconductor at the oxide-semiconductor interface. The electron drift current density flowing in the x-direction at x = 0 (on the semiconductor side of the interface) is

(a) Zero

(b) $q\mu_n N_D \mathcal{E}_S$

(c) $q\mu_n n_i \mathcal{E}_S$

(d) $-qD_N N_D/W$

(e) $-qD_N n_i/W$

(17) N_D = ?

(a) $3.24 \times 10^{14}/cm^3$ (c) $1.00 \times 10^{10}/cm^3$

(b) $6.98 \times 10^{14}/cm^3$ (d) $1.02 \times 10^{15}/cm^3$

(18) V_G = ?

(a) 0.29V (b) -0.29V (c) 1.5V (d) -1.5V (e) 0 V

(19) What is the voltage drop (ΔV_{ox}) across the oxide?

(a) -1.11V (b) -1.38V (c) -0.83V (d) -1.5V (e) -1.0V

(20) What is the voltage drop across the semiconductor ($V|_{x=0} - V|_{x=\infty}$)?

(a) -0.98V (b) 0.29V (c) -0.29V (d) 0.83V (e) -0.83V

(21) What is the metal-semiconductor workfunction difference (ϕ_{MS})?

(a) 0.46V (b) 0.17V (c) -0.1V (d) -0.39V

(22) The mobile ion charge in the oxide must be very small (i.e., $Q_M \simeq 0$). One comes to this conclusion because...

(a) There is no band bending in the metal.

(b) The fields in the oxide and semiconductor have the same polarity at the oxide-semiconductor interface.

(c) The band-bending in the oxide is a linear function of position.

(d) The voltage drop across the oxide only slightly exceeds the voltage drop across the semiconductor.

(23) Q_F/C_o = ? (NOTE: If the energy band diagram is examined very carefully, one concludes $D_{SEMI} = D_{OX}$ at the oxide-semiconductor interface.)

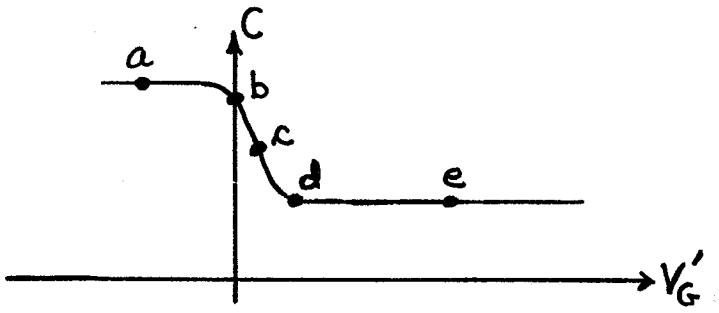
(a) Zero (b) -0.28V (c) 0.58V (d) 0.27V (e) 1.5V

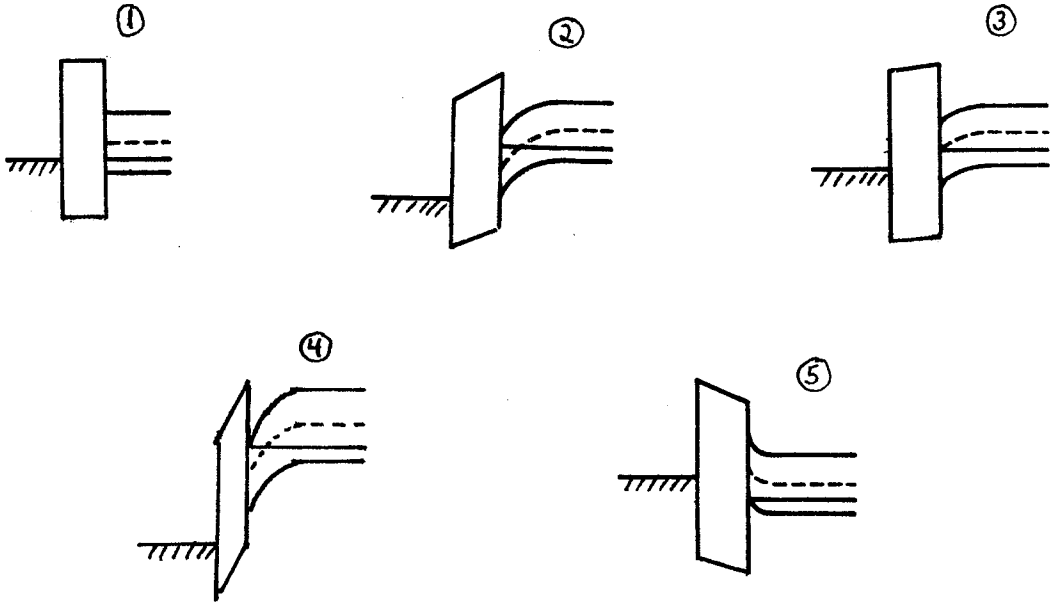
(24) Compute the normalized small signal capacitance, C/C_0, at the applied bias point.

(a) 0.12 (b) 0.21 (c) 0.45 (d) 0.63 (e) 1.00

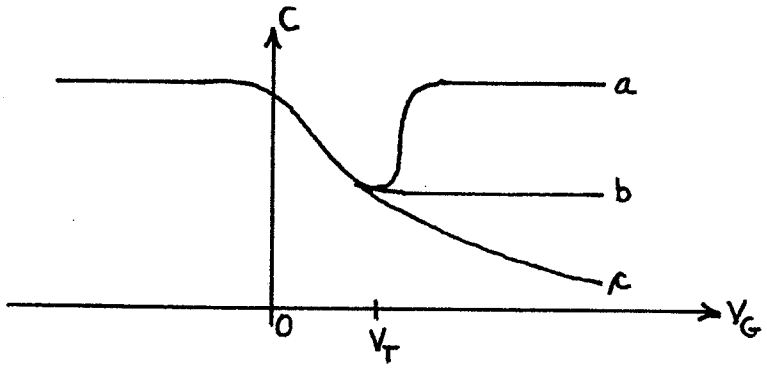
[25/26] Complete the following table making use of the ideal-structure C-V characteristics and energy band diagrams included below the table. Specifically, for each of the biasing conditions named in the table, identify (1) the corresponding bias point on the ideal MOS-C C-V characteristic employing a letter (a - e) and (2) the associated band diagram using a number (1 - 5).

Bias Condition	Capacitance (a-e)	Band Diagram (1-5)
Inversion		
Depletion		
Flat Band		
Threshold		
Accumulation		





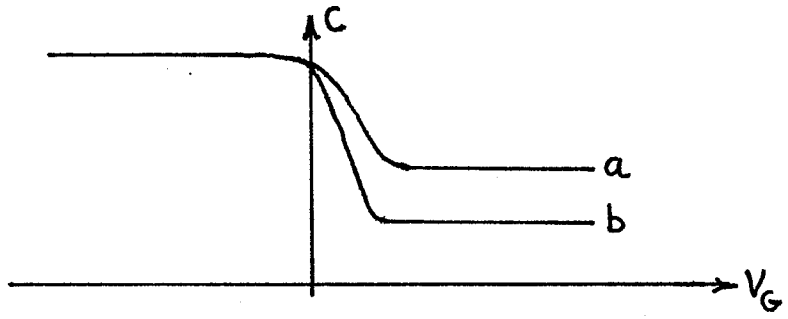
[27]



Considering the C-V curves shown above, for which curve (or curves) is an <u>equilibrium</u> inversion layer present when $V_G > V_T$?

(a) curve a
(b) curve b
(c) curve c
(d) curves a and b
(e) curves b and c
(f) curves a, b, and c

[28]



Relative to the MOS-C exhibiting curve-a, the MOS-C exhibiting curve-b has...

(a) thinner oxide
(b) thicker oxide
(c) lower silicon doping
(d) higher silicon doping
(e) both a and c
(f) both b and c
(g) both a and d
(h) both b and d

[29-31] A silicon MOSFET has the following parameters: $x_o = 0.05\mu m = 5 \times 10^{-6} cm$, $Q_F = 3 \times 10^{-8}$ coul/cm^2 ($Q_F/q = 1.875 \times 10^{11}/cm^2$), $N_A = 10^{16}/cm^3$, $N_D = 0$, $\Phi_M = 4.1eV$, $\chi = 4.05eV$, and $Q_M = Q_{IT} = 0$. The source and back of the MOSFET are grounded.

(29) Calculate V_{FB}.

(a) -0.434V (b) -0.869V (c) -1.30V (d) -0.743V

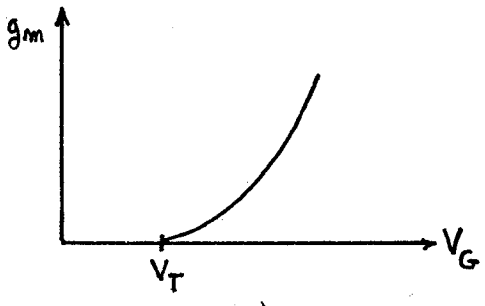
(30) Calculate $V_T - V_{FB}$.

(a) 0.718V (b) 1.426V (c) 0.359V (d) 0.860V

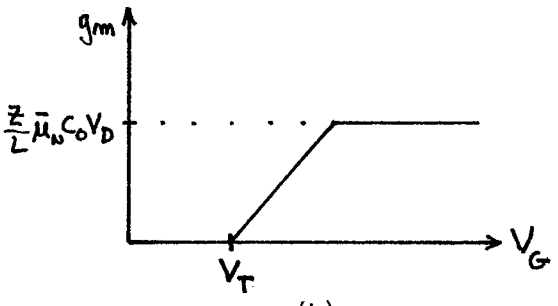
(31) Calculate the depletion width at the source end of the channel (y = 0) when $V_G = V_T$.

(a) 0.306μm (b) 0.216μm (c) 0.612μm (d) 1.216μm

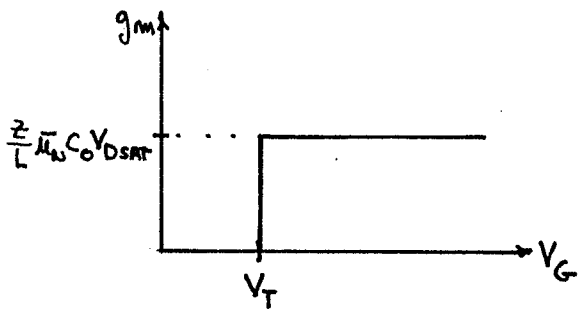
[32] In a MOSFET the transconductance, g_m, is defined as $\partial I_D/\partial V_G|_{V_D=constant}$. Which of the plots below correctly characterizes g_m when $V_D > V_{Dsat}$?



(a)



(b)



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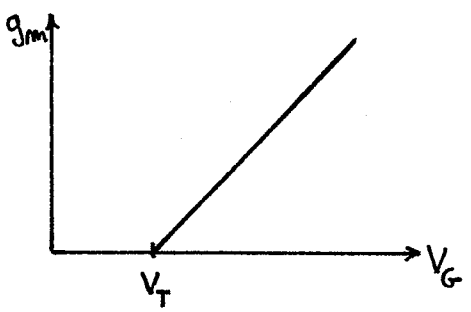

(d)

[33-44] MOS True or False Quiz

Answer ONLY 8 of the following 12 questions.
Only the FIRST 8 you answer will be graded.

(33) The effective mobility of carriers in MOSFET surface channels is always less than or equal to the bulk mobility of the same carriers.

(a) True (b) False

(34) The fixed oxide charge in MOS devices is typically distributed almost uniformly throughout the oxide.

(a) True (b) False

(35) The fixed oxide charge is typically minimized by annealing the structure in the presence of hydrogen at temperatures < 500°C.

(a) True (b) False

(36) "Saturation" in a MOSFET occurs when both source and drain inject minority carriers into the channel region at the same time.

(a) True (b) False

(37) The "Square-Law" theory for the d.c. characteristics of a MOSFET derives its name from the fact that, in this theory, one obtains $I_{Dsat} \propto (V_G - V_T)^2$.

(a) True (b) False

(38) MOSFET's which do not conduct current (are "OFF") when $V_G=0$ are typically referred to as "depletion mode" devices.

(a) True (b) False

(39) Velocity saturation can result in a factor-of-two correction to the MOSFET I-V curves in short channel devices.

(a) True (b) False

(40) "Field-Effect" is the term used to describe the elimination of the conducting inversion layer at the drain end of the MOSFET channel when $V_D=V_{Dsat}$.

(a) True (b) False

(41) Both the fixed charge and the interfacial trap density are greater on {111} Si surfaces than on {100} surfaces.

(a) True (b) False

(42) "Bias-Temperature Stressing" in MOS work refers to applying a bias between the source and drain of a MOSFET while monitoring the temperature rise of the substrate.

(a) True (b) False

(43) Ion implantation and back biasing are two methods which have been employed to adjust the threshold voltage of MOSFET's.

(a) True (b) False

(44) The MOSFET has a lower channel current when biased in the reverse direction (i.e. source and drain terminals interchanged).

(a) True (b) False