Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**C**
Test:	**C16**
Type:	**Closed Book, Closed Notes**
Note:	**Available Info/Equation Sheets**

Problem Weighting is noted adjacent to each problem.

NAME_____ F-1 _____SCORE

IN ANSWERING THE FOLLOWING QUESTIONS INCLUDE ANY COMMENTS WHICH MAY HELP TO FORESTALL A MISINTERPRETATION OF THE REQUESTED PICTORIAL ANSWERS.

For parts (a)-(d) indicate how one uses the energy band diagram to visualize:

(4 each)

(a) Freeze-out of majority carrier electrons at donor sites as the temperature is lowered toward zero Kelvin.	(b) A degenerate semiconductor.
(c) The origin of the recombination-generation current in a reverse biased PN junction diode.	(d) A PNP Bipolar Junction Transistor under cutoff mode biasing.

NAME_____ F-1 continued

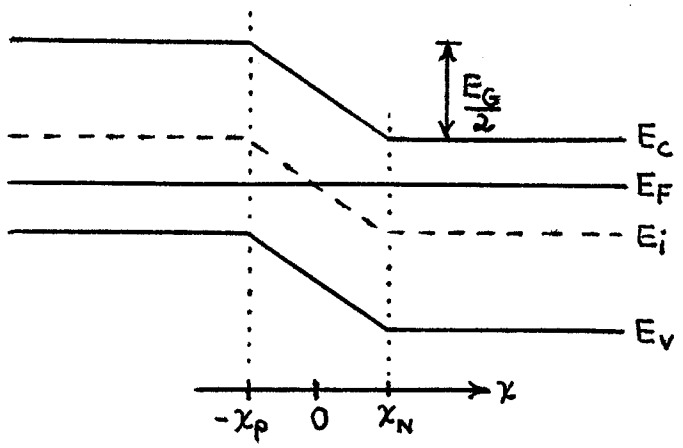
For parts (e) and (f) sketch an outine of the depletion region in...

(4) (e) a Bipolar Junction Transistor biased so as to cause "punch-through".

(4) (f) an n-channel J-FET where $V_P < V_G < 0$ and $V_D > V_{Dsat}$.

NAME_____ F-2 _____SCORE

The energy band diagram shown below characterizes a junction diode maintained at room temperature. Answer the questions which follow using the information conveyed in the diagram and the data adjacent to the diagram.



Data

$E_G = 1.00eV$

$kT = 0.025eV$

$K_S = 10.0$

$\varepsilon_o = 8.85 \times 10^{-14}$ f/cm

$A(area) = 10^{-3}$ cm^2

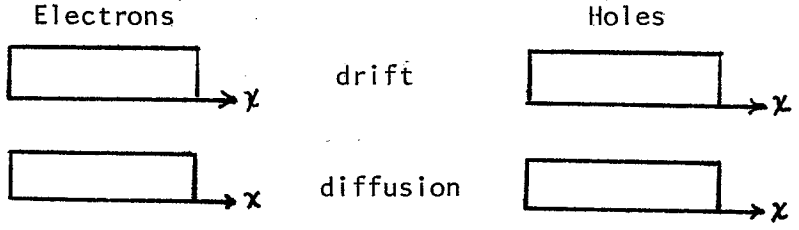
$x_n + x_p = 10^{-4}$ cm

(4) (a) Do equilibrium conditions prevail? How did you arrive at your answer?

(4) (b) What is the electric field ($\mathcal{E}$) in the depletion region? (Provide both a symbolic and numerical answer.)

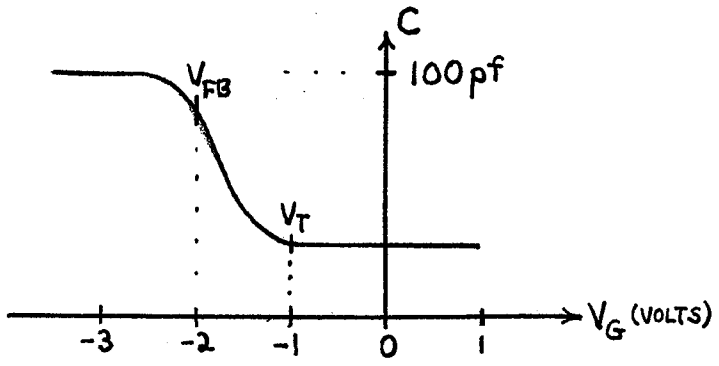
(4) (c) What will be the junction (or depletion-layer) capacitance exhibited by the diode at the pictured bias point?

(4) (d) Place arrows in the boxes shown below to indicate the direction of the drift and diffusion currents inside the depletion region.



NAME_____ F-3 _____SCORE

An MOS-C exhibits the high-frequency C-V characteristic shown below.



(4) (a) Identify the accumulation, depletion, and inversion bias regions for the given MOS-C by completing the following table.

Bias Region	V_G Range
accumulation	
depletion	
inversion	

(2) (b) Is the semiconductor doped n or p-type?

(3) (c) Using a dashed line and adding to the figure in the statement of the problem, sketch the low-frequency C-V characteristic to be expected from the given MOS-C.

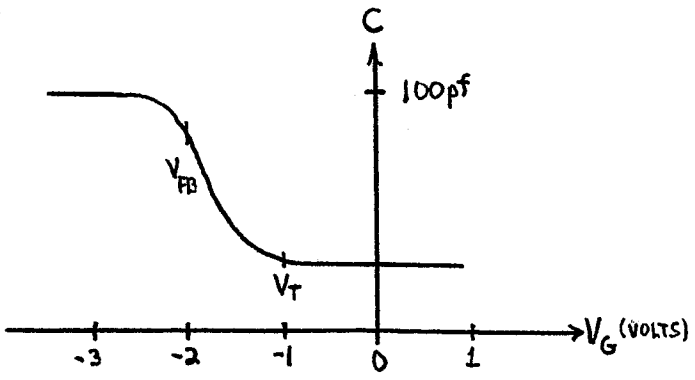
(8) (d) As concisely as possible, explain the "inside-the-device" cause of differences in the low- and high-frequency C-V characteristics exhibited by an MOS-C.

NAME_____ F-3 continued

(4) (e) If the area of the MOS-C gate is $A_G = 10^{-3}$ cm^2, what is the oxide thickness (x_o)?

(6) (f) ϕ_{MS} for the given device is -1V. Assuming the remaining shift in the observed flat band voltage is due to sodium ions uniformly distributed throughout the SiO_2, determine the concentration (ions/cm^3) of sodium ions in the oxide.

(3) (g) The semiconductor doping of the given MOS-C is somehow increased. Graphically indicate on the figure below the expected change in the high-frequency C-V characteristics.



NAME_____ F-4 _____SCORE

A MOSFET is fabricated with $\phi_{MS} = -0.2V$, $Q_M = Q_{IT} = 0$, $Q_F/q = 5 \times 10^{10}/cm^2$, $x_o = 0.1\mu m$, $A_G = 10^{-3}cm^2$, $N_A = 1 \times 10^{16}/cm^3$. Assume the source and substrate are always grounded; $T = 23^oC$.

(4) (a) Determine the flatband gate voltage, V_{FB}. (Provide both a symbolic and numerical answer.)

(6) (b) Determine the gate voltage at the onset of inversion, V_T.

(2) (c) Is the given MOSFET an enhancement mode or depletion mode device? Explain.

NAME _____ F-4 continued

(6) (d) Sketch the MOS energy band diagram for the given transistor at the onset of inversion ($V_G = V_T$, $V_D = 0$).

(6) (e) Sketch the MOS block charge diagram for the given transistor at the onset of inversion ($V_G = V_T$, $V_D = 0$).

(6) (f) Sketch the inversion layer and depletion region inside the MOSFET at pinch-off. Show and label all parts of the transistor.