Course:	**Semiconductor Device Fundamentals**
Level:	**Undergraduate**
Module:	**C**
Test:	**C17**
Type:	**Closed Book, Closed Notes**
Note:	**Available Info/Equation Sheets**

Problem Weighting--- **F-1...24 (4 each part)**
F-2...24 (4 each part)
F-3...24 (4 each part)
F-4...28 (4 each part)

F - 1

IN ANSWERING THE FOLLOWING QUESTIONS INCLUDE ANY COMMENTS WHICH MAY HELP FORESTALL A MISINTERPRETATION OF THE REQUESTED PICTORIAL ANSWERS.

Using the energy band diagram indicate how you would visualize...

(a) Recombination of an electron and a hole at a recombination-generation site;

(b) Tunneling (the Zener breakdown process) in a heavily-doped reverse-biased P^+-N^+ junction diode.

Sketch an outline of the depletion region(s) in...

(c) A Bipolar Junction Transistor where punch-through has occurred;

(d) An n-channel J-FET where $V_P < V_G < 0$ and $V_D = V_{Dsat}$.

Sketch the approximate charge distribution in...

(e) A linearly-graded p-n junction diode under equilibrium conditions;

(f) A $V_G = 0$ biased n-bulk capacitor which is ideal except for a $\phi_{MS} < 0$.

F - 2

The energy band diagram shown in Fig. F-2 characterizes a step junction diode maintained at room temperature. Answer the questions which follow using the information conveyed in the diagram and the data adjacent to the diagram.

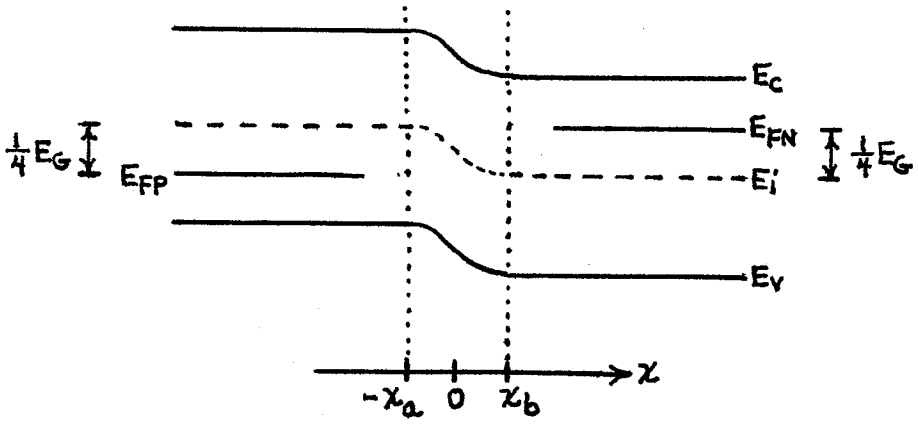

Fig. F-2

Data

$E_{Fn}-E_{Fp} = E_G/4$

$E_G = 1.00eV$

$kT = 0.0255eV$

$K_S = 10.0$

$\varepsilon_o = 8.85 \times 10^{-14} f/cm$

$A(area) = 10^{-2} cm^2$

$x_a + x_b = 10^{-4} cm$

(a) What is the polarity and magnitude of the voltage (V_A) being applied to the device. Explain how you arrived at your answer.

(b) Determine V_{bi}, the built-in voltage.

(c) What will be the junction (or depletion-layer) capacitance exhibited by the diode at the pictured bias point?

(d) Make a rough sketch of the carrier concentrations, n and p, for the $x \leq -x_a$ and $x \geq x_b$ portions of the diode. Assume low level injection conditions.

(e) Would you expect the device to exhibit a significant diffusion capacitance at the applied bias point? Explain.

(f) What additional information would you require in order to compute the recombination-generation current flowing through the diode at the pictured bias point? Explain.

F - 3

(a) What is the relationship between the depletion-inversion transition point voltage introduced in the MOS-C discussion and the threshold (or turn-on) voltage introduced in the MOSFET discussion?

(b) What is the observed dependence of the fixed oxide charge (Q_F) on the silicon surface orientation?

(c) What is (or what is believed to be) the physical origin of the interfacial traps in MOS structures?

(d) Why is the mobility of carriers in a surface inversion layer different than the bulk mobility of the same carriers?

(e) Precisely, what is the "channel" in MOSFET terminology?

(f) What is the mathematical definition of the MOSFET (i) drain conductance and (ii) transconductance?

F - 4

A Si - SiO_2 - Si capacitor (SOS-C) is constructed with a p-type nondegenerate silicon electrode on the left-hand side of the oxide and an n-type nondegenerate silicon electrode on the right-hand side of the oxide. The structure is ideal except for the non-zero workfunction difference between the two electrodes. N_A(p-side) = N_D(n-side) = $10^{15}/cm^3$ and the structure is being maintained at room temperature where n_i(Si) = 8.6 X $10^9/cm^3$ and kT/q = 0.0255V.

(a) Sketch the energy band diagram for the structure under flat band conditions.

(b) What is the gate voltage one must apply to the structure to achieve flat band conditions? (Give both the magnitude and sign of V_G.)

(c) Draw the approximate form of the energy band diagram for the structure under zero-bias (V_G = 0) conditions.

(d) Draw the energy band diagram for the structure if V_G is a large negative bias.

(e) Draw the block charge diagram characterizing the structure when V_G is a large negative bias.

(f) Sketch the general shape of the high-frequency C-V_G characteristic one expects to obtain from the SOS-C described in this problem.

(g) At large negative biases, will the high-frequency capacitance displayed by this SOS-C be greater than, equal to, or less than the high-frequency capacitance displayed by a standard n-bulk MOS-C? Explain.