EE-612:
Lecture 20:
MOSFET Leakage

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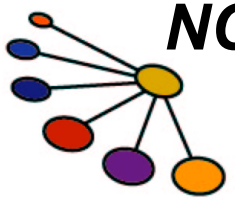
Fall 2006



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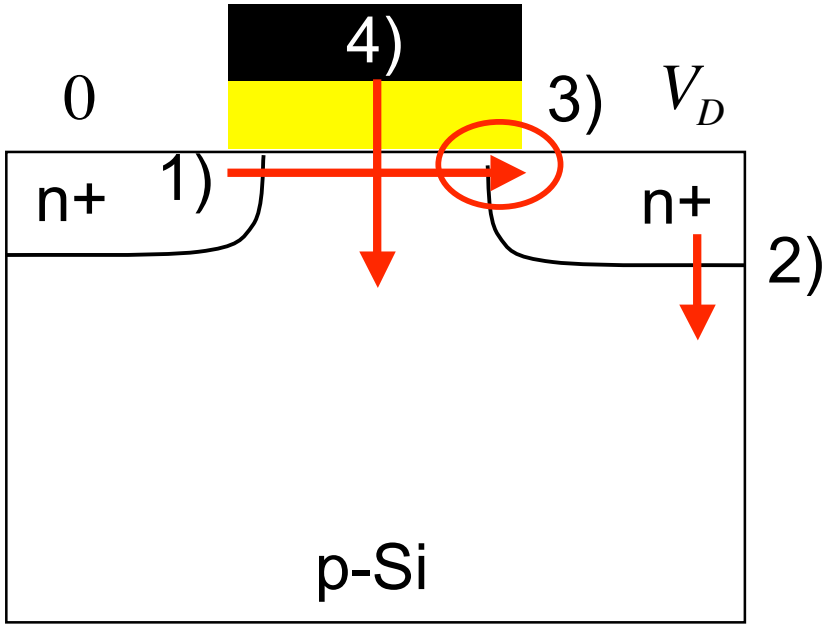
outline

1) Leakage components
2) Band to band tunneling
3) Gate-induced drain leakage
4) Gate leakage
5) Scaling and ITRS

leakage components



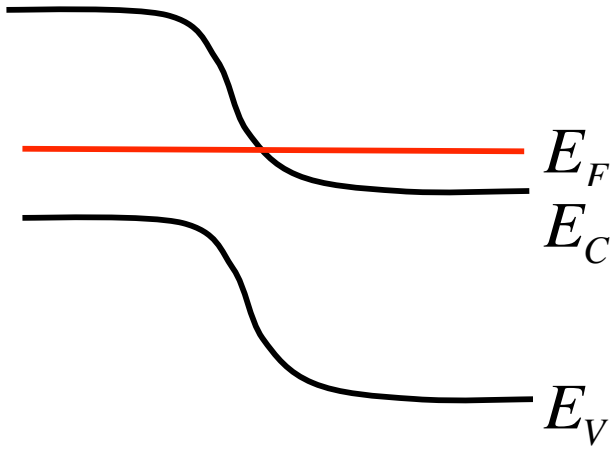
1) subthreshold current
2) junction leakage
3) gate-induced drain leakage (GIDL)
4) gate-leakage

outline

1) Leakage components
2) **Band to band tunneling**
3) Gate-induced drain leakage
4) Gate leakage
5) Scaling and ITRS

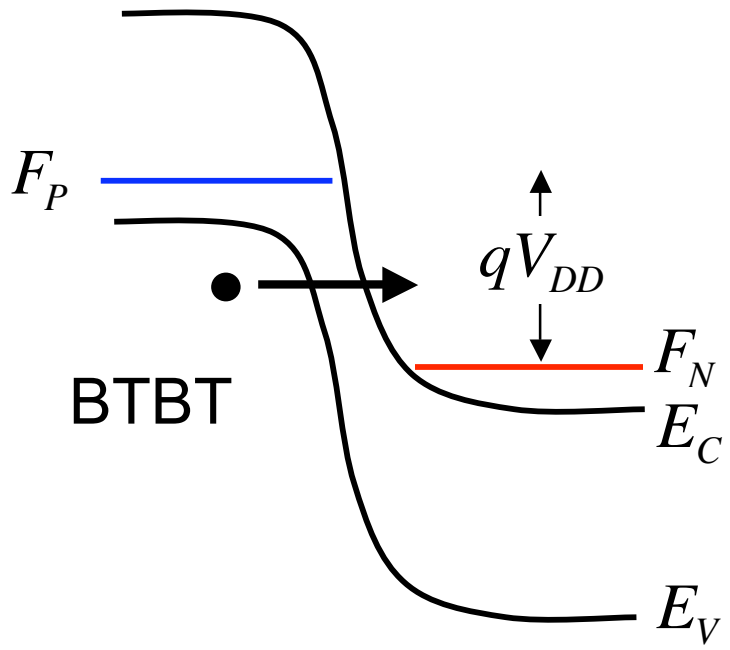
BTBT in the drain-substrate junction

equilibrium



p-substrate n+ drain

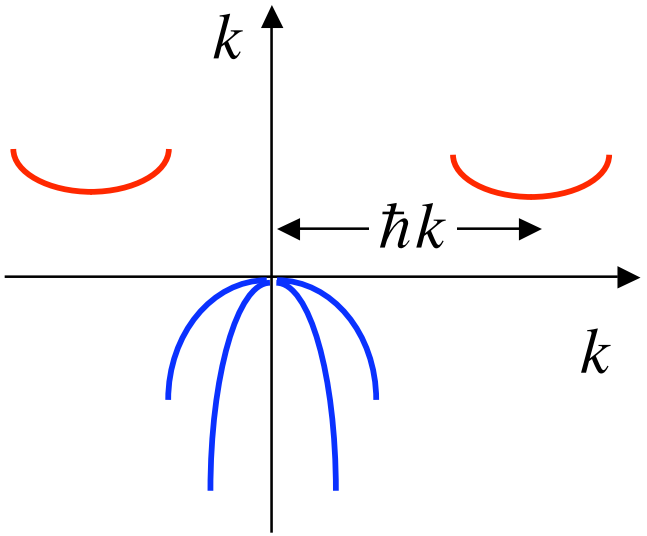
$V_D = V_{DD}$



p-substrate n+ drain

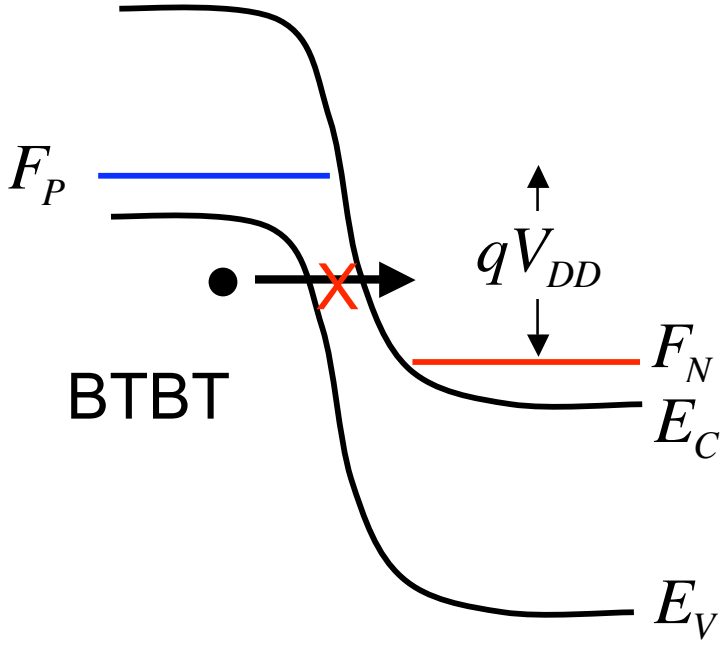
BTBT in the drain-substrate junction

k-space



conserve crystal momentum by phonon emission or absorption

$V_D = V_{DD}$



defect-assisted tunneling

BTBT (iii)

tunneling probability should involve the barrier height (E_G) and the barrier width (depletion layer)

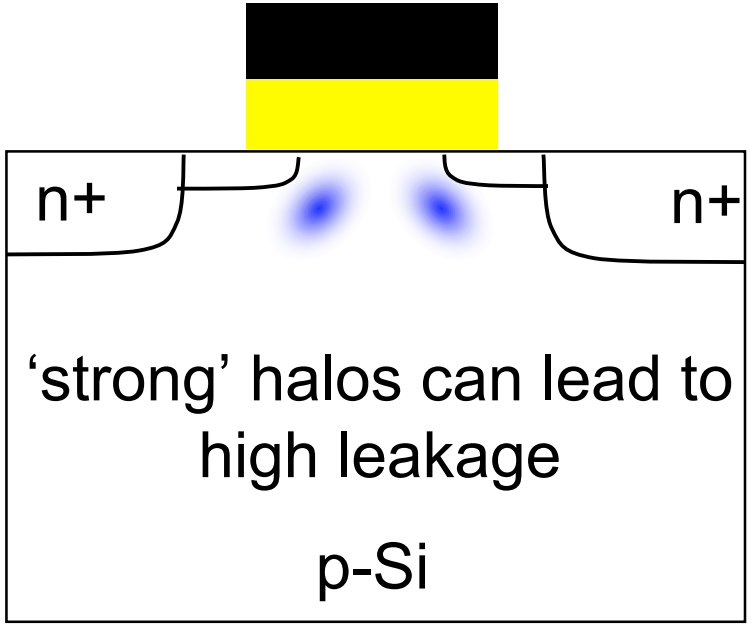
$$J_{B-B} = \frac{\sqrt{2m^*}q^3 E V_{DD}}{4\pi^3\hbar^2 E_G^{1/2}} \exp\left[-\frac{4\sqrt{2m^*}E_G^{3/2}}{3qE\hbar}\right]$$

eqn. (2.207) of Taur and Ning

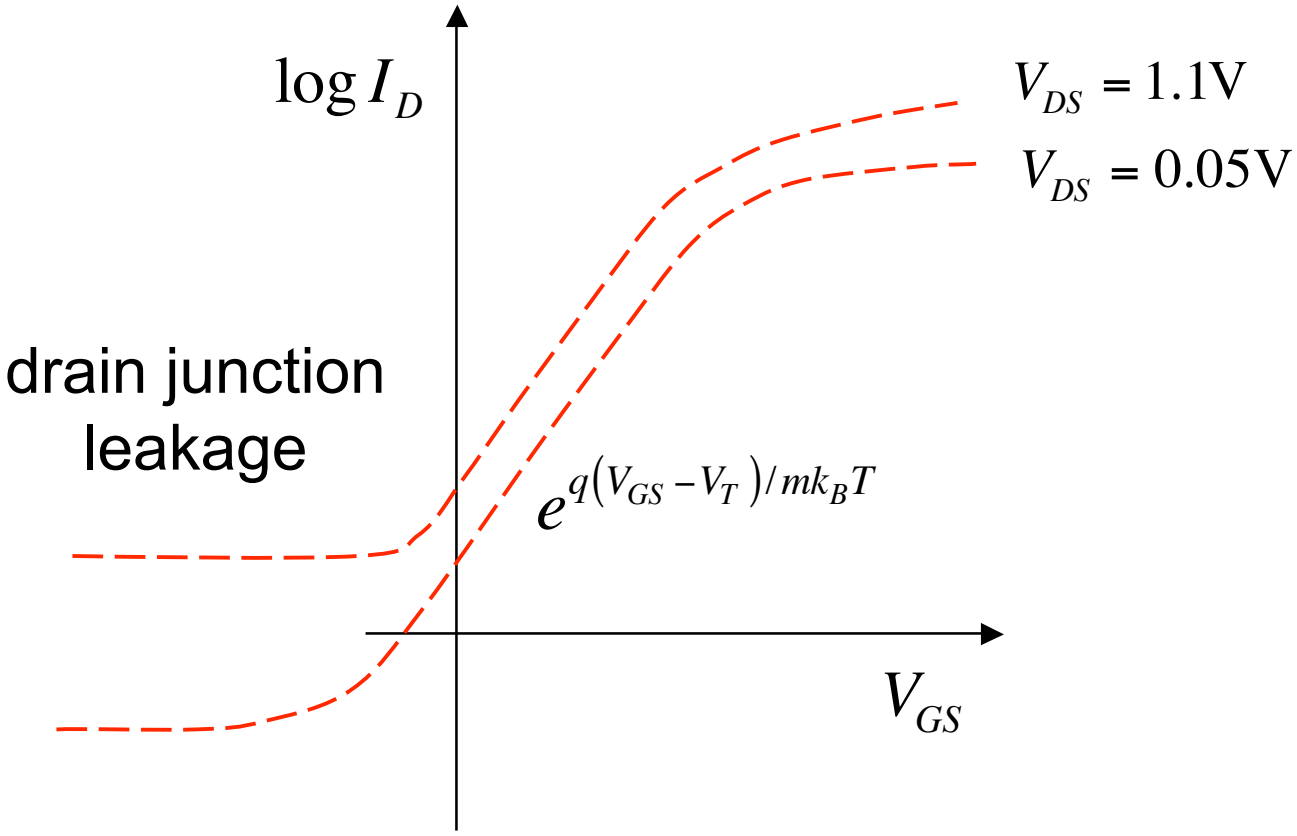
$$E = \sqrt{\frac{2qN_A\left(V_{DD}+V_{bi}\right)}{\varepsilon_{Si}}}$$

for $N_A = 5 \times 10^{18}$ cm^{-3}, V_{DD}=1V, $J_{B\text{-}B} \sim 1$A/cm^2

BTBT and halos



BTBT: effect on I-V



BTBT (iv)

is BTBT significant at the 70 nm node?

$$I_D = J_{B-B} L_D W = 1 \times 187 \times 10^{-7} \times 1000 \times 10^{-7} = 1.9 \times 10^{-9} \text{ A}/\mu\text{m}$$

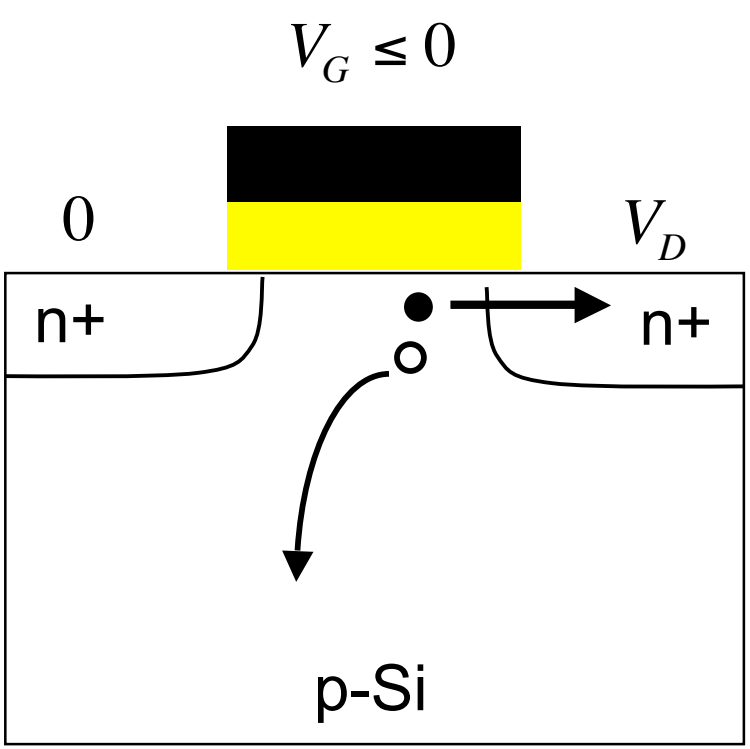
$$I_{OFF}(HP) = 0.15 \ \mu\text{A}/\mu\text{m} = 150 \text{ nA}/\mu\text{m}$$

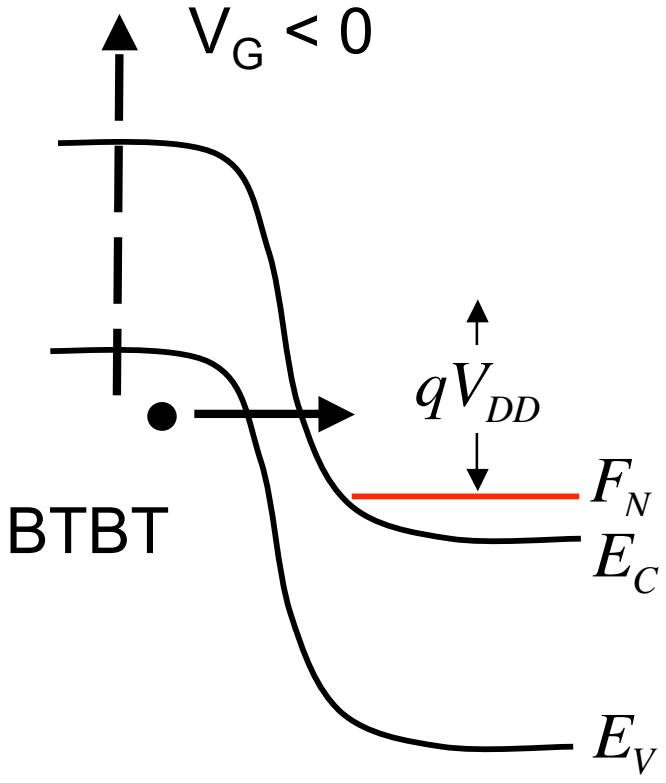
$$I_{OFF}(LSP) = 10^{-5} \ \mu\text{A}/\mu\text{m} = 10^{-2} \text{ nA}/\mu\text{m}$$

outline

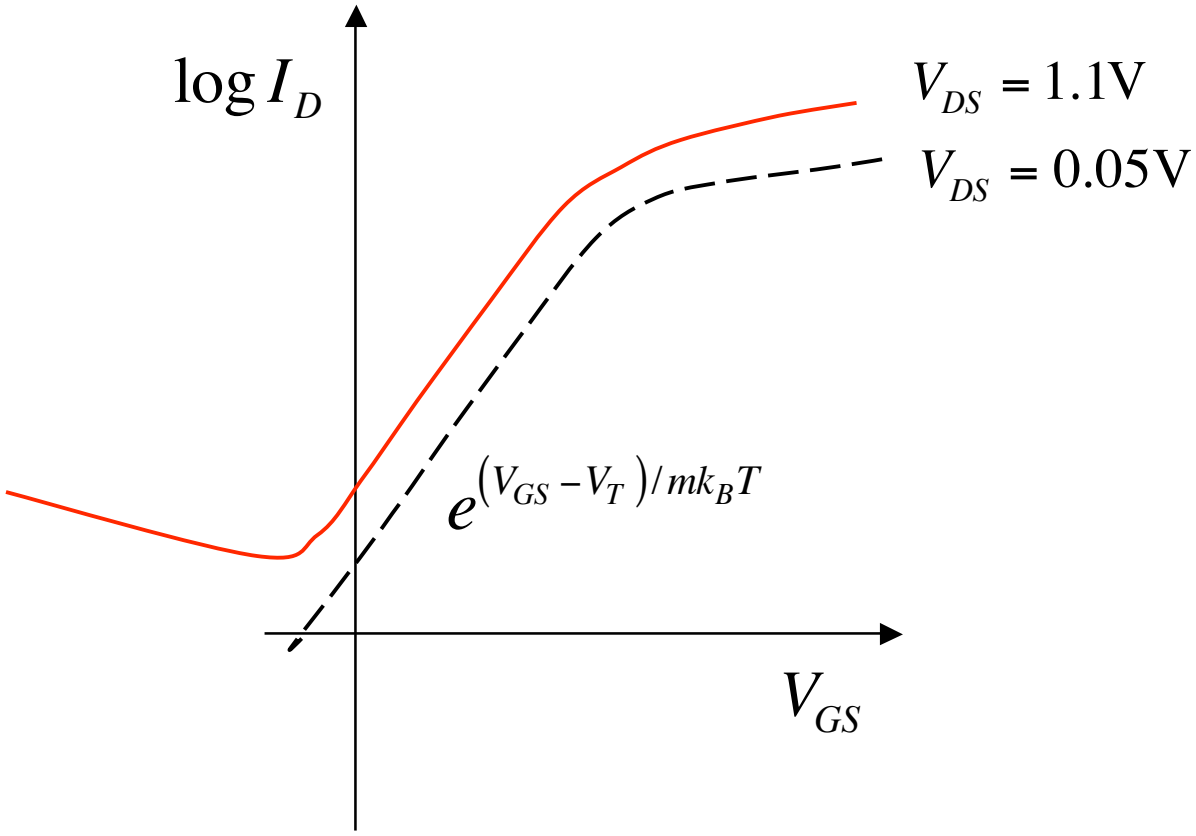
1) Leakage components
2) Band to band tunneling
3) **Gate-induced drain leakage**
4) Gate leakage
5) Scaling and ITRS

gate-induced BTBT

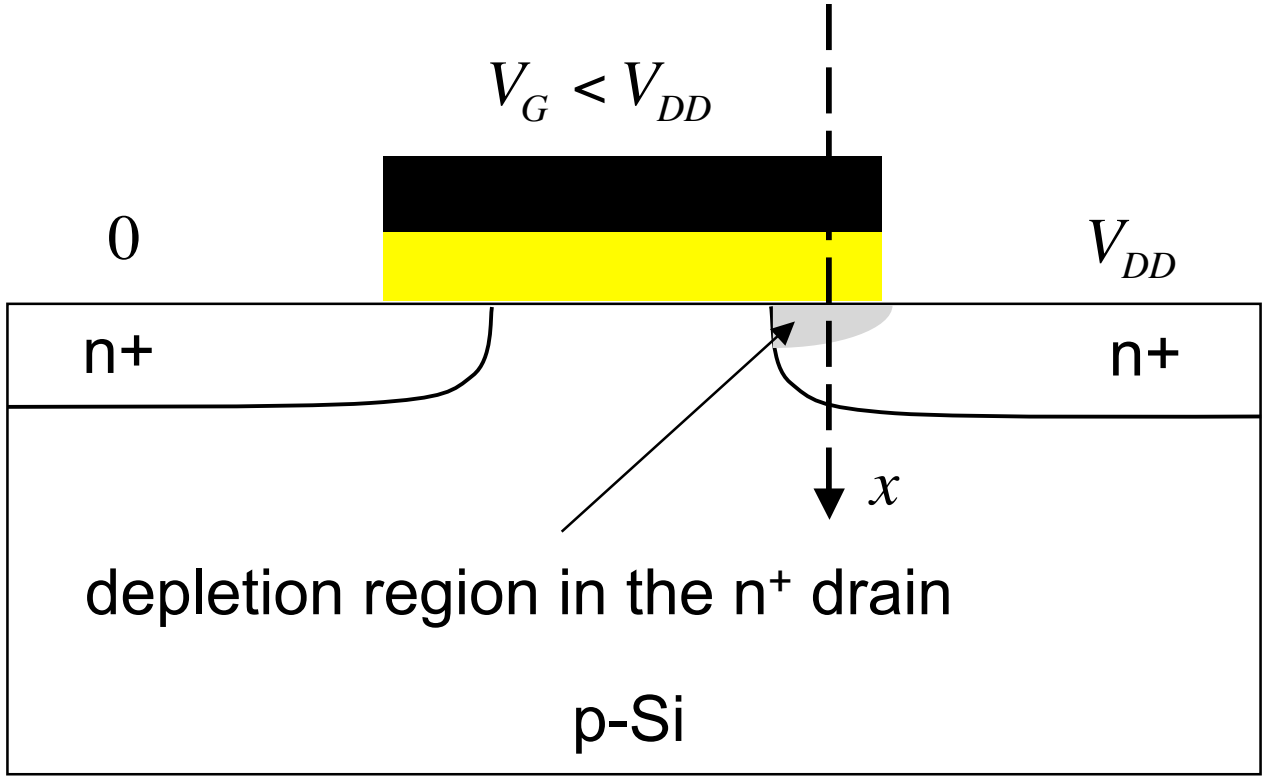




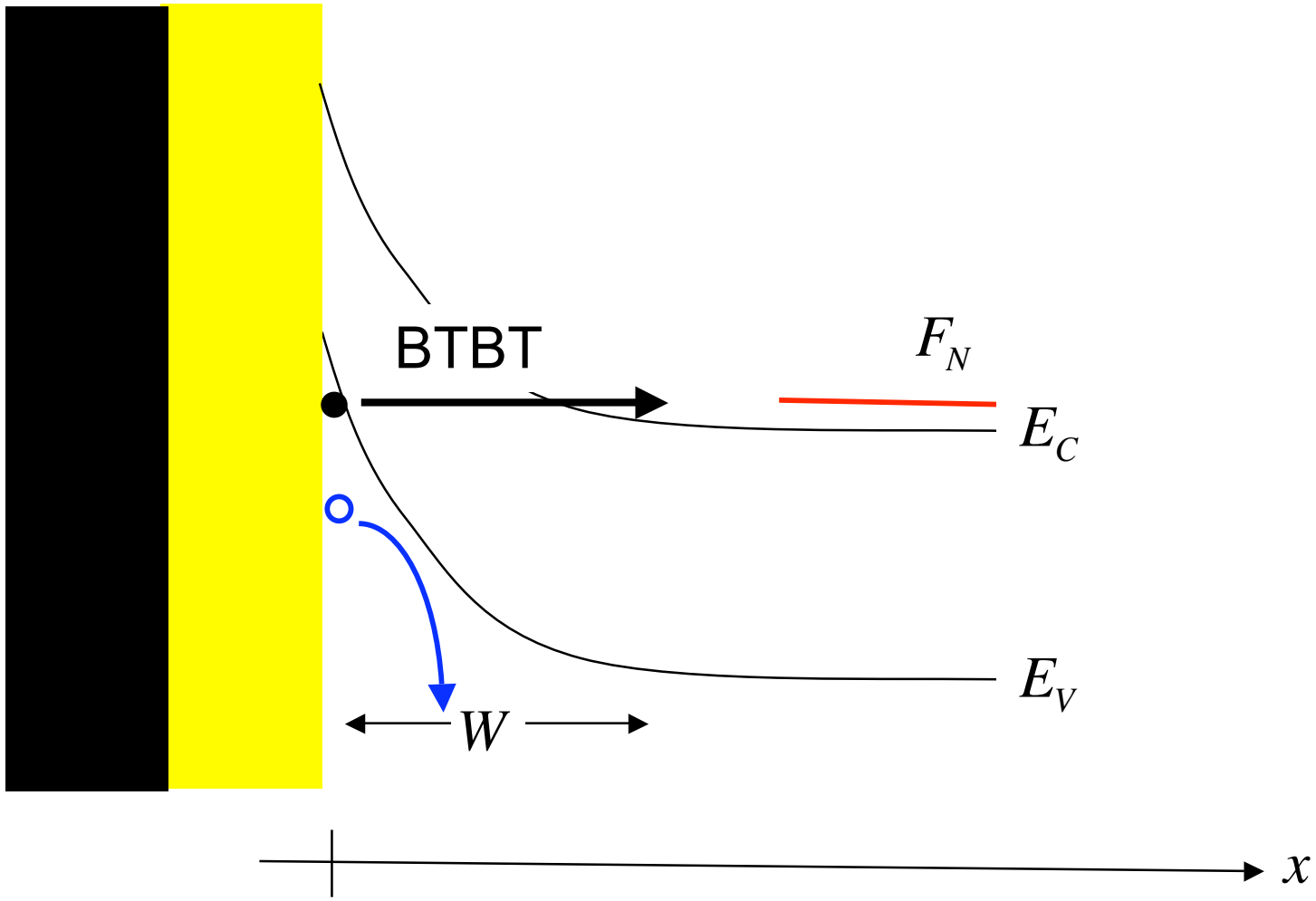
gate-induced BTBT: effect on I-V



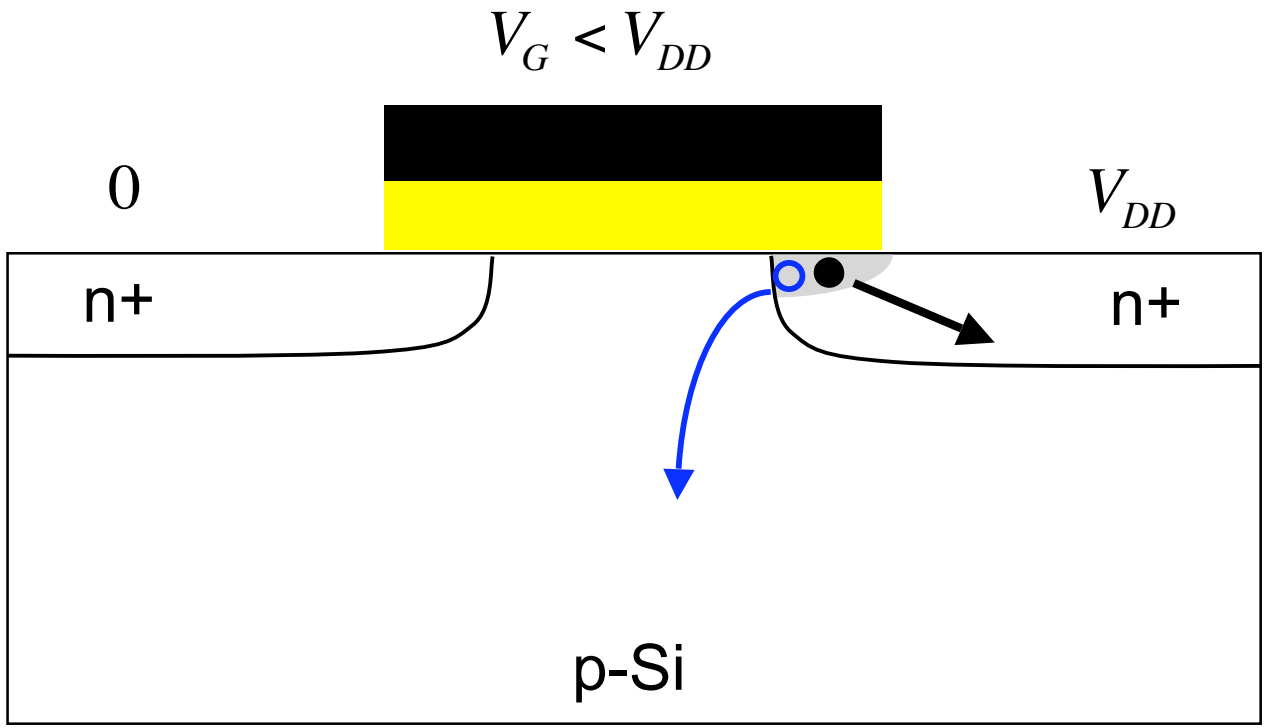
gate-induced drain leakage (GIDL)



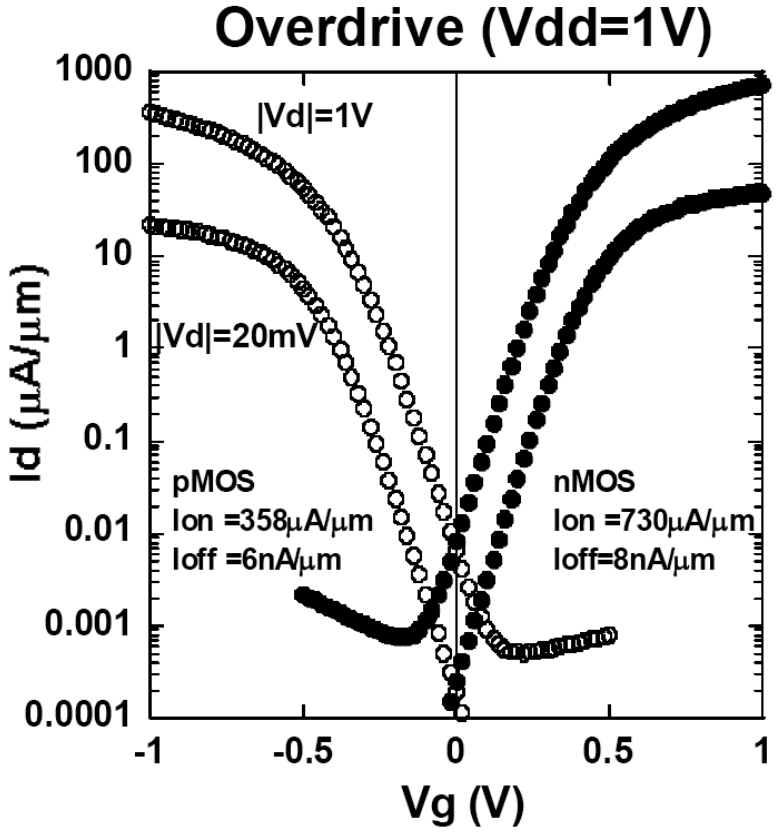
GIDL (iii)



GIDL (iii)

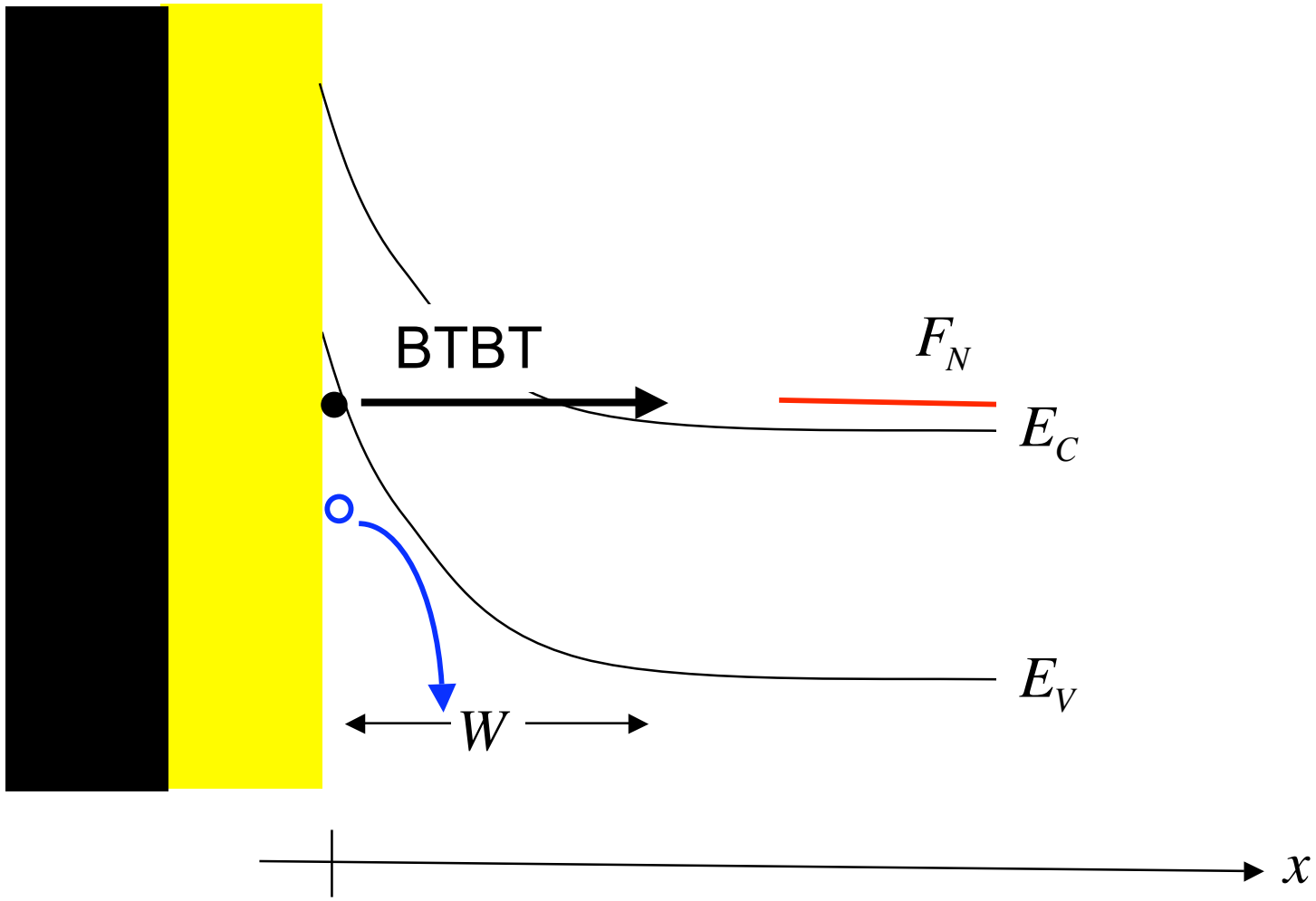


GIDL: example

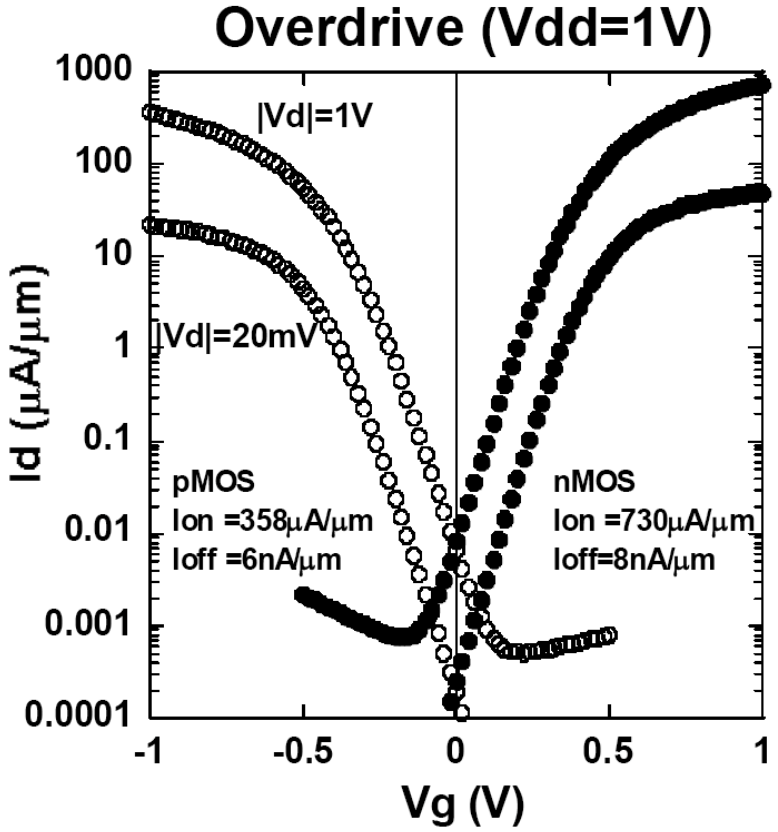


M. Okuno, et al., "45-nm Node CMOS Integration with a Novel STI Structure and Full-NCS/Cu Interlayers for Low-Operation-Power (LOP) Applications," IEDM, Washington DC. Dec. 5-7, 2005

GIDL (iii)



GIDL: example



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outline

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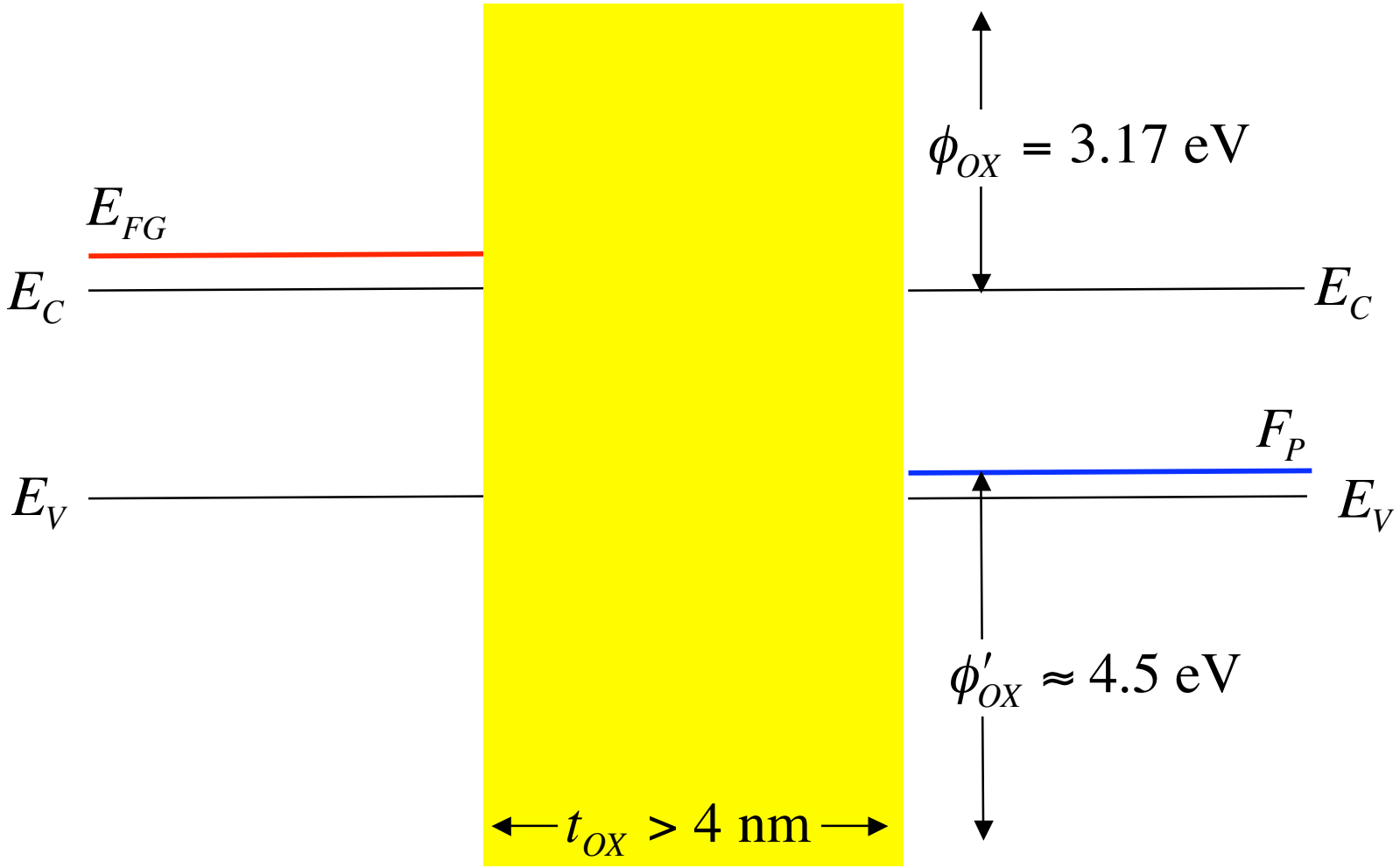
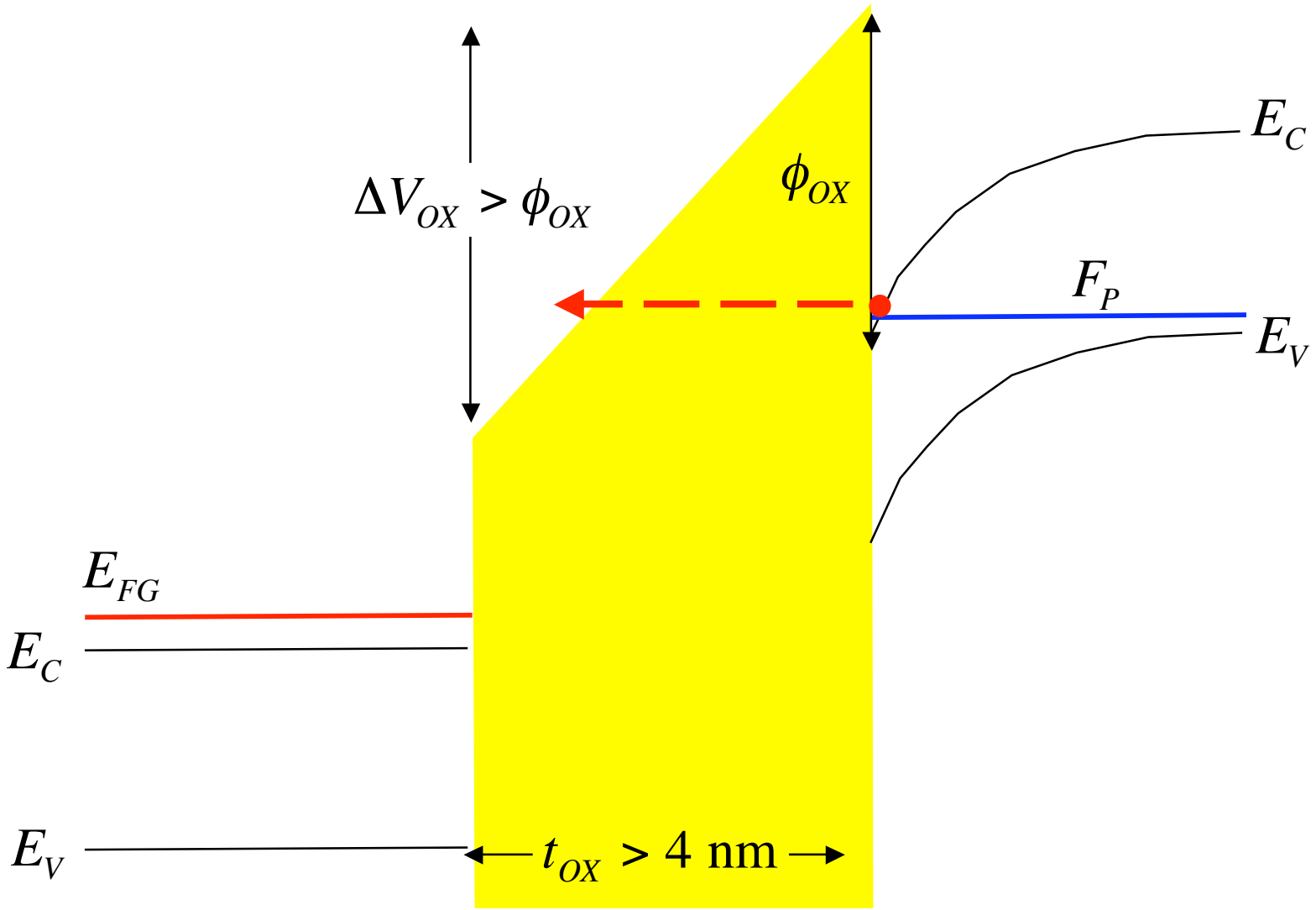
2) Band to band tunneling
3) Gate-induced drain leakage
4) **Gate leakage**
5) Scaling and ITRS

gate leakage



Fowler-Nordheim tunneling



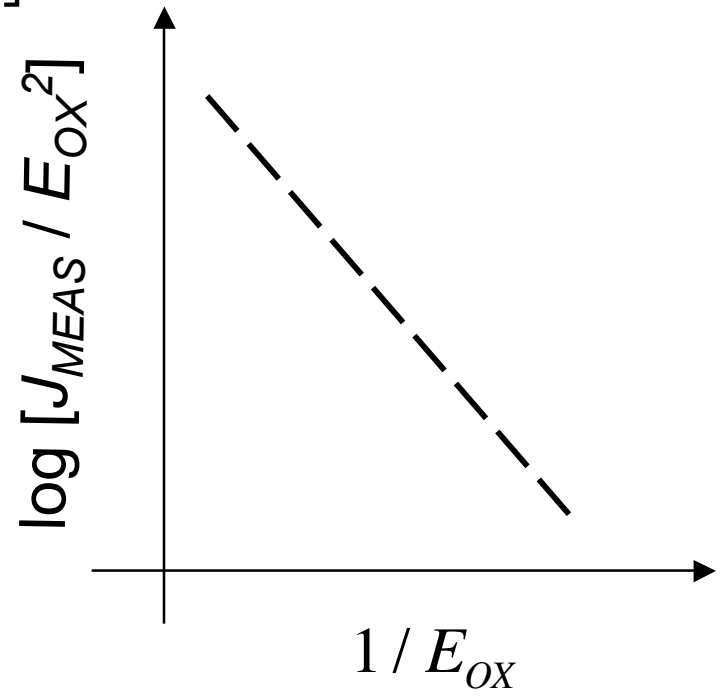
Fowler-Nordheim tunneling (ii)

$$J_{FN} = \frac{q^3 E_{OX}^2}{16\pi^2 \hbar \phi_{OX}} \exp\left[-\frac{4\sqrt{2m^* \phi_{OX}^{3/2}}}{3\hbar q E_{OX}} \right]$$ eqn. (2.209) Taur and Ning

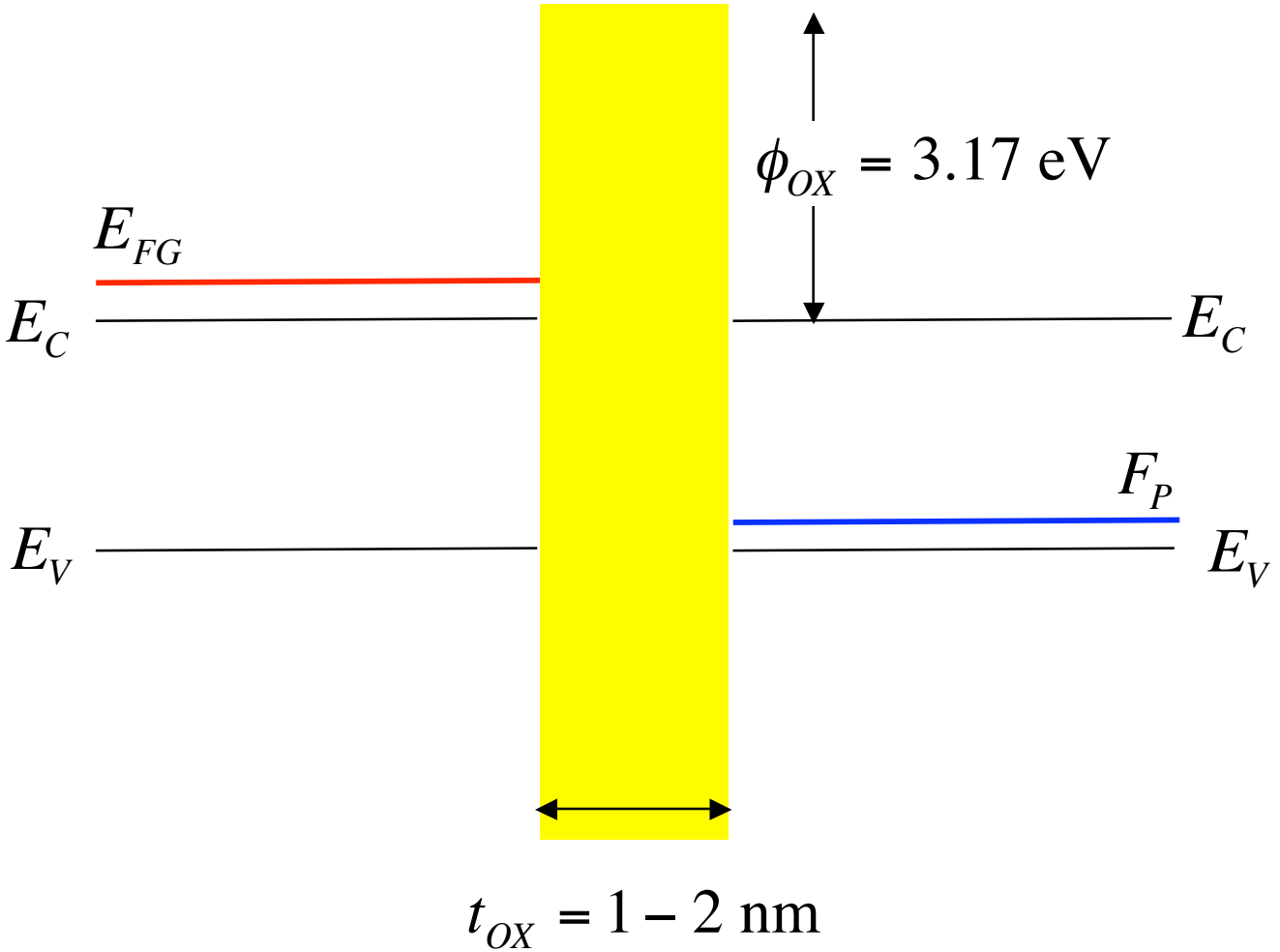
$$J_{FN} / C_1 E_{OX}^2 = \exp\left[-\frac{C_2}{E_{OX}} \right]$$

$$E_{OX} = 8 \text{ MV/cm}$$

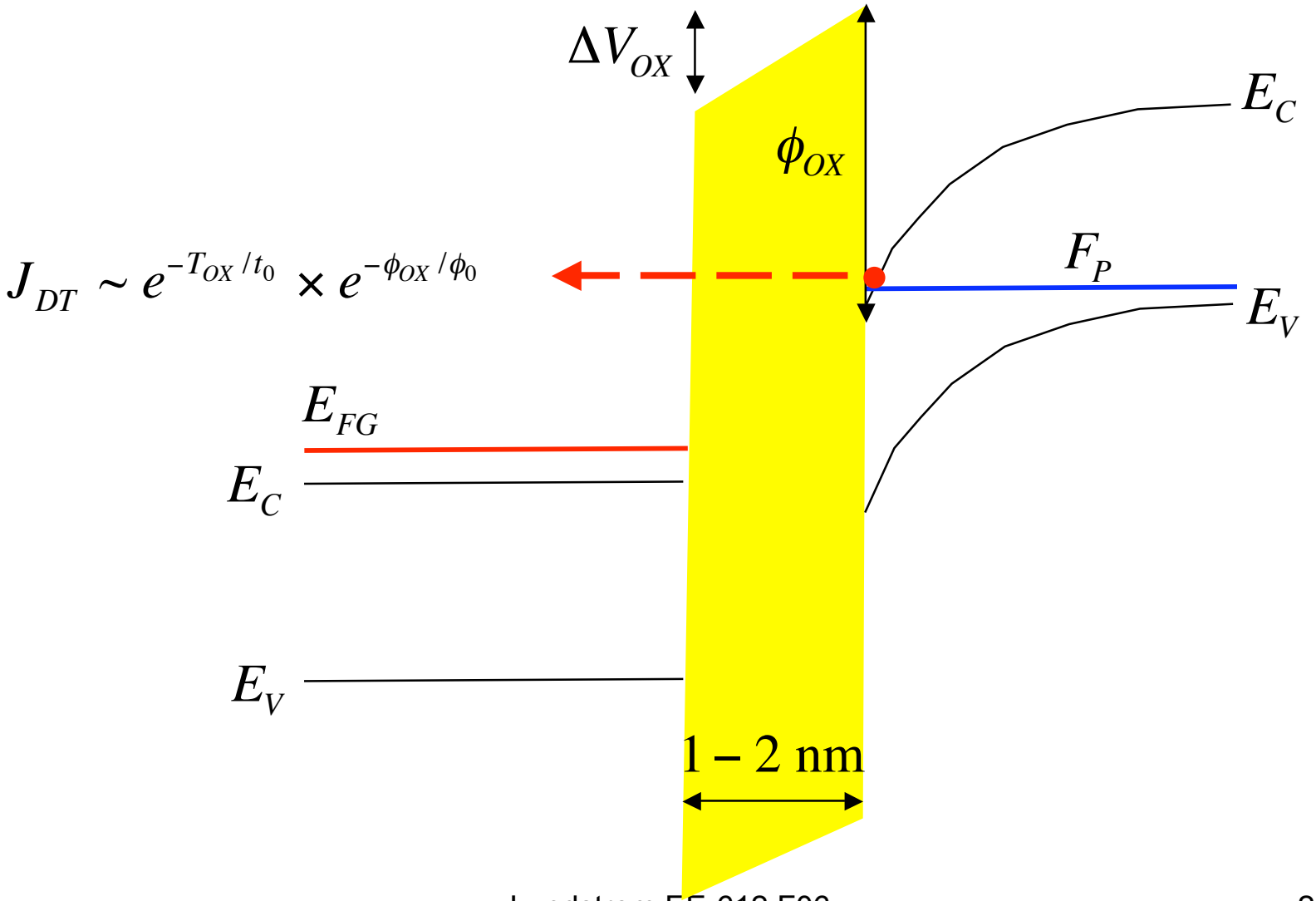
$$J_{FN} = 5 \times 10^{-7} \text{ A/cm}^2$$



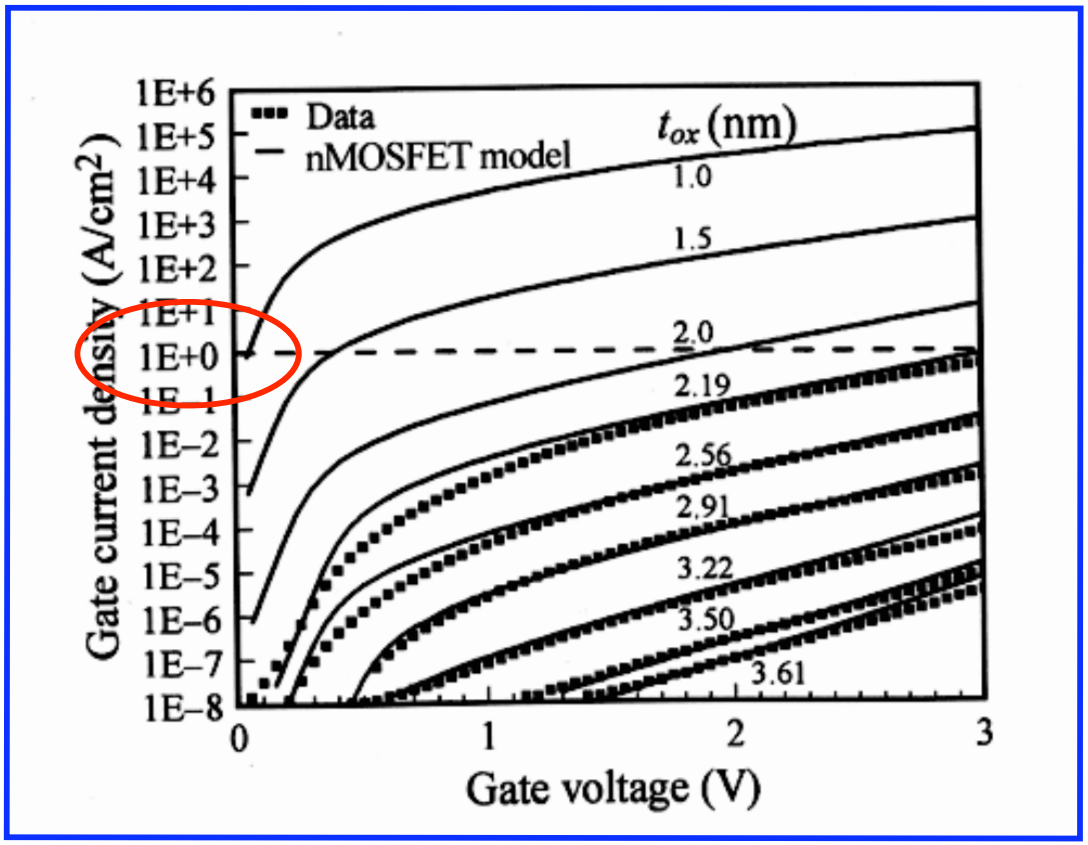
gate leakage (thin oxides)



direct tunneling



direct tunneling in practice



Lo, Buchanan, and Taur, "Modeling and characterization of quantization, polysilicon depletion, and direct tunneling effects in MOSFETs with ultrathin oxides," *IBM J. Res. Develop.*, **43**, pp. 327-337, 1999.

gate leakage at the 70 nm node

is gate leakage a problem at the 70 nm node?

$$A_{GATE} = WL_{GATE} = 1000 \text{ nm} \times 28 \text{ nm} = 2.8 \times 10^{-10} \text{ cm}^2$$

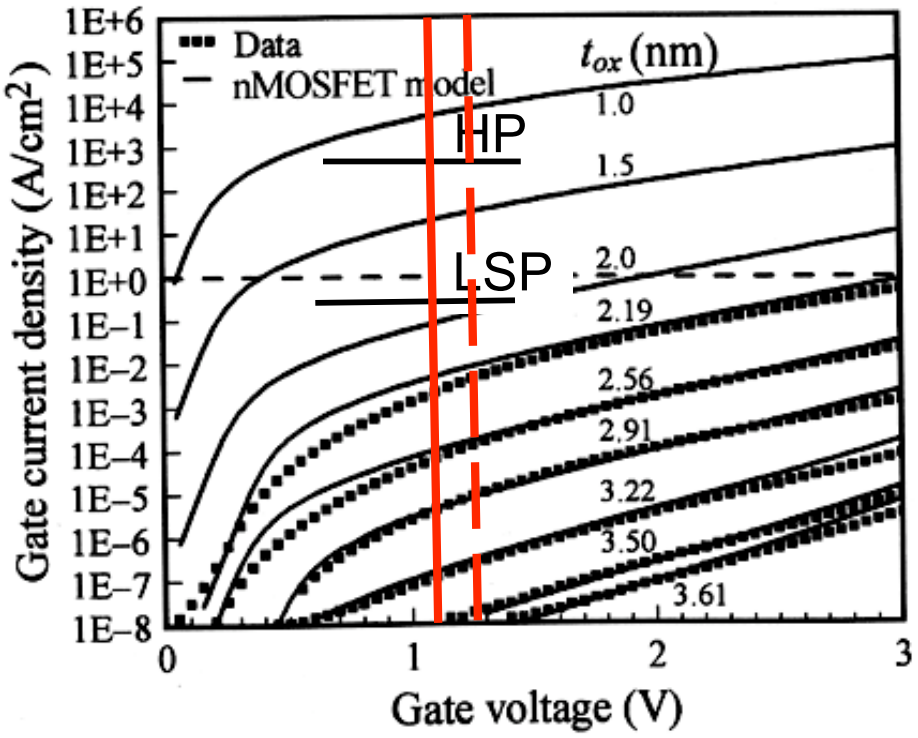
$$I_{OFF}(HP) = 0.15 \ \mu\text{A}/\mu\text{m}$$

$$I_{GATE} < I_{OFF}(HP) \rightarrow J_{GATE} < 540 \text{ A/cm}^2$$

$$I_{OFF}(LSP) = 10^{-5} \ \mu\text{A}/\mu\text{m}$$

$$I_{GATE} < I_{OFF}(LSP) \rightarrow J_{GATE} < 0.04 \text{ A/cm}^2$$

direct tunneling in practice



EOT (70 nm HP) = 1.1 nm

EOT (70 nm LSP) = 2.0 nm

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outline

1) Leakage components
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5) **Scaling and ITRS**

ITRS 2005 Ed.

Table 40a High-Performance Logic Technology Requirements—Near-term

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
L_g: Physical L_{gate} for High Performance logic (nm) [1]	**32**	**28**	**25**	**22**	**20**	**18**	**16**	**14**	**13**
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	**12**	**11**	**11**	**9**	**7.5**	**6.5**	**5**	**5**	
UTB FD (Å)				**9**	**8**	**7**	**6**	**5**	**5**
DG (Å)							**8**	**7**	**6**
Gate Poly Depletion and Inversion-Layer Thickness [3]									
Extended Planar Bulk (Å)	**7.3**	**7.4**	**7.4**	**2.9**	**2.8**	**2.7**	**2.5**	**2.5**	
UTB FD (Å)				**4**	**4**	**4**	**4**	**4**	**4**
DG (Å)							**4**	**4**	**4**
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
Extended Planar Bulk (Å)	**19.3**	**18.4**	**18.4**	**11.9**	**10.3**	**9.2**	**7.5**	**7.5**	
UTB FD (Å)				**13**	**12**	**11**	**10**	**9**	**9**
DG (Å)							**12**	**11**	**10**
$J_{g.limit}$: Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm^2)	**1.88E+02**	**5.36E+02**	**8.00E+02**	**9.09E+02**	**1.10E+03**	**1.56E+03**	**2.00E+03**	**2.43E+03**	

oxide scaling

[2] For a gate dielectric of thickness Td and relative dielectric constant κ, κ/3.9), where 3.9 is the relative dielectric constant of thermal silicon dioxide. …. It is projected that **high-κ gate dielectric will be required by 2008 to control the gate leakage** (see the text for further discussion on this point.) Note that the **rate of scaling of EOT is quite slow from 2005 through 2007 to keep the gate leakage current within the specified limits while utilizing silicon oxy-nitride for the gate dielectric.** However, there is **a sharp EOT decrease in 2008, when we assume that high-κ gate dielectric will be implemented.** Red coloring for 2008 and beyond reflects the projected implementation of high-κ gate dielectric. The color is red because it is felt that the solutions for EOT below 1.0 nm are not understood. …

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high-k gate dielectrics

$$J_{DT} \sim e^{-t_{OX}/t_0} \times e^{-\phi_{OX}/\phi_0} \qquad C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$J_{DT} \sim e^{-t_{INS}/t_0} \times e^{-\phi_{INS}/\phi_0}$$

$$C_{INS} = \frac{\varepsilon_{INS}}{t_{INS}} = \frac{\varepsilon_{OX}}{\varepsilon_{OX}} \frac{\varepsilon_{INS}}{t_{INS}} = \frac{\varepsilon_{OX}}{\left(\varepsilon_{OX} t_{INS} / \varepsilon_{INS}\right)} = \frac{\varepsilon_{OX}}{EOT}$$

If $\kappa_{INS} >> \kappa_{OX}$, then we can use a thicker t_{INS}, get a higher C_{INS}, and lower J_{DT}

oxide scaling

[5] **Jg,limit** is the maximum allowed gate leakage current density at 25°C, and it is measured with the gate biased to Vdd and the source, drain, and substrate all set to ground. Jg,limit is related to Isd,leak, the nominal subthreshold leakage current per micron device width (see Note [8] below). The yellow and red coloring follows that of EOT (see Note [2] above).

leakage current

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FDSOI (A/cm^2)				**7.73E+02**	**9.50E+02**	**1.22E+03**	**1.38E+03**	**2.07E+03**	**2.23E+03**
DG (A/cm^2)							**6.25E+02**	**7.86E+02**	**8.46E+02**
V_{dd}: Power Supply Voltage (V) [6]	**1.1**	**1.1**	**1.1**	**1**	**1**	**1**	**1**	**0.9**	**0.9**
$V_{t,sat}$: Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	**195**	**168**	**165**	**160**	**159**	**151**	**146**	**148**	
UTB FD (mV)				**169**	**168**	**167**	**170**	**166**	**167**
DG (mV)							**181**	**184**	**185**
$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (μA/μm)	**0.06**	**0.15**	**0.2**	**0.2**	**0.22**	**0.28**	**0.32**	**0.34**	
UTB FD (μA/μm)				**0.17**	**0.19**	**0.22**	**0.22**	**0.29**	**0.29**
DG (μA/μm)							**0.1**	**0.11**	**0.11**

oxide scaling

[8] **Isd,leak: subthreshold leakage current** is defined as the NMOSFET source current per micron of device width, at 25°C, with the drain bias set equal to Vdd and with the gate, source, and substrate biases set to zero volts. **Total NMOS off-state leakage current (Ioff) is the NMOSFET drain current per micron of device width at 25°C, and is the sum of the NMOS subthreshold, gate, and junction leakage current (which includes band-to-band tunneling and gate induced drain leakage [GIDL]) components.** The subthreshold leakage current is assumed to be larger than the junction leakage current component at either 25°C or high-temperature conditions, but see Note [5] for the relation between Isd,leak and gate leakage current density. The yellow and red coloring follows that of Vt,sat (see Note 7 above) because Vt,sat is a critical determinant of Isd,leak. The above subthreshold, gate, and junction leakage current scaling scenario also applies to PMOS devices.

outline

1) Leakage components
2) Band to band tunneling
3) Gate-induced drain leakage
4) Gate leakage
5) Scaling and ITRS