EE-612:
Lecture 22:
CMOS Process Steps

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NCN

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outline

1) Unit Process Operations
2) Process Variations

unit process operations

1) Oxidation
2) Diffusion
3) Ion Implantation
4) RTA/RTP
5) Chemical Vapor Deposition
6) Lithography
7) Etching
8) Metalization
9) Well Structures
10) Isolation
11) Source / Drain structures

useful references

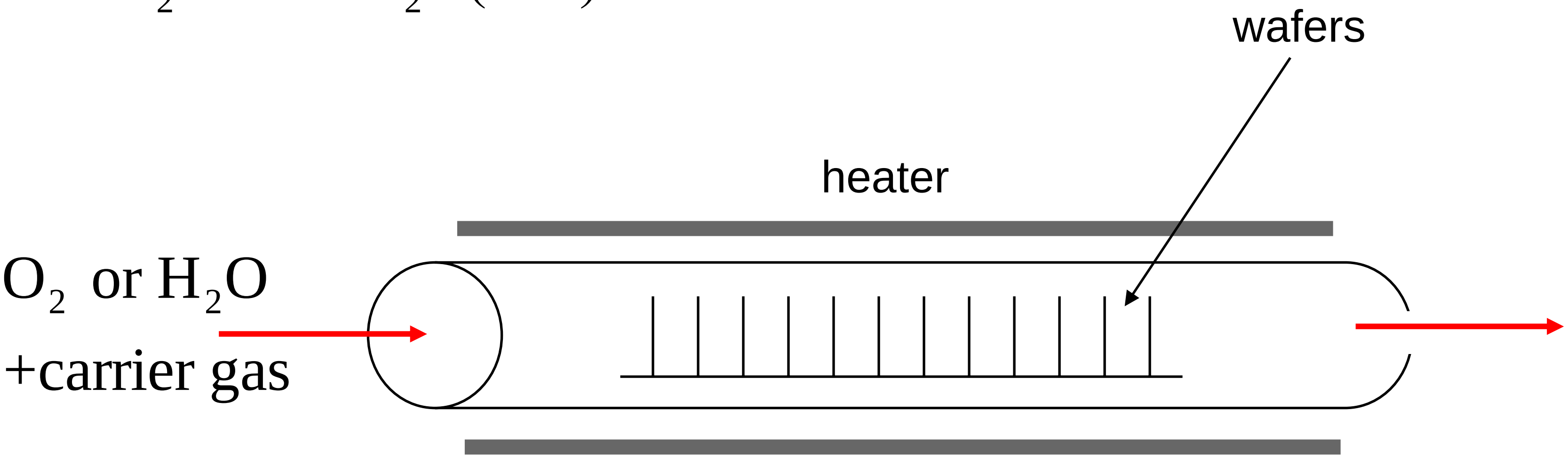
1) J.D. Plummer, M.D. Deal, P.B. Griffin, *Silicon VLSI Technology, Fundamentals, Practice, and Modeling*, Prentice Hall, Upper Saddle River, NJ, 2000.

2) S.A. Campbell, *The Science and Engineering of Microelectronic Fabrication*, 2nd Ed., Oxford Univ. Press, New York, 2001.

oxidation

$\mathrm{Si} + \mathrm{O_2} \rightarrow \mathrm{SiO_2}$ (dry)

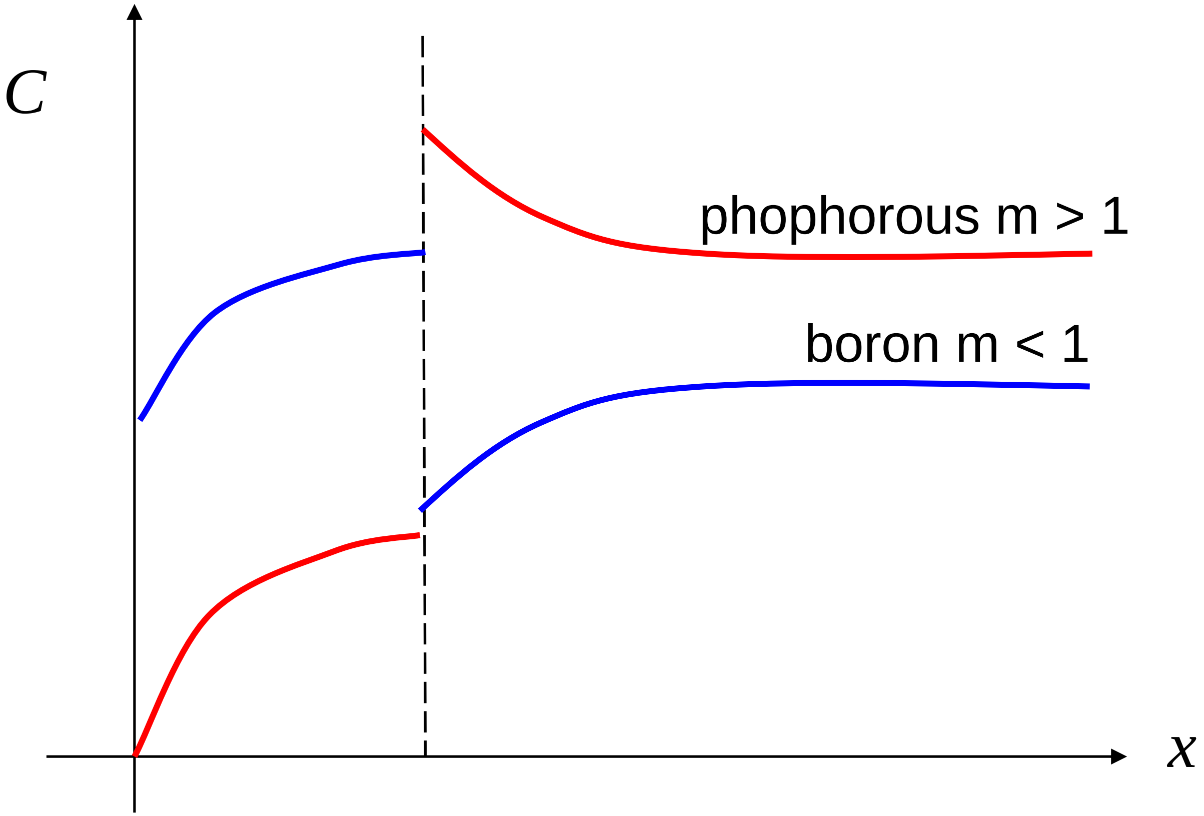
$\mathrm{Si} + \mathrm{H_2O} \rightarrow \mathrm{SiO_2}$ (wet)



$T = 800 - 1100\ ^{\circ}\mathrm{C}$

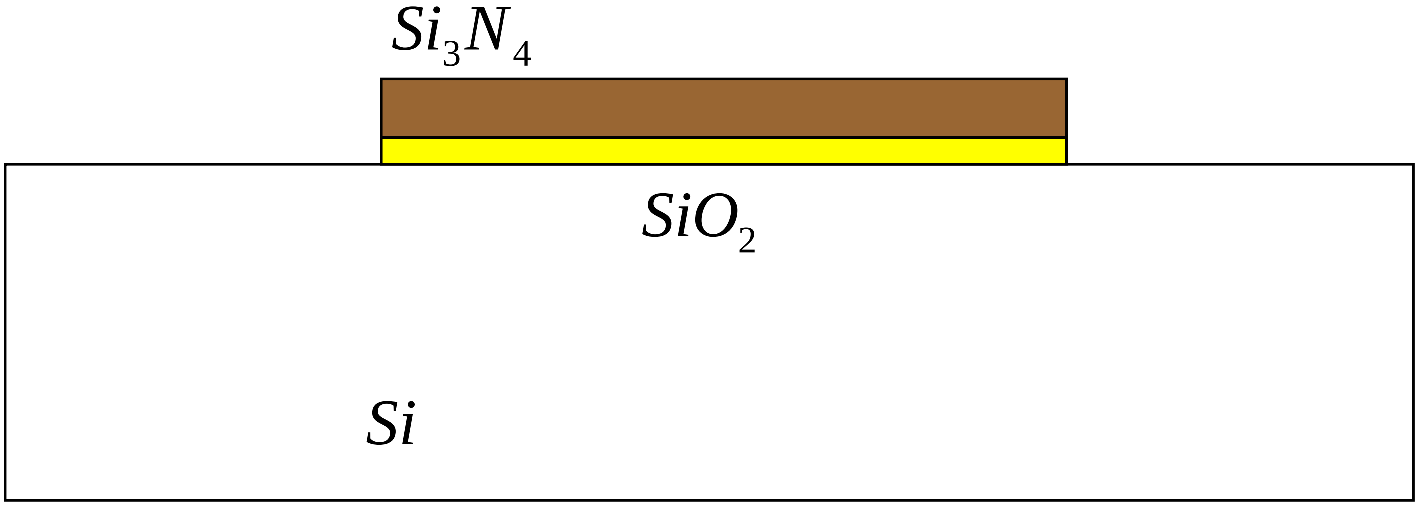
fused quartz
furnace tube

oxidation and doping

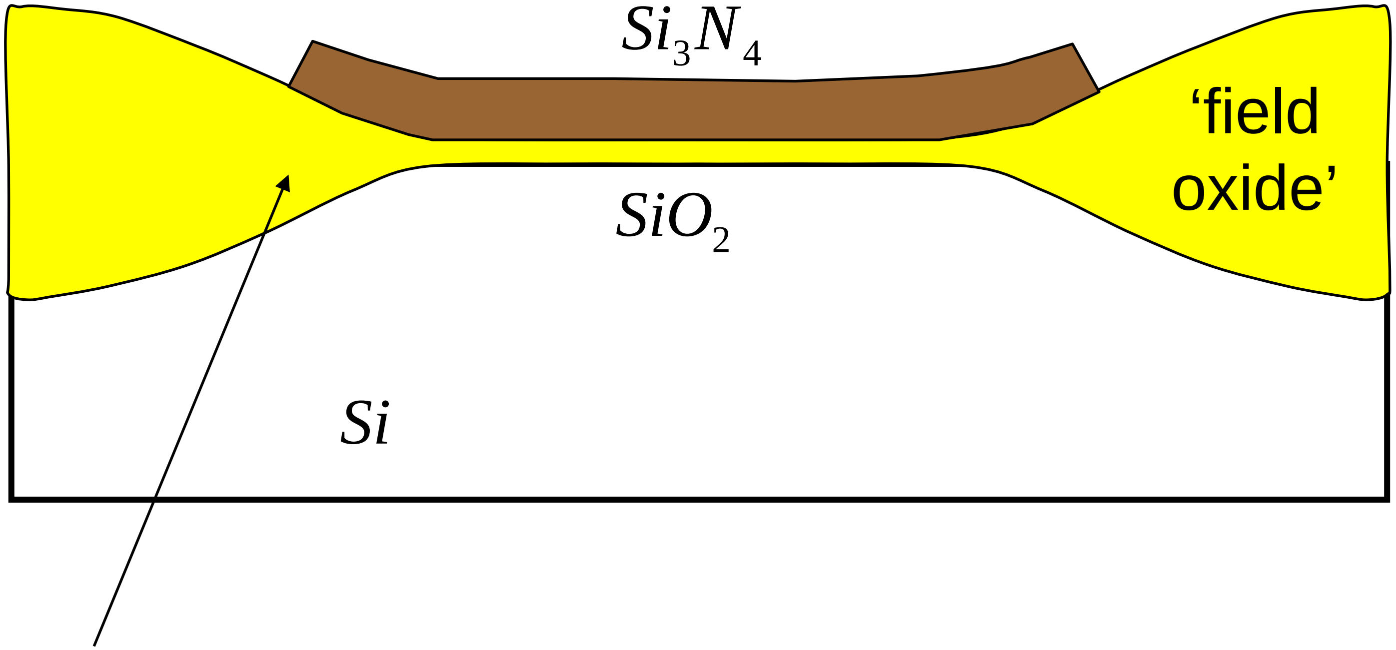


$$m = \frac{C_{Si}}{C_{SiO_2}}$$

local oxidation



local oxidation (LOCOS)



Si_3N_4

‘field oxide’

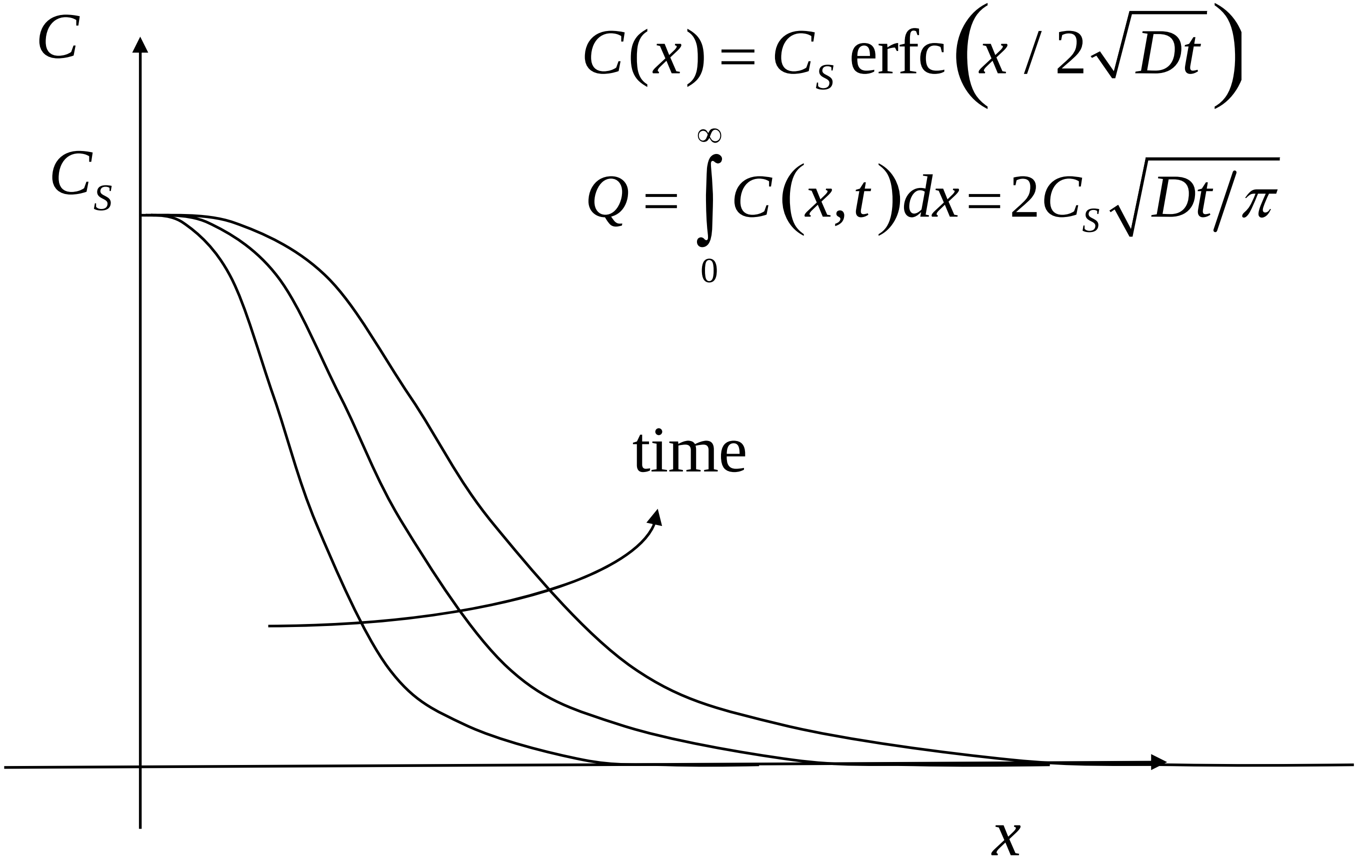
SiO_2

Si

'bird's beak'

constant source diffusion

dopant-containing gas (e.g. $POCl_3$)

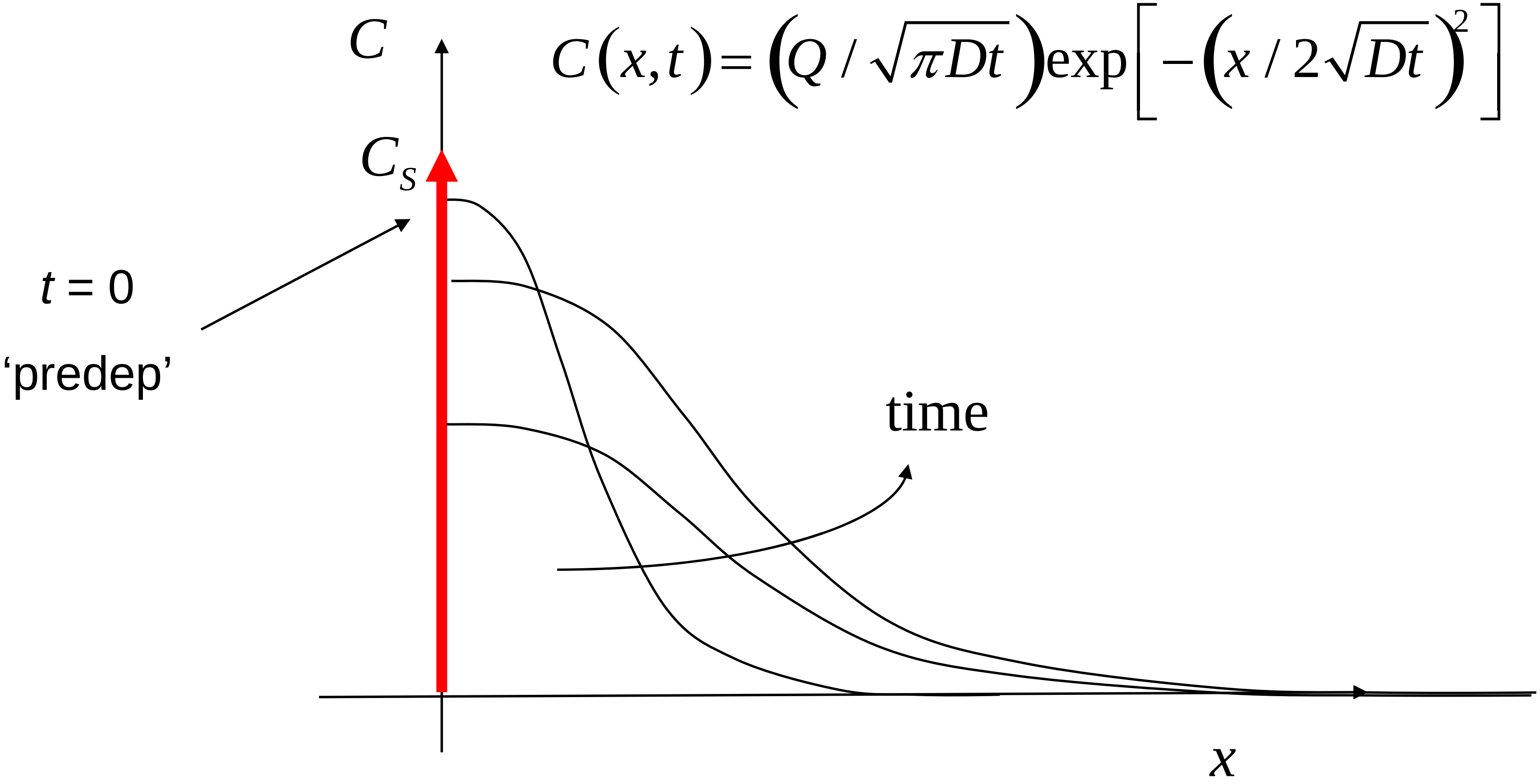


$$C(x) = C_S \operatorname{erfc}\left(x / 2\sqrt{Dt}\right)$$

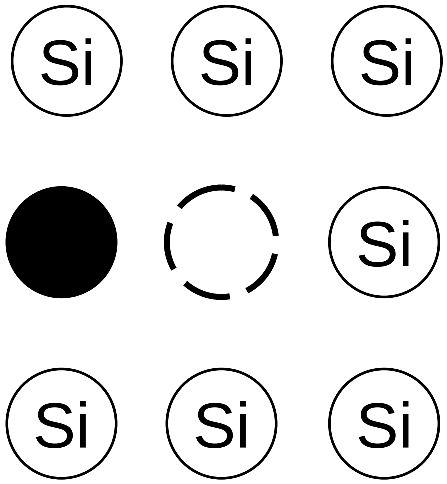
$$Q = \int_0^\infty C\left(x,t\right)dx = 2C_S\sqrt{Dt/\pi}$$

Limited source diffusion

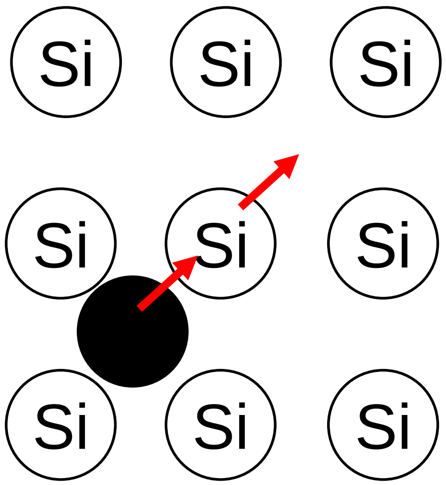
$$C(x,t)=\left(Q/\sqrt{\pi Dt}\right)\exp\left[-\left(x/2\sqrt{Dt}\right)^{2}\right]$$



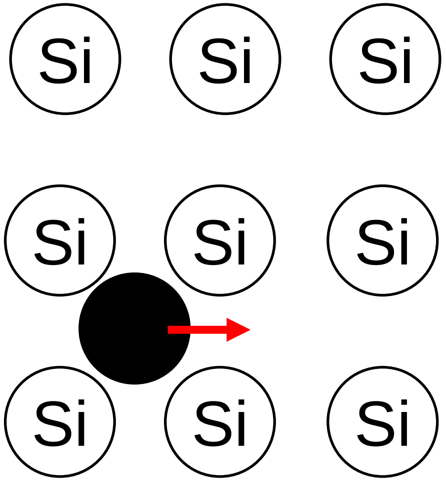
diffusion



substitutional



interstitialcy



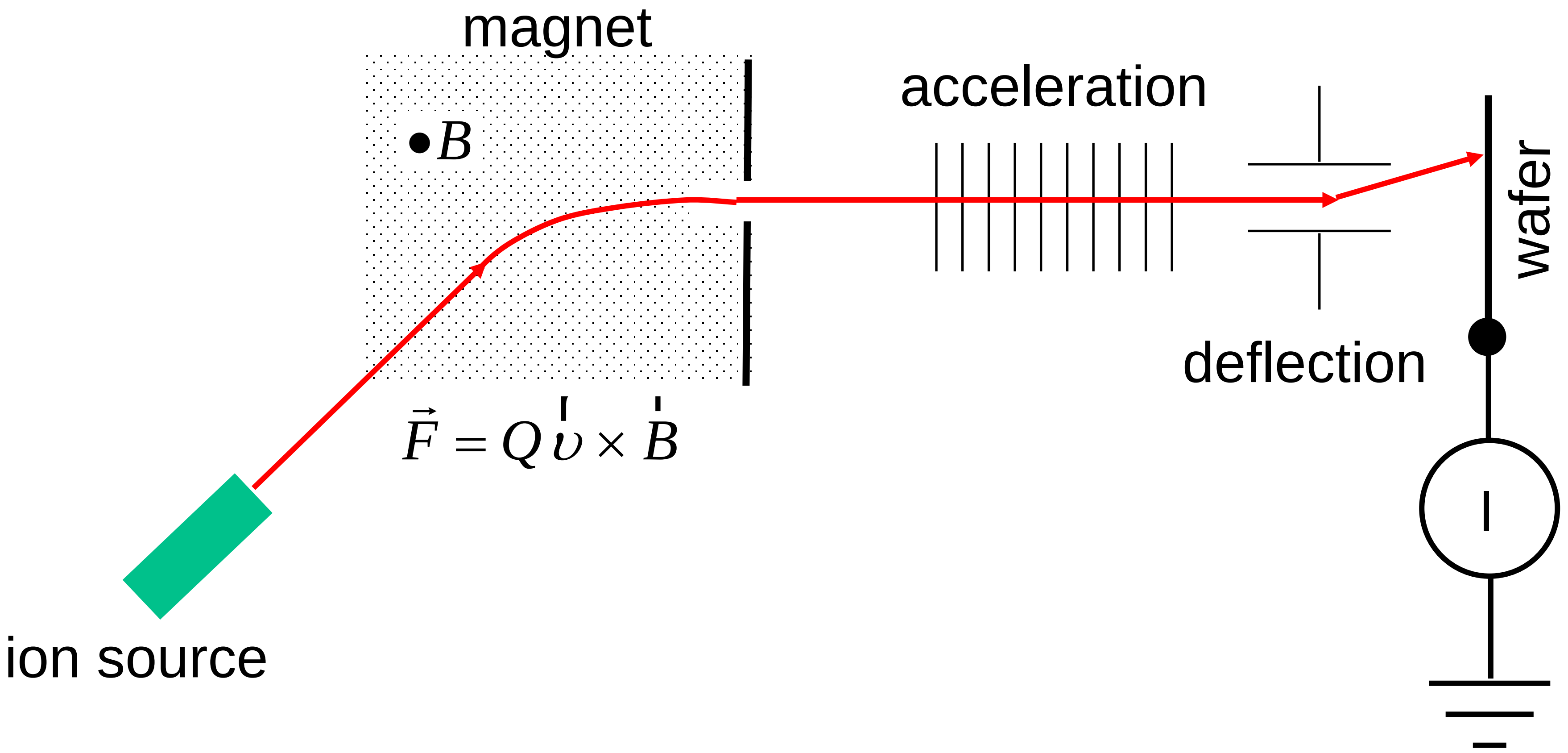
interstitial

$$D(T) = D_0 e^{-E_A/k_B T}$$

“oxidation enhanced diffusion’

ion implantation

energetic ions bombard silicon wafer



magnet

$\bullet B$

acceleration

wafer

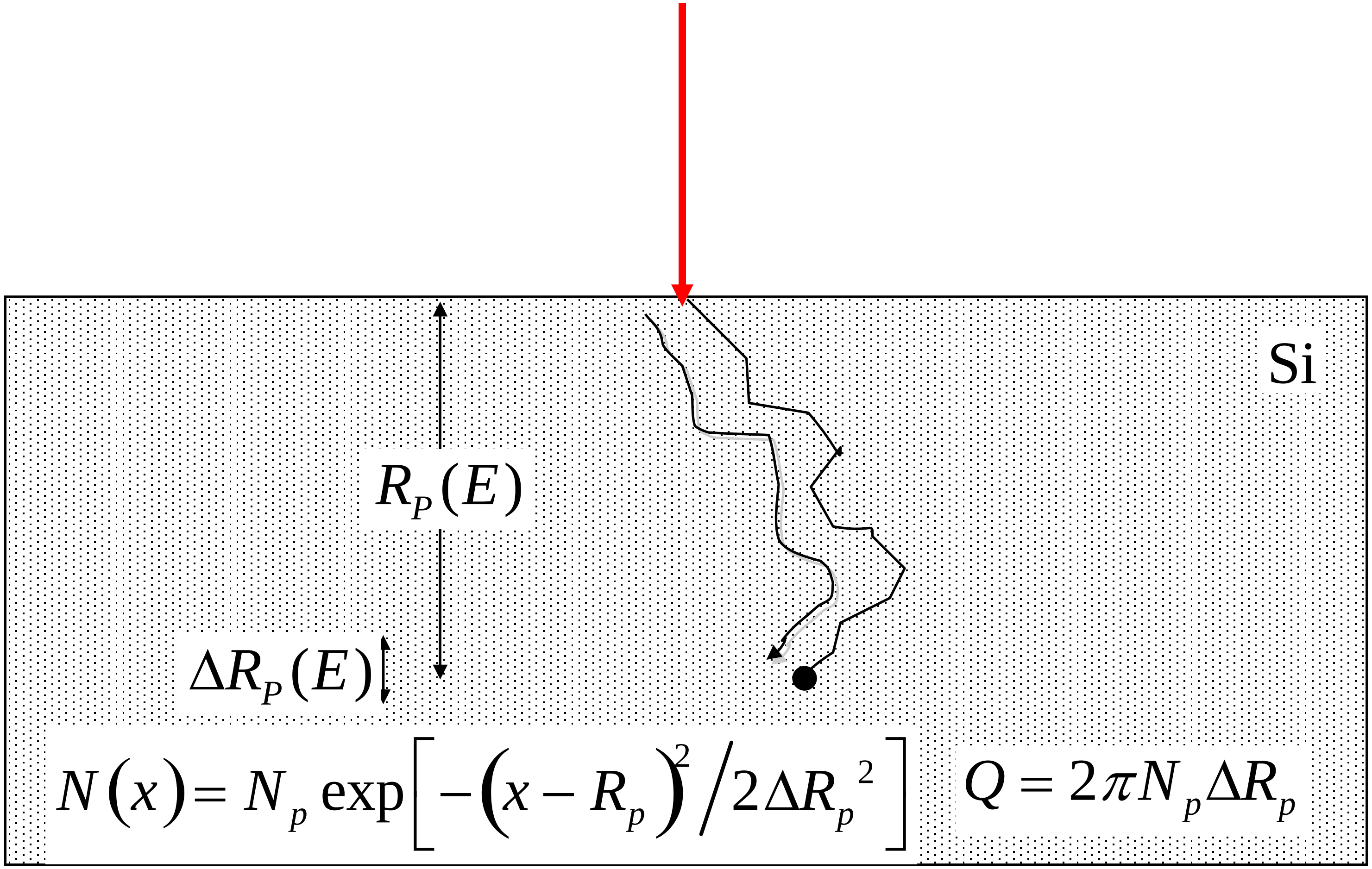
deflection

$$\vec{F} = Q\,\vec{\upsilon} \times \vec{B}$$

I

ion source

ion implantation

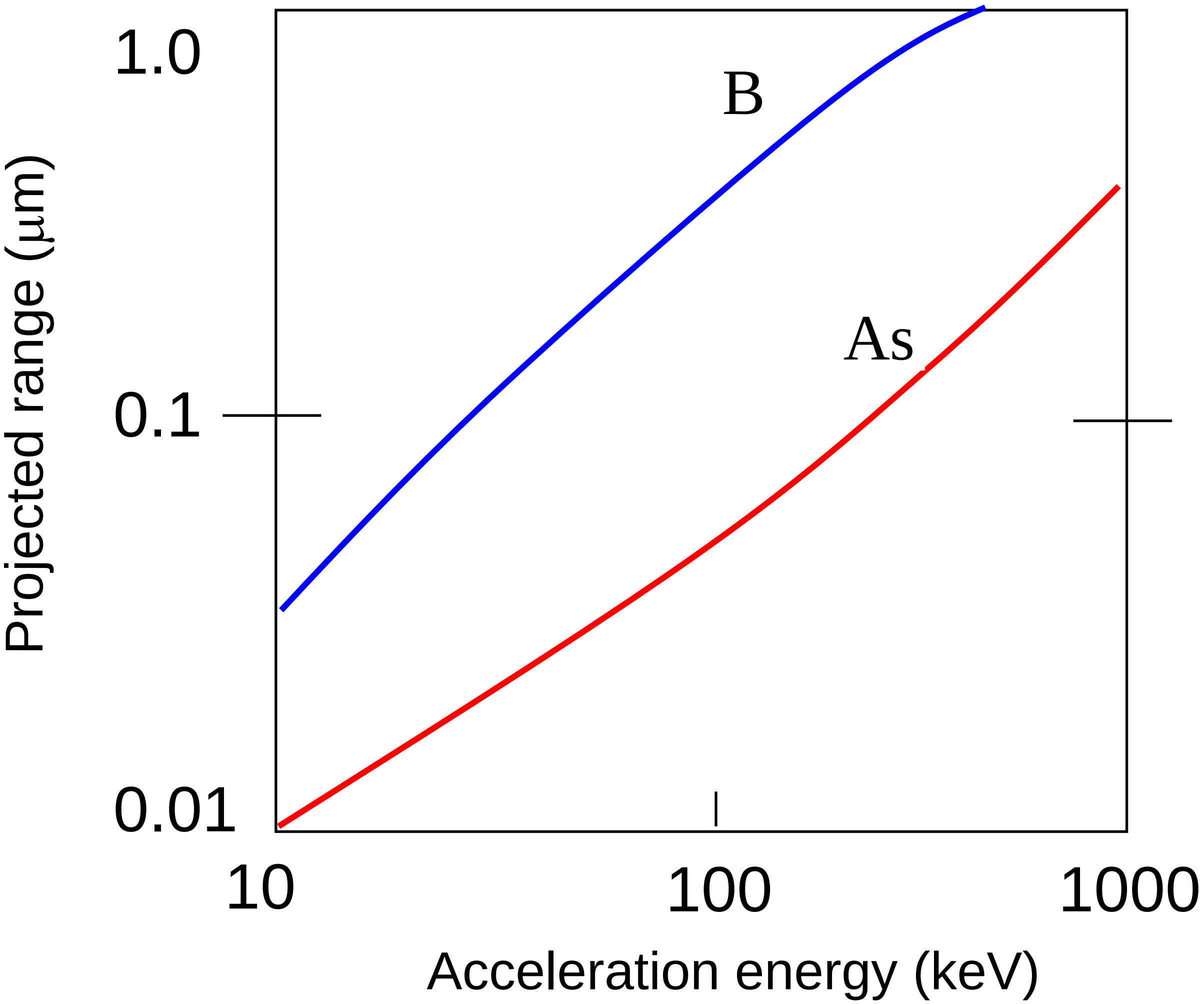


$$N(x) = N_p \exp\left[-\left(x - R_p\right)^2 / 2\Delta R_p{}^2\right]$$

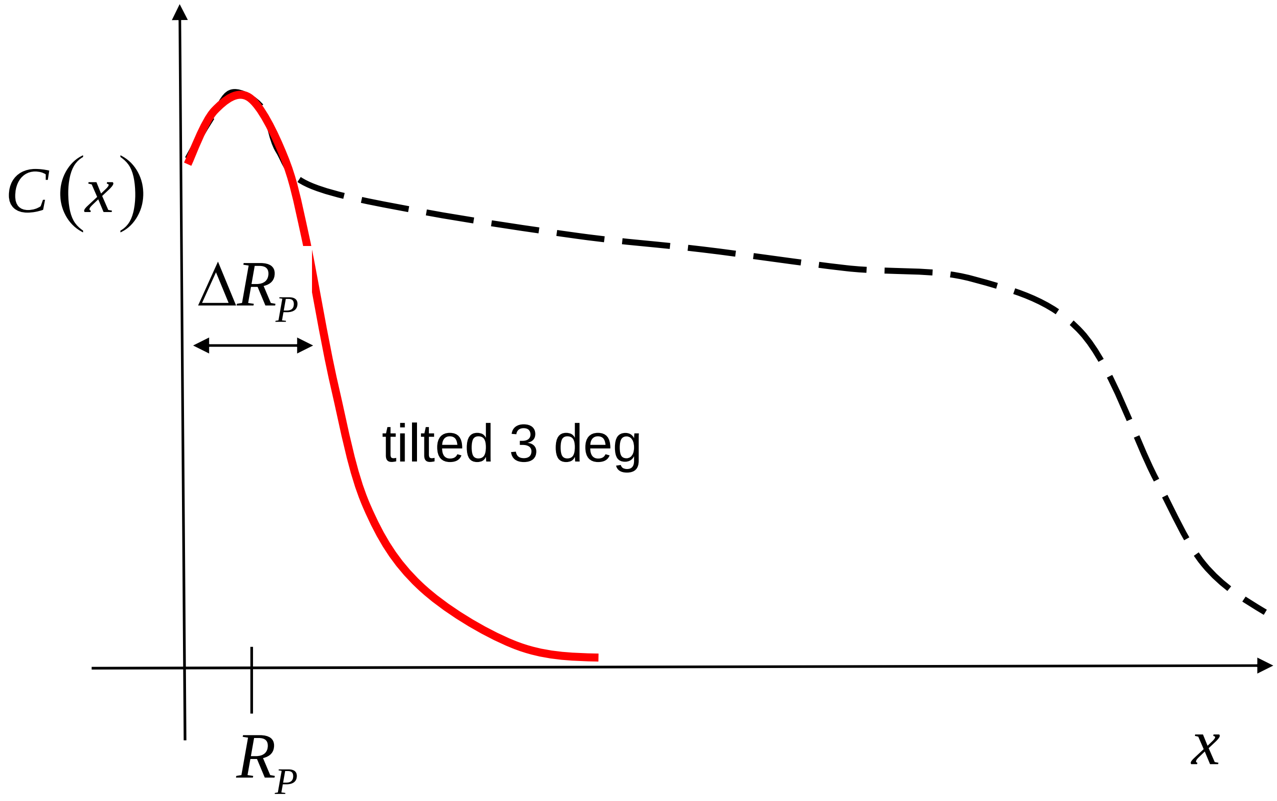
$$Q = 2\pi N_p \Delta R_p$$

implant damage (anneal)

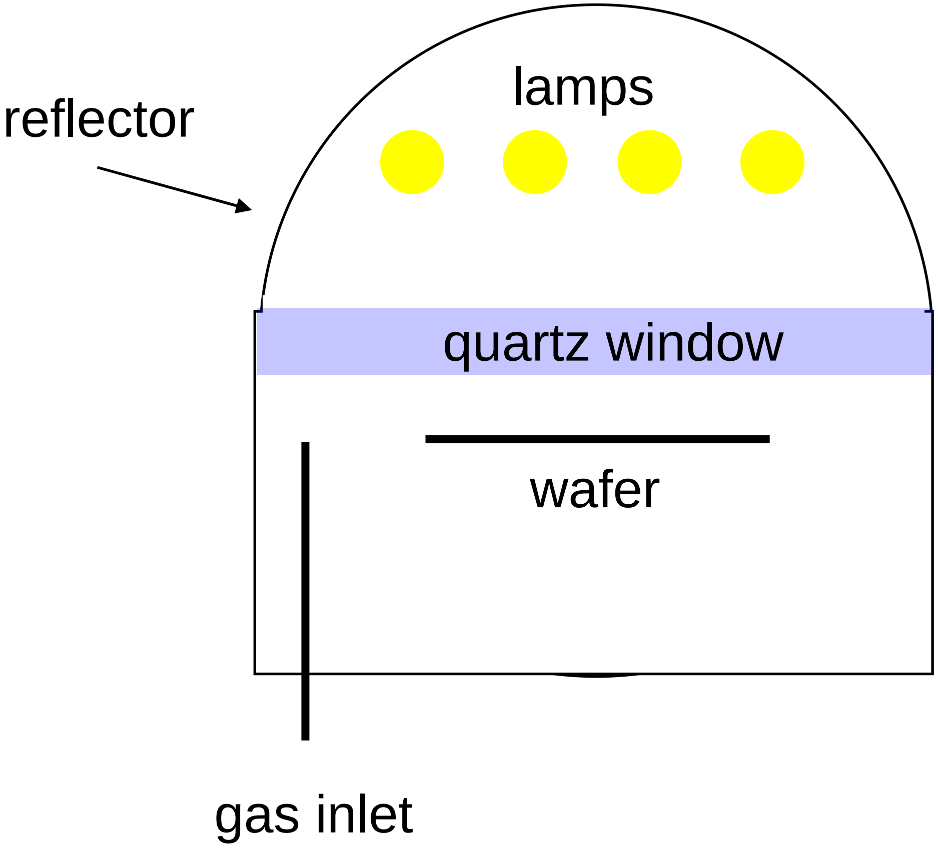
ion implantation (ii)



channeling



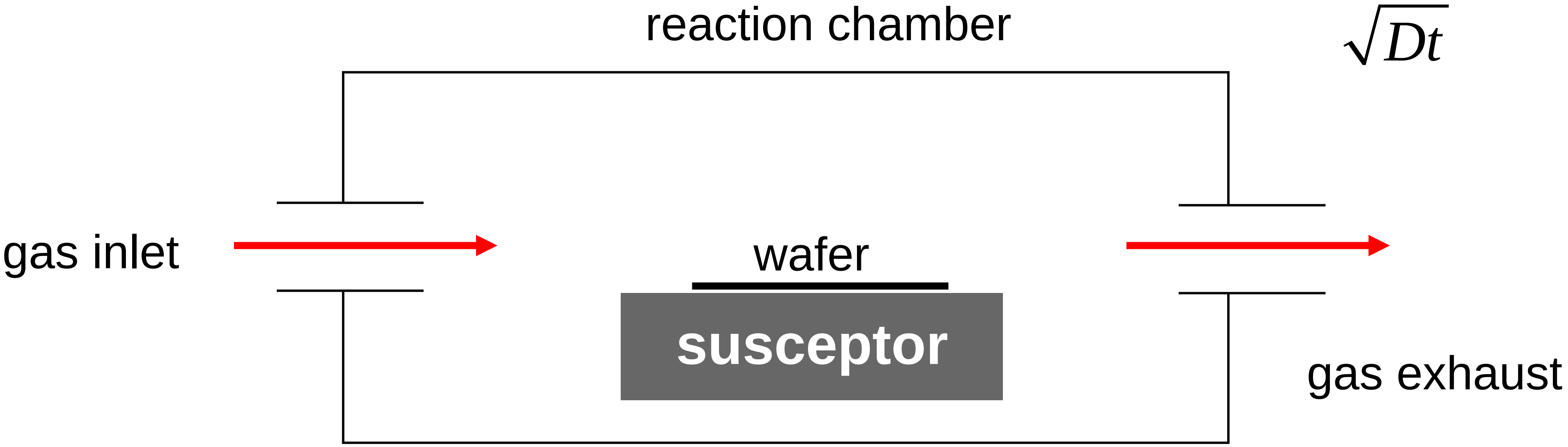
rapid thermal annealing



thermal budget

$\sqrt{Dt}$

chemical vapor deposition

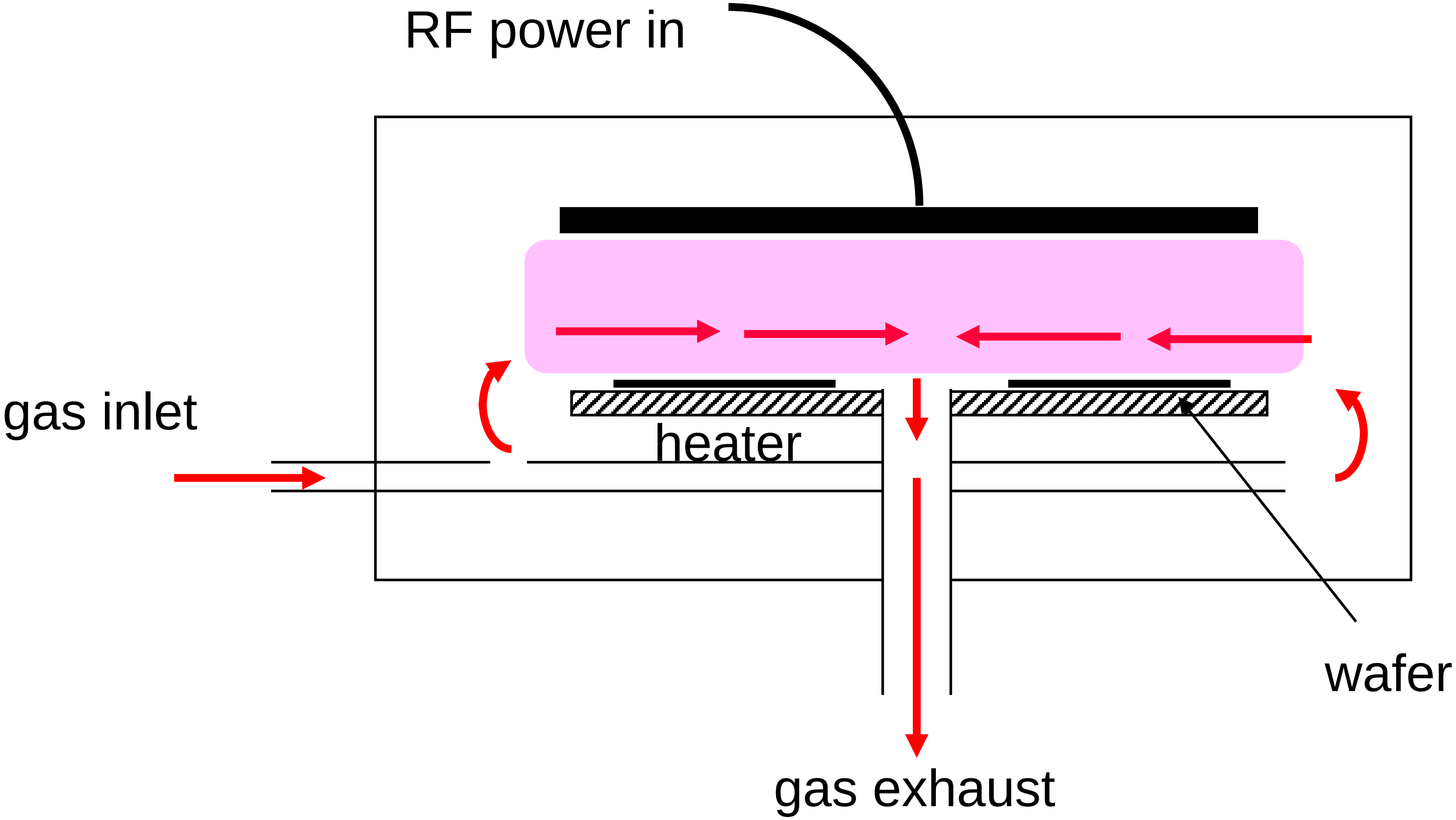


$2SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$ silicon nitride

$SiH_4 \rightarrow Si + 2H_2$ poly silicon

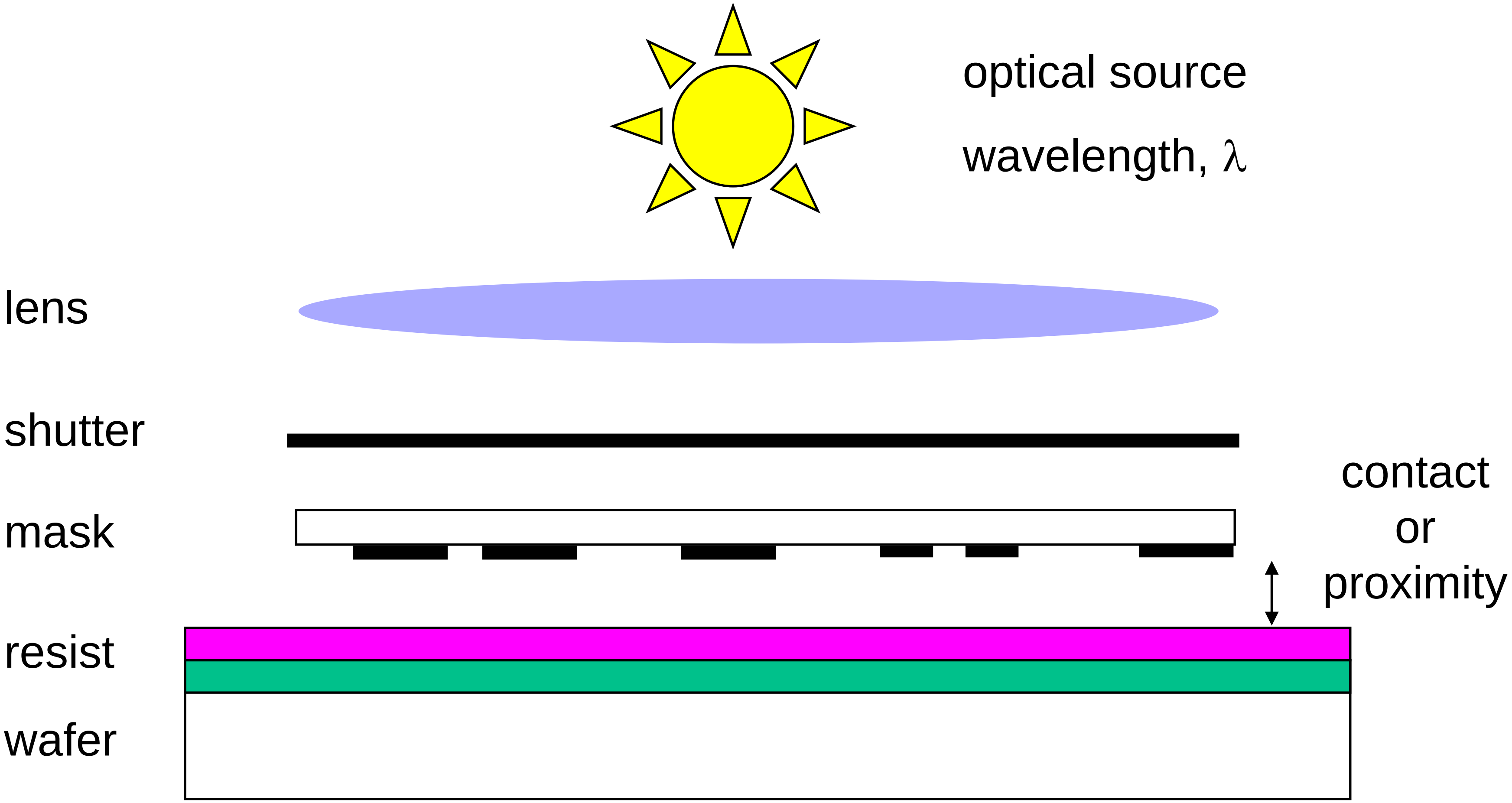
$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$ silicon dioxide

plasma CVD / etching



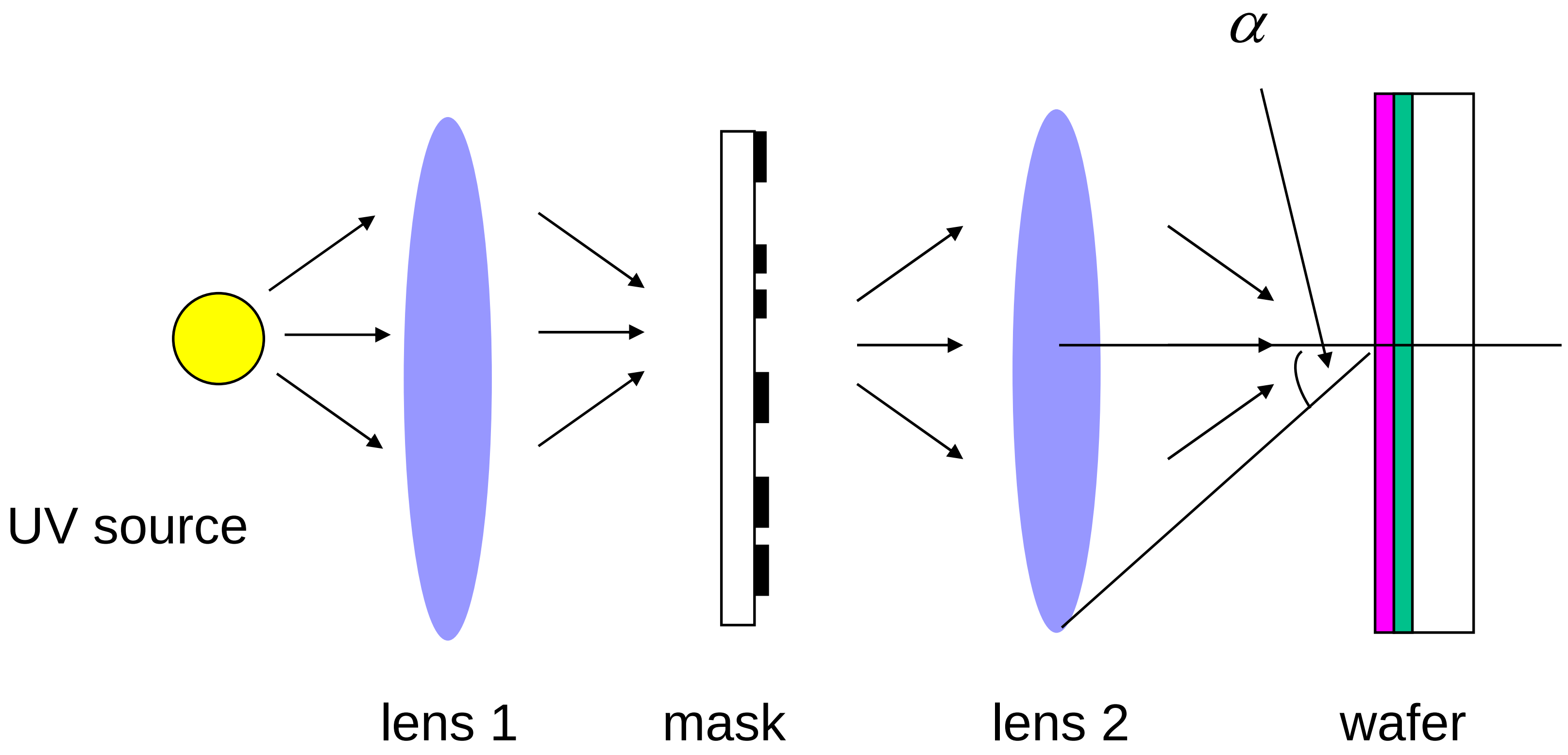
lower temperature reduces thermal budget $\sqrt{Dt}$

lithography

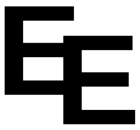


expose, develop, etch

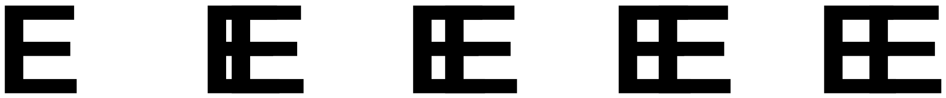
projection printing



registration errors



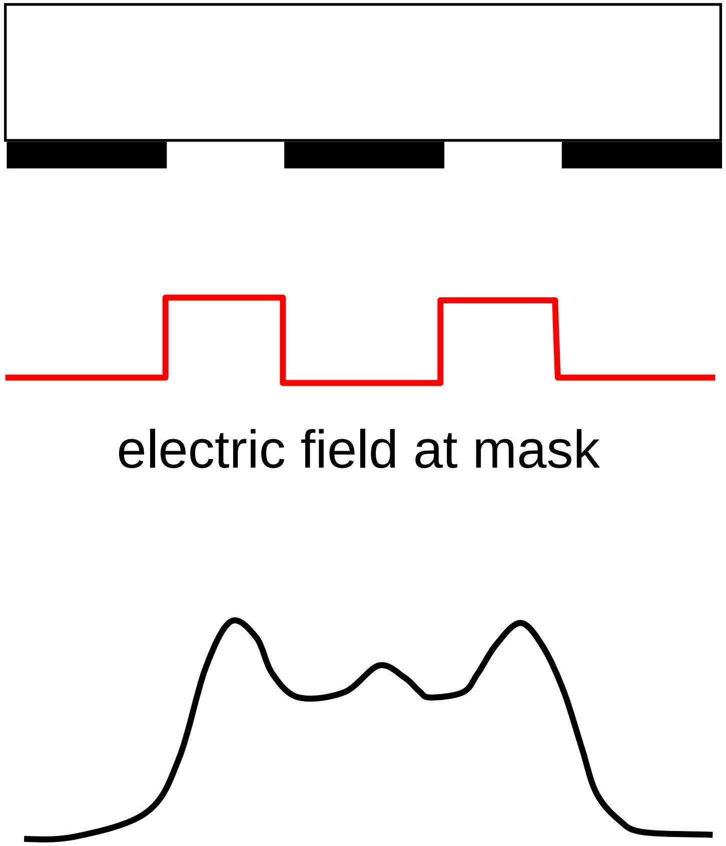
misalignment



run out

phase shift lithography

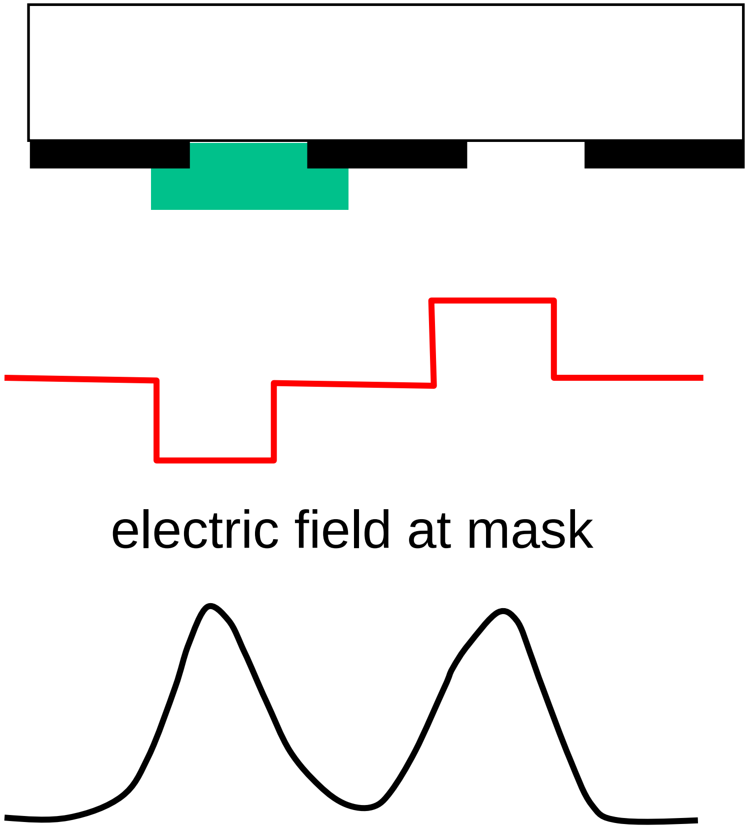
conventional mask



electric field at mask

intensity at wafer

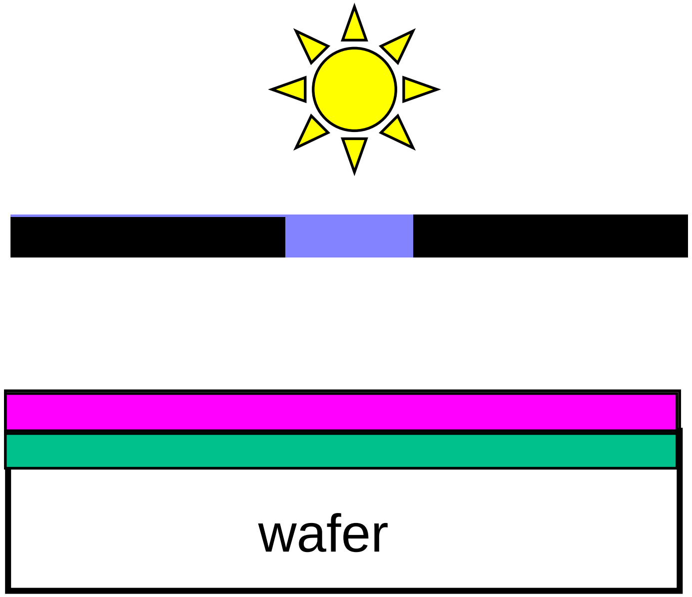
phase shift mask



electric field at mask

intensity at wafer

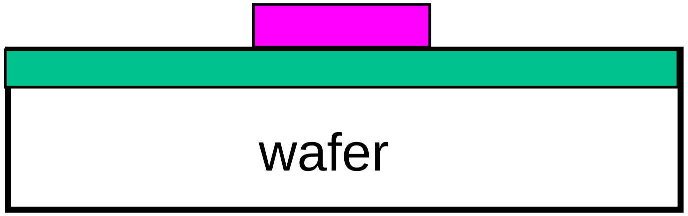
pattern transfer



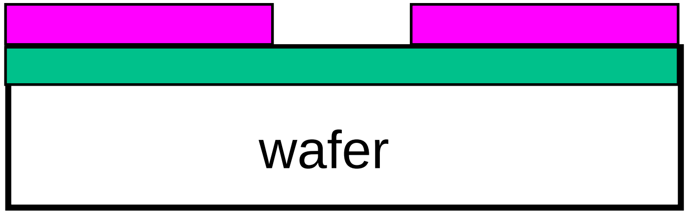
resist:

optically sensitive polymer which, when exposed to UV changes its solubility in specific chemicals

negative resist
(**less soluble** after exposure)



positive resist
(**more soluble** after exposure)



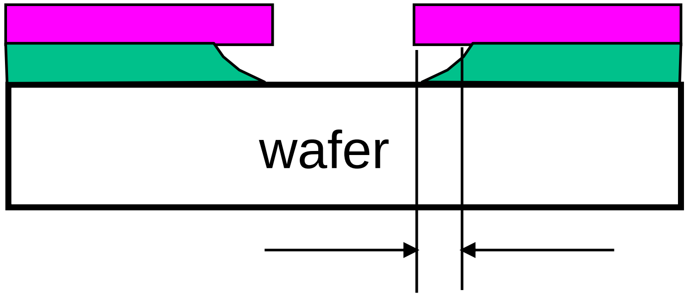
etching

wet chemical etching

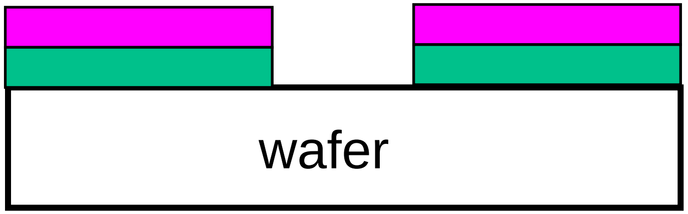
(isotropic)

dry etching (plasma or reactive ion etching - RIE)

(anisotropic)



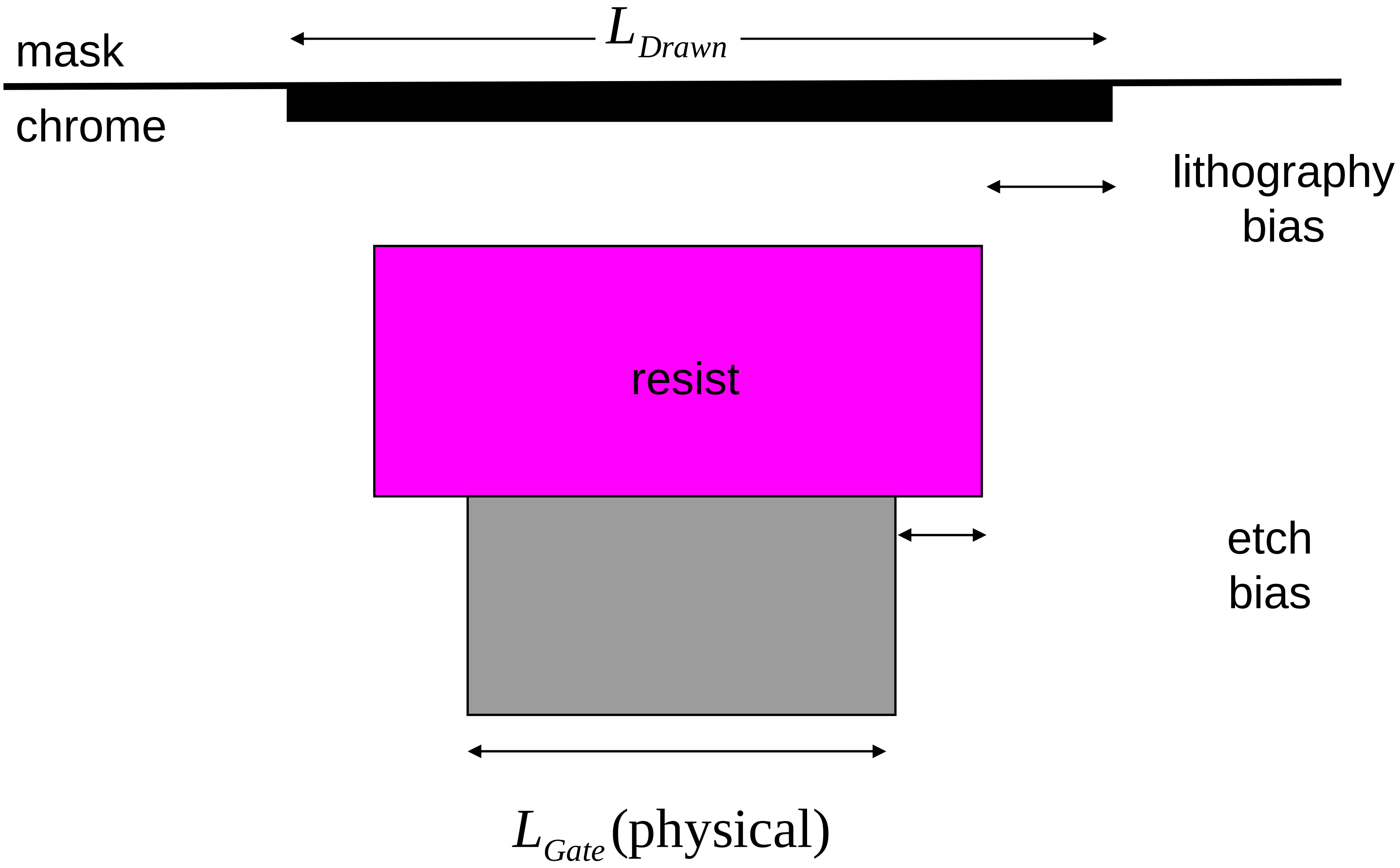
undercut



chemicals react with underlying material, but not resist

ionized gases react with underlying material, but not resist

pattern transfer (ii)



metalization

10 Interconnect

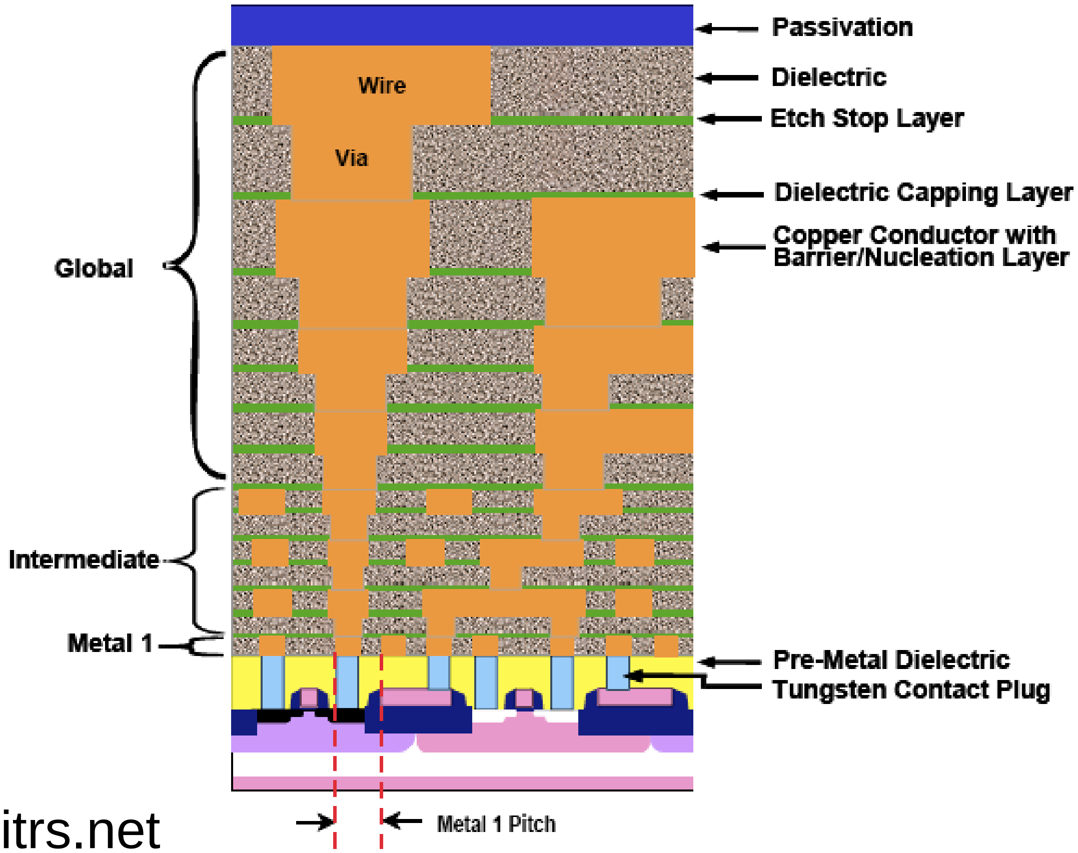


Figure 70 Cross-section of Hierarchical Scaling—MPU Device

Tungsten (W) plugs for first layer metal dep
CMP

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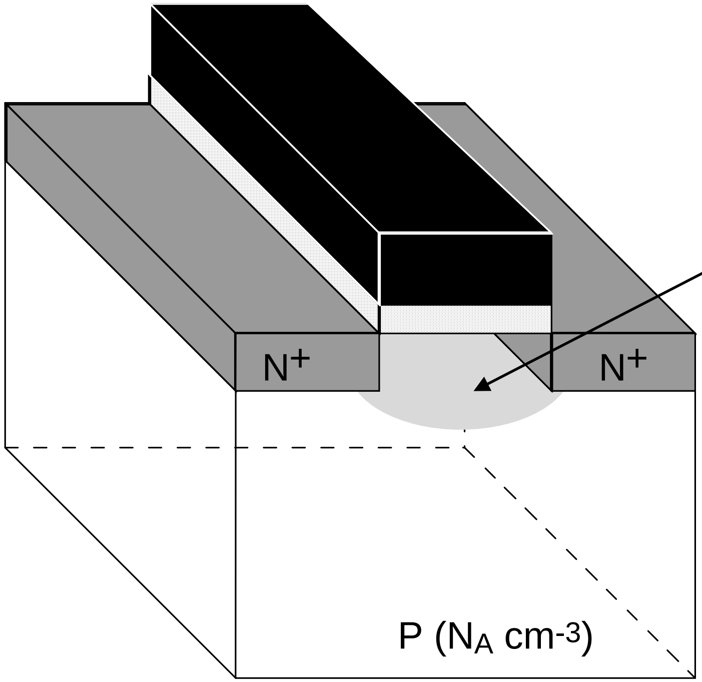
outline

1) Unit Process Operations

2) Process Variations

discrete doping effects



$$V = W \times L \times x_j$$

example:

$L =$ 50 nm

$W =$ 100 nm

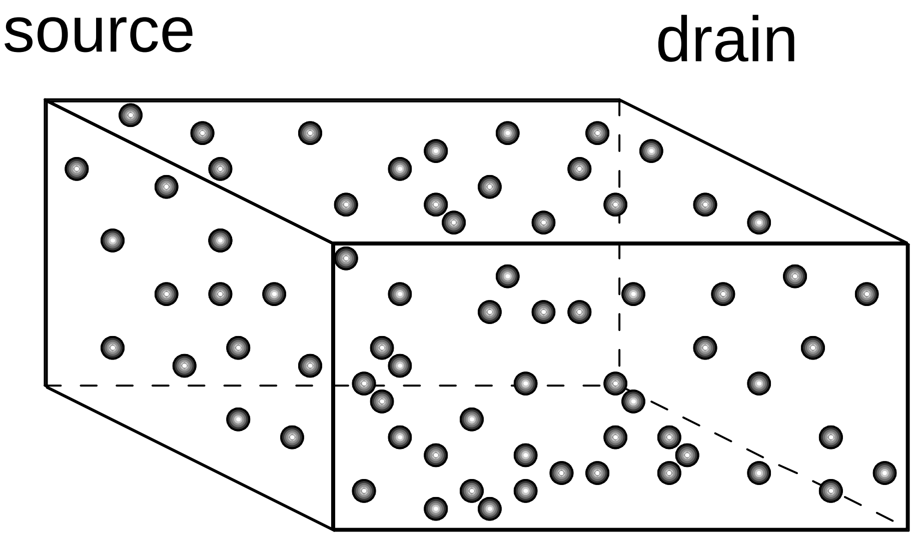
$x_j =$ 25 nm

$N_A =$ 10^{18} cm^{-3}

$N_{TOT} = 125$

Number of dopants in the critical volume is a **statistical quantity**

discrete doping effects (ii)



Effects:

1) σ_{VT} (10’s of mV)

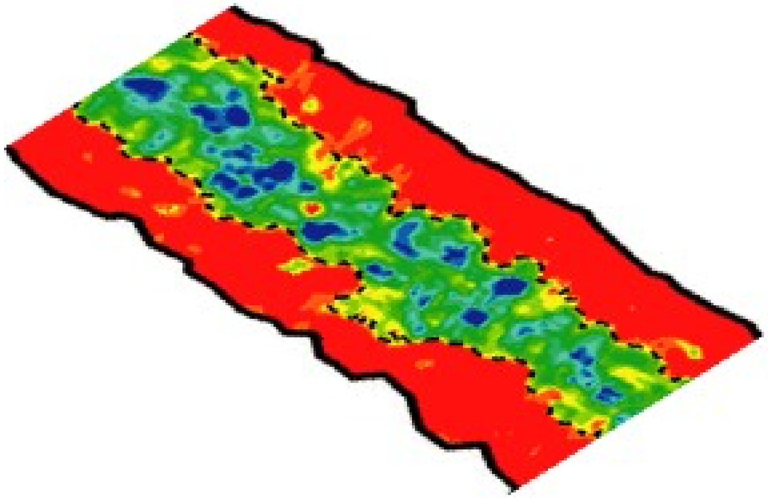
2) lower avg. V_T (10’s of mV)

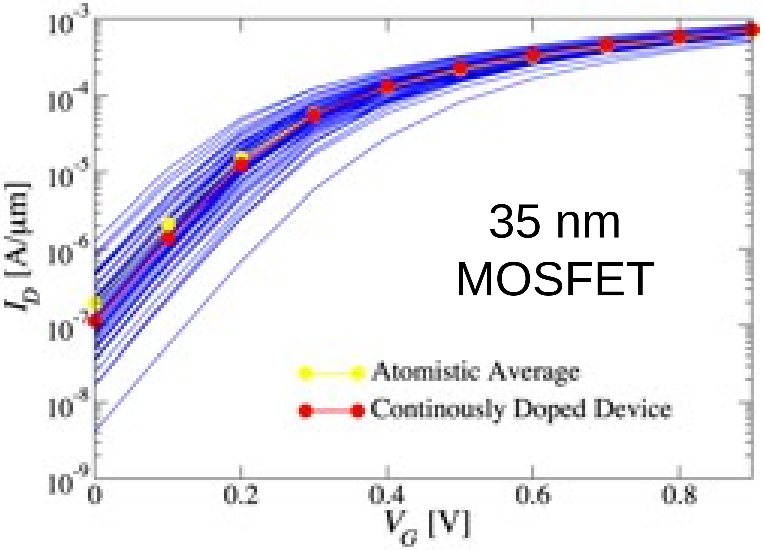
3) asymmetry in I_D

3D transport leads to inhomogeneous conduction

(see Wong and Taur, IEDM, 1993, p. 705)

discrete doping effects (iii)



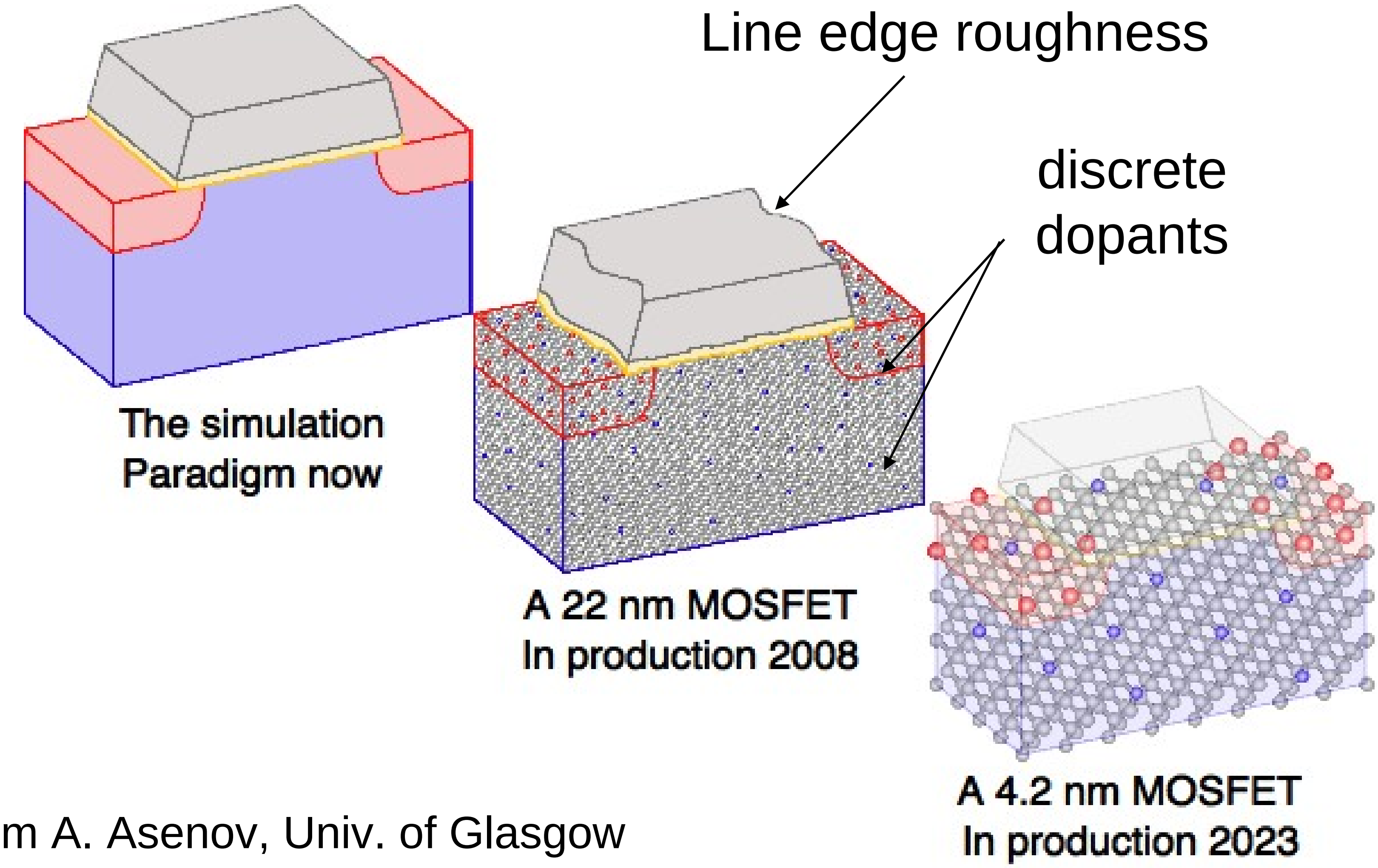


35 nm
MOSFET

AFM measurements, Fujitsu

(simulations from A. Asenov group, Univ. of Glasgow)

statistical variability

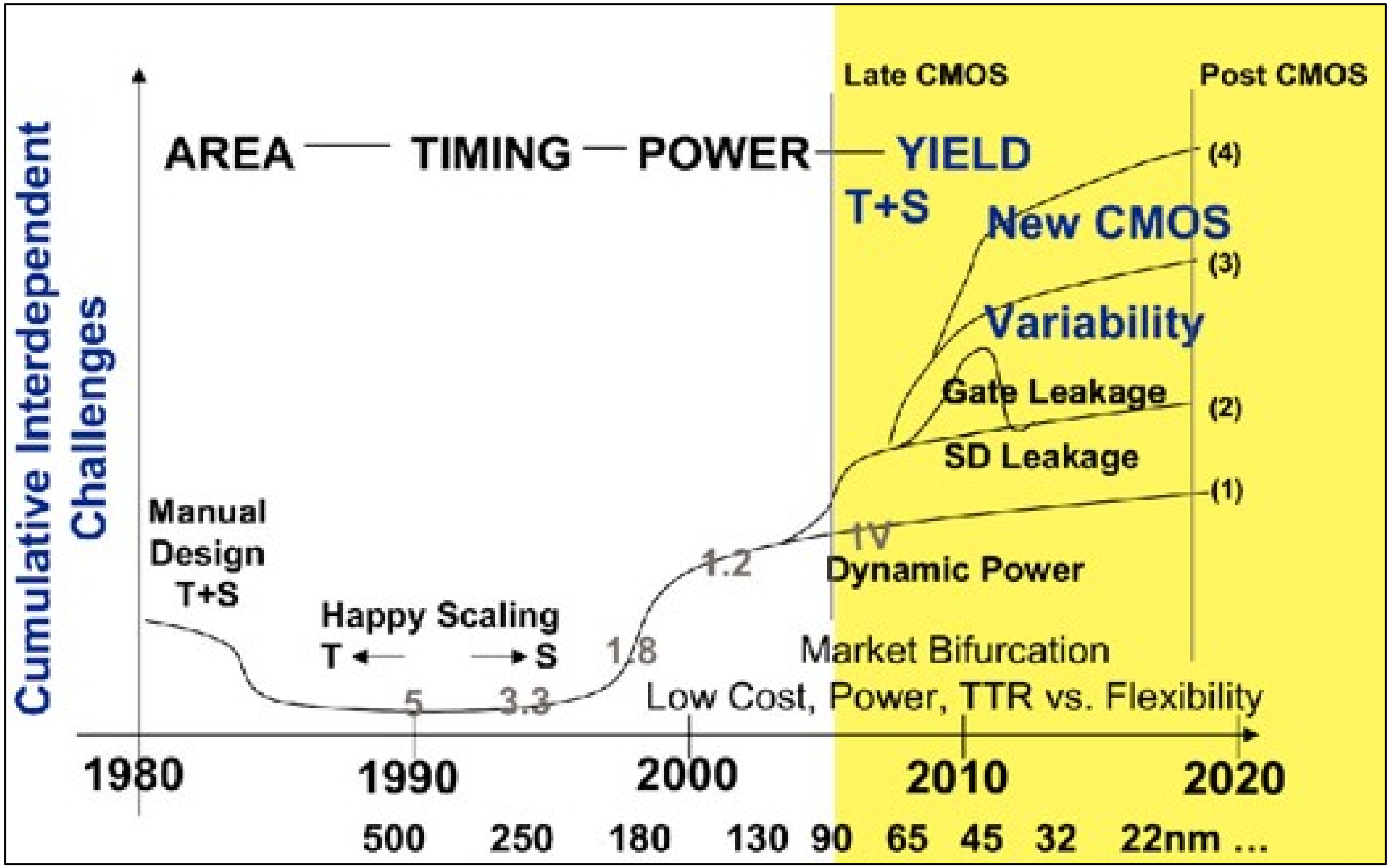


Line edge roughness

discrete dopants

From A. Asenov, Univ. of Glasgow

variability is becoming a major issue



G. Declerck, Keynote talk, VLSI Technol. Symp. 2005

outline

1) Unit Process Operations
2) Process Variations

For a basic, CMOS process flow for an STI (shallow trench isolation process), see: http://www.rit.edu/~lffeee/AdvCmos2003.pdf

CMOS process flow

For a basic, CMOS process flow for an STI

(shallow trench isolation process), see:

http://www.rit.edu/~lffeee/AdvCmos2003.pdf

The author is indebted to Dr. Lynn Fuller of Rochester Institute of Technology for making these materials available. What follows is a condensed version of a more complete presentation by Dr. Fuller. I regret any errors that I may have introduced by shortening these materials. -Mark Lundstrom 10/19/06