Dragica Vasileska

nanoHUB Used in Research:

A One Developer/User View

Talk Outline

- Introduction: PUNCH and nanoHUB
- Moore's Law for Transistor Scaling: SCHRED Tool
- Diving Deeper into Quantum Mechanics: QUAMC2D
- Nanoelectronics: The Need for NEMO5
- What nanoHUB Tools Can/Can't Do
- Conclusions

nanoHUB Predecessor: PUNCH

PUNCH: Purdue University Network Computing Hub

Developed at:	Purdue University
Deployed:	1995
Retired:	April, 2007
Usage:	4600 users, 395,000 simulations

Prof. Vasileska became affiliated to PUNCH as part of a NSF sponsored **DESCARTES** project in 1998:

- SCHRED MOS Capacitor Tool: installed on PUNCH 1998 (Dragica Vasileska)
- SCHRED Dual-Gate Capacitor Tool: installed on PUNCH 1999 (Dragica Vasileska and Zhibin Ren)

NCN nanoHUB Launched 2002

Dragica Vasileska Contributions

Item	Value
Contributions:	372
Total Simulation Users Served:	22,144
Rank by Contributions:	3 / 1588
First Contribution:	09 Mar 2005
Last Contribution:	17 Feb 2015
Citations on Contributions:	136
Usage in Courses/Classrooms:	7,516 users served in 480 courses from 47 institutions

Tools Co-Authored by Vasileska: 19

HgCdTe Photodetector Lab

Cu in CdTe Lab

1D Drift Diffusion Model for Crystalline Solar Cells

Optoelectronics: Education

ACUTE

AQME - Advancing Quantum Mechanics for Engineers

ABACUS -

Education

MESFET Lab

BJT Lab

MOSCap

MOSFet

PN Junction Lab

TCAD – Tools Education

Bulk Monte Carlo Lab

QuaMC2D

Research Tools/Education Particle-Based Device Simulators

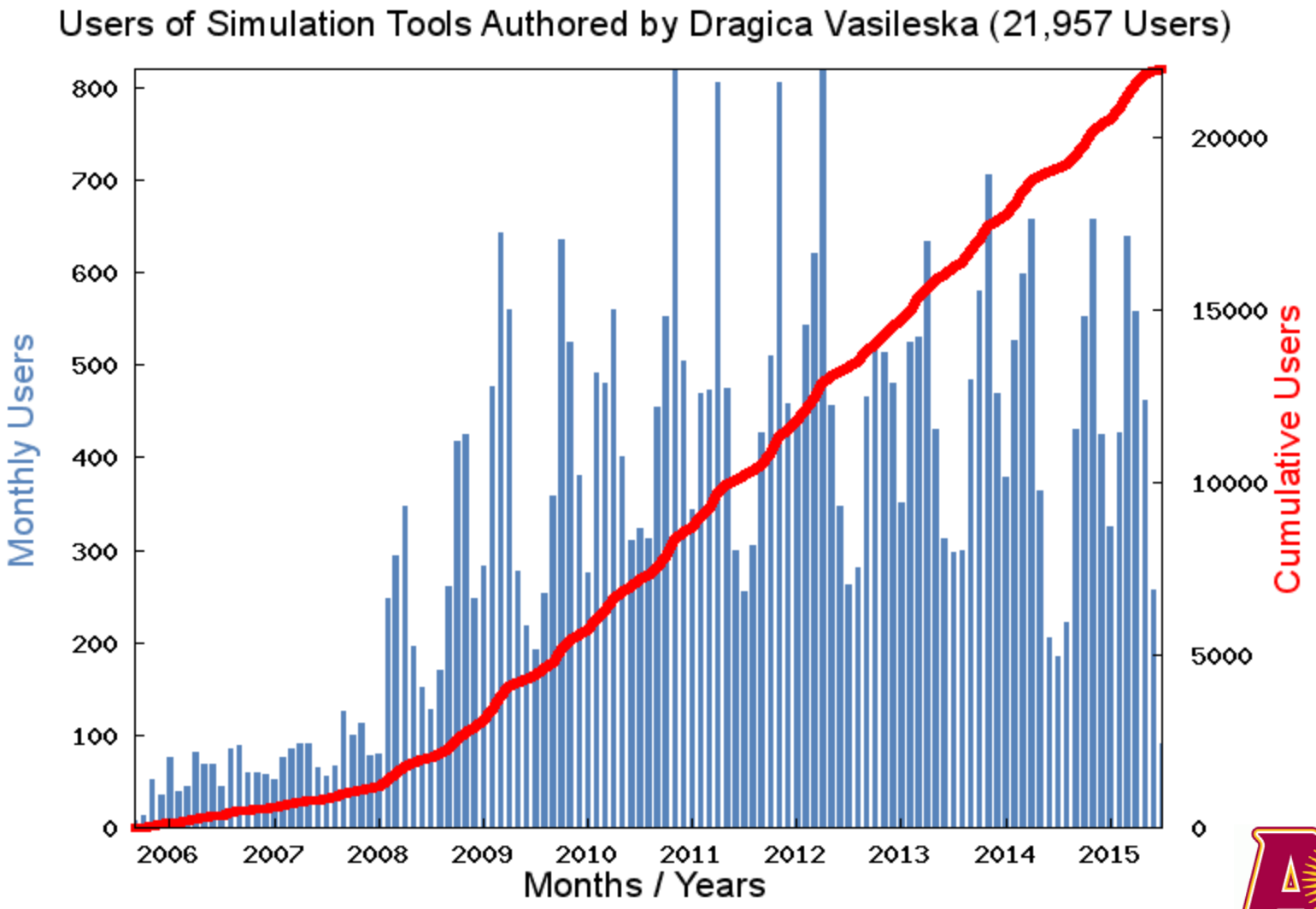
Bound States Calculation Lab

Piece-Wise Constant Potential Barriers Tool

Schred

Education/Research

Impact Graph



Tool-Based Curricula

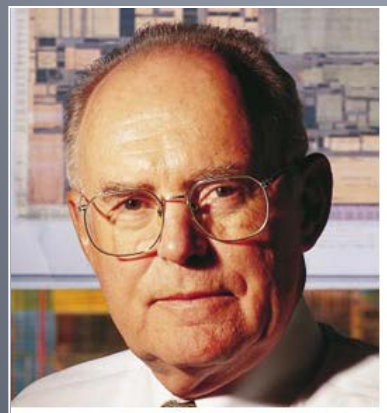
New paradigms of learning are necessary for training students in the vibrant and constantly changing field of **nanoelectronics**.

Prof. Vasileska and Prof. Klimeck propose a novel methodology: **Tool-Based Curricula.**

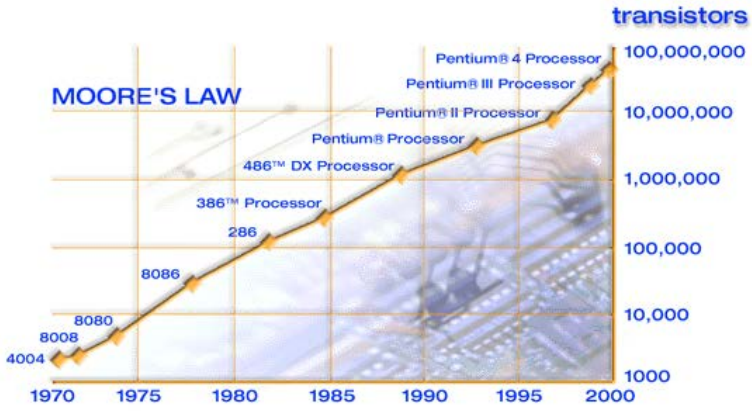
Tool-Based Curricula consists of assembling a set of computational simulation tools with:

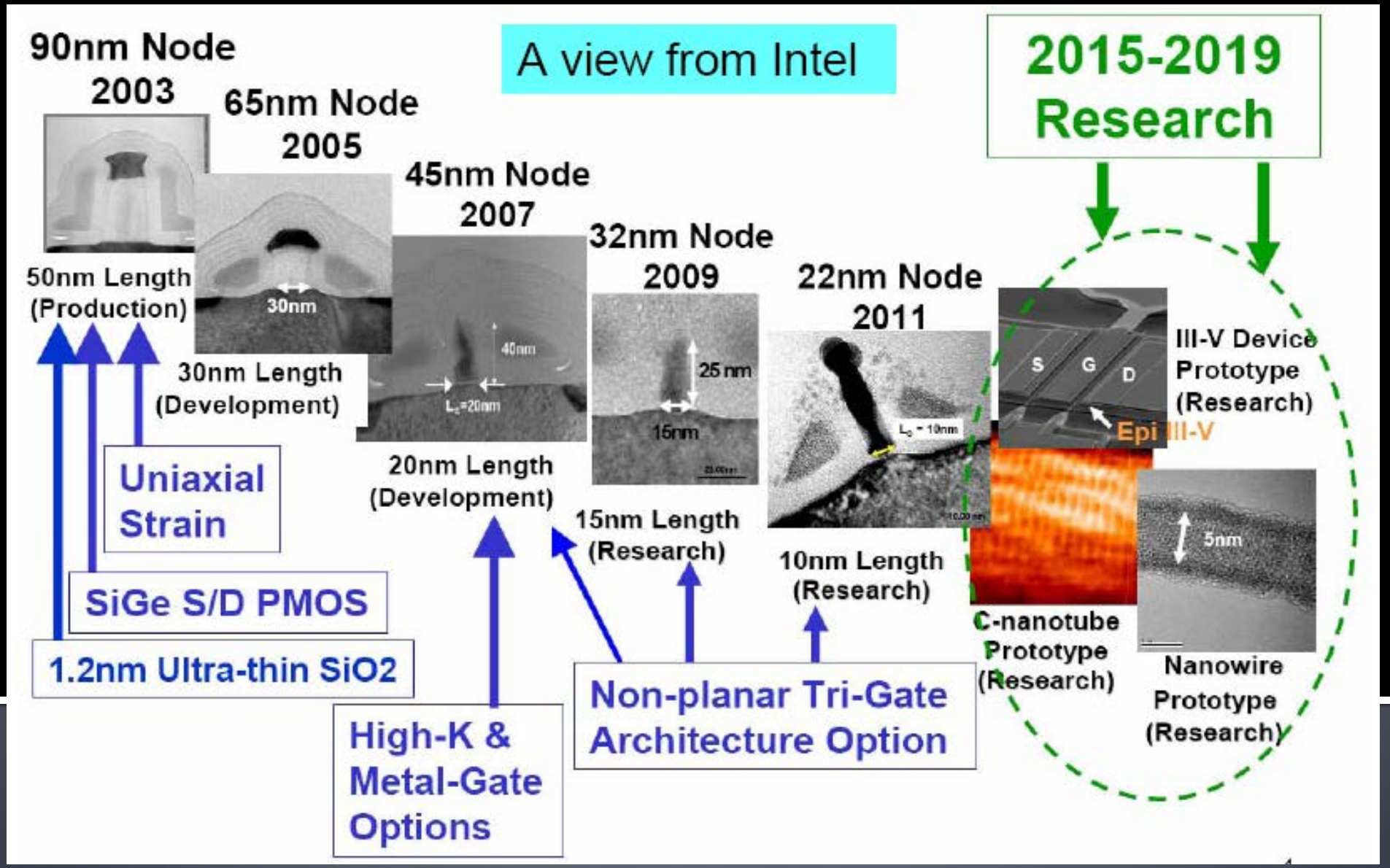
- demos on how to use the tools,
- the objectives of the tool and what can be learned with them,
- assembly of solved problems,
- homework assignments,
- challenge problems which are related to real world applications.

Moore's Law for Transistor Scaling: NEED for SCHRED Tool



Gordon Moore
"*every 1.5 years complexity doubles*"




A view from Intel
90nm Node
2003
65nm Node
2005
45nm Node
2007
32nm Node
2009
22nm Node
2011
2015-2019
Research
50nm Length
(Production)
30nm
30nm Length
(Development)
40nm
L_g=20nm
20nm Length
(Development)
25 nm
15nm
15nm Length
(Research)
L_g = 10nm
10nm Length
(Research)
S
G
D
III-V Device
Prototype
(Research)
Epi III-V
5nm
C-nanotube
Prototype
(Research)
Nanowire
Prototype
(Research)
Uniaxial
Strain
SiGe S/D PMOS
1.2nm Ultra-thin SiO2
High-K &
Metal-Gate
Options
Non-planar Tri-Gate
Architecture Option

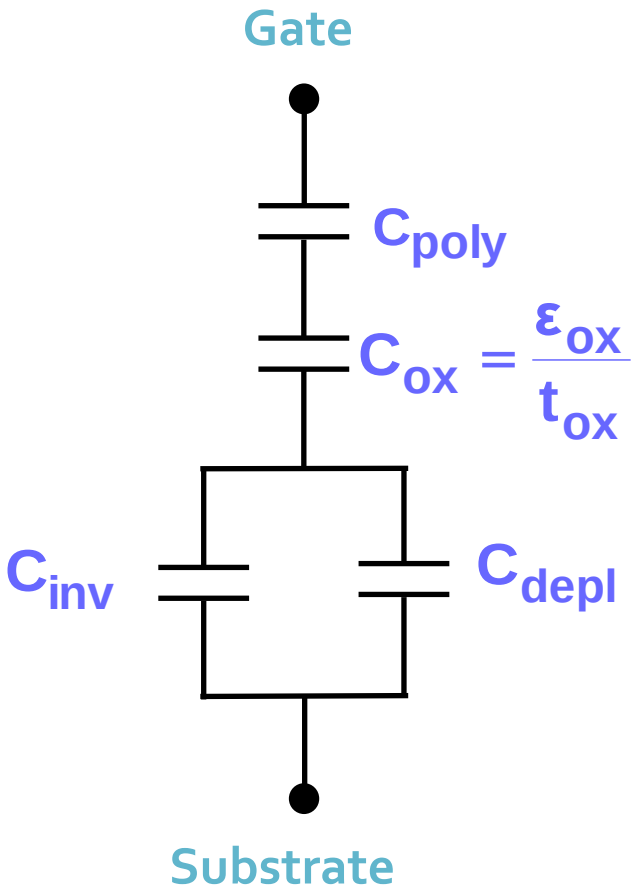
Quantum Mechanical Size Quantization

Historical Perspective

- Bacarani and Worderman ⇒ transconductance degradation (Proceedings of the IEDM, pp. 278-281, 1982)
- Hartstein and Albert ⇒ estimate of the inversion layer thickness (Phys. Rev. B, Vol. 38, pp.1235-1240, 1988)
- van Dort et al. ⇒ analytical model for Vth which accounts for QM effects (IEEE TED, Vol. 39, pp. 932-938, 1992)
- Takagi and Toriumi ⇒ physical origins of Cinv (IEEE TED, Vol. 42, pp. 2125-2130, 1995)
- Hareland et al. ⇒ modeling of the QM effects in the channel (IEEE TED, Vol. 43, pp. 90-96, 1996)
- Krisch et al. ⇒ poly-gate capacitance attenuation (IEEE EDL, Vol. 17, pp. 521-524, 1996)
- Vasileska, Schroder and Ferry ⇒ influence of many-body effects on Cinv (IEEE TED, Vol. 44, pp. 584-587, 1997)

Quantum-Mechanical Size Quantization

Physical Origin

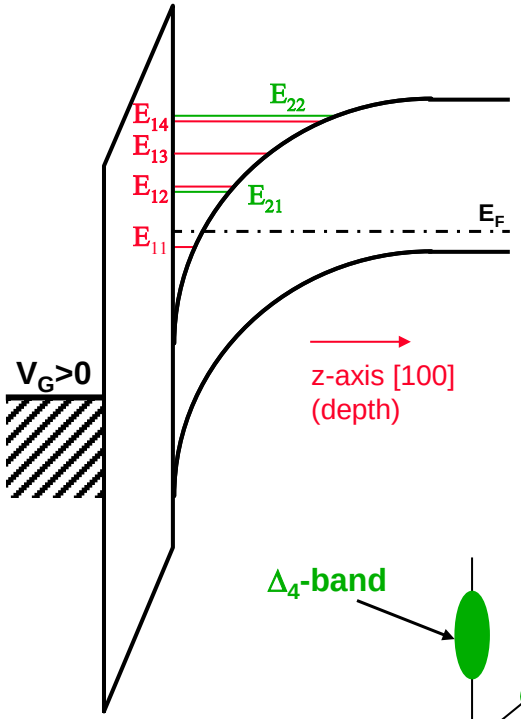


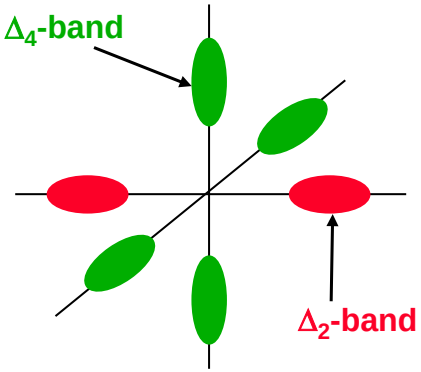
$$C_{tot} = \frac{C_{ox}}{1 + \frac{C_{ox}}{C_{poly}} + \frac{C_{ox}}{C_{inv} + C_{depl}}} \approx \frac{C_{ox}}{1 + \frac{C_{ox}}{C_{poly}} + \frac{C_{ox}}{C_{inv}}}$$

D. Vasileska, and D.K. Ferry, "The influence of poly-silicon gates on the threshold voltage, inversion layer and total gate capacitance in scaled Si-MOSFETs," *Nanotechnology* Vol. 10, pp.192-197 (1999).

Quantum-Mechanical Size Quantization

Numerical Modeling





- **1D Poisson equation:**

$$\frac{\partial}{\partial z}\left[\frac{1}{\varepsilon(z)}\frac{\partial \varphi}{\partial z}\right] = -e\left[N_D^+(z) - N_A^-(z) + p(z) - n(z)\right]$$

- **1D Schrödinger equation:**

$$\left[-\frac{\hbar^2}{2}\frac{\partial}{\partial z}\left(\frac{1}{m_\perp^i(z)}\frac{\partial}{\partial z}\right) + V(z)\right]\psi_{ij}(z) = E_{ij}\psi_{ij}(z)$$

- **Electron density:**

$$n(z) = \sum_{i,j} N_{ij}\psi_{ij}^2(z)$$

$$N_{ij} = \frac{m_{\|}^i k_B T}{\pi\hbar^2}\ln\left[1 + \exp\left(\frac{E_F - E_{ij}}{k_B T}\right)\right]$$

Δ_2-band :
$m_\perp = m_l = 0.916m_0$, $m_{||} = m_t = 0.196m_0$

Δ_4-band:
$m_\perp = m_t = 0.196m_0$, $m_{||} = (m_l\, m_t)^{1/2}$

Exchange-Correlation

$$E = E^{HF} + E_{corr} = E^{HF}_{kin} + E^{HF}_{exchange} + E_{corr}$$

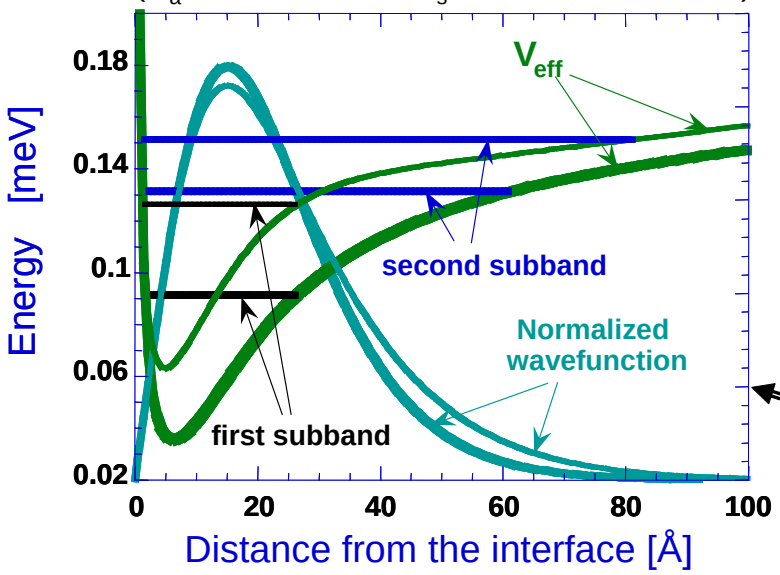
Total Ground State Energy of the System

Hartree-Fock Approximation for the Ground State Energy

Accounts for the error made with the Hartree-Fock Approximation

Accounts for the reduction of the Ground State Enery due to the inclusion of the Pauli Exclusion Principle

Vasileska *et al*., J. Vac. Sci. Technol. B **13**, 1841 (1995)
(N_a=2.8x10^{15} cm^{-3}, N_s=4x10^{12} cm^{-2}, T=0 K)

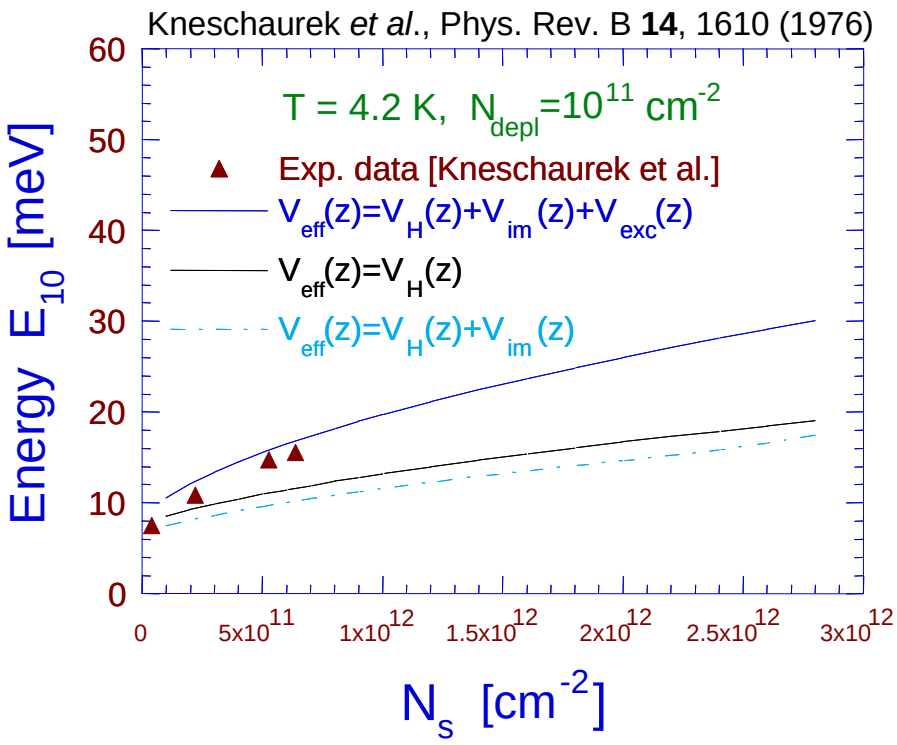


Exchange-Correlation Correction:

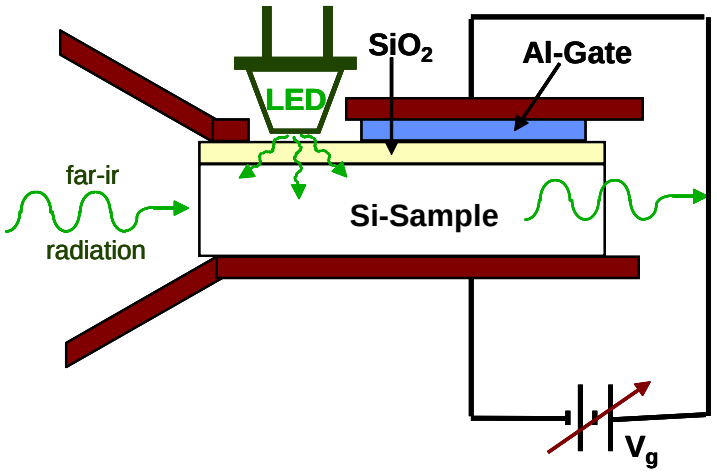
- Lower subband energies
- Increase in the subband separation
- Increase in the carrier concentration at which the Fermi level crosses into the second subband
- Contracted wavefunctions

Thick (thin) lines correspond to the case when the exchange-correlation corrections are included (omitted) in the simulations.

Comparison With Experiments



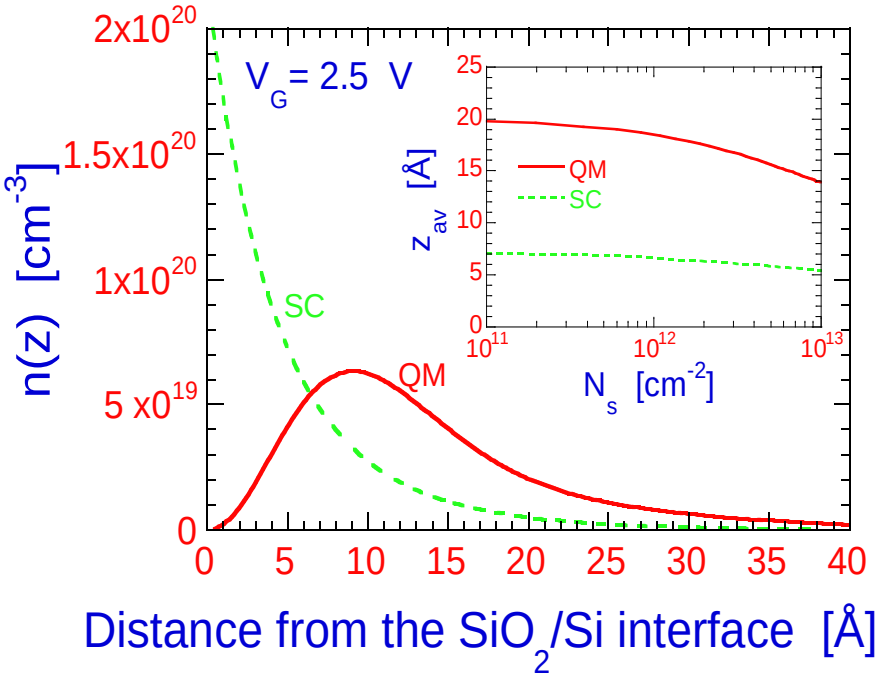
Infrared Optical Absorption Experiment:

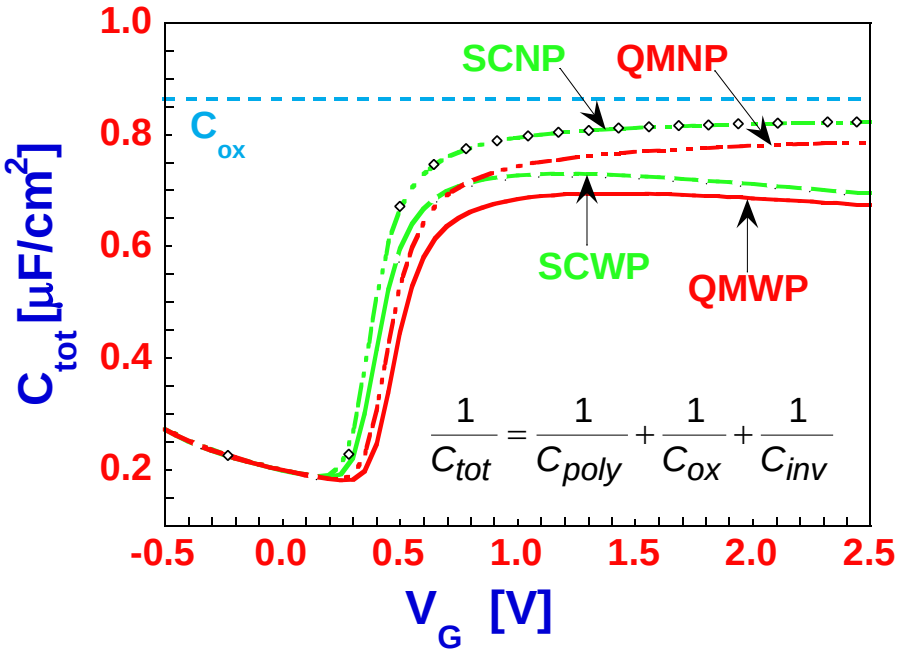


Transmission-Line Arrangement

Tool Validation!

Simulation Results Obtained With SCHRED

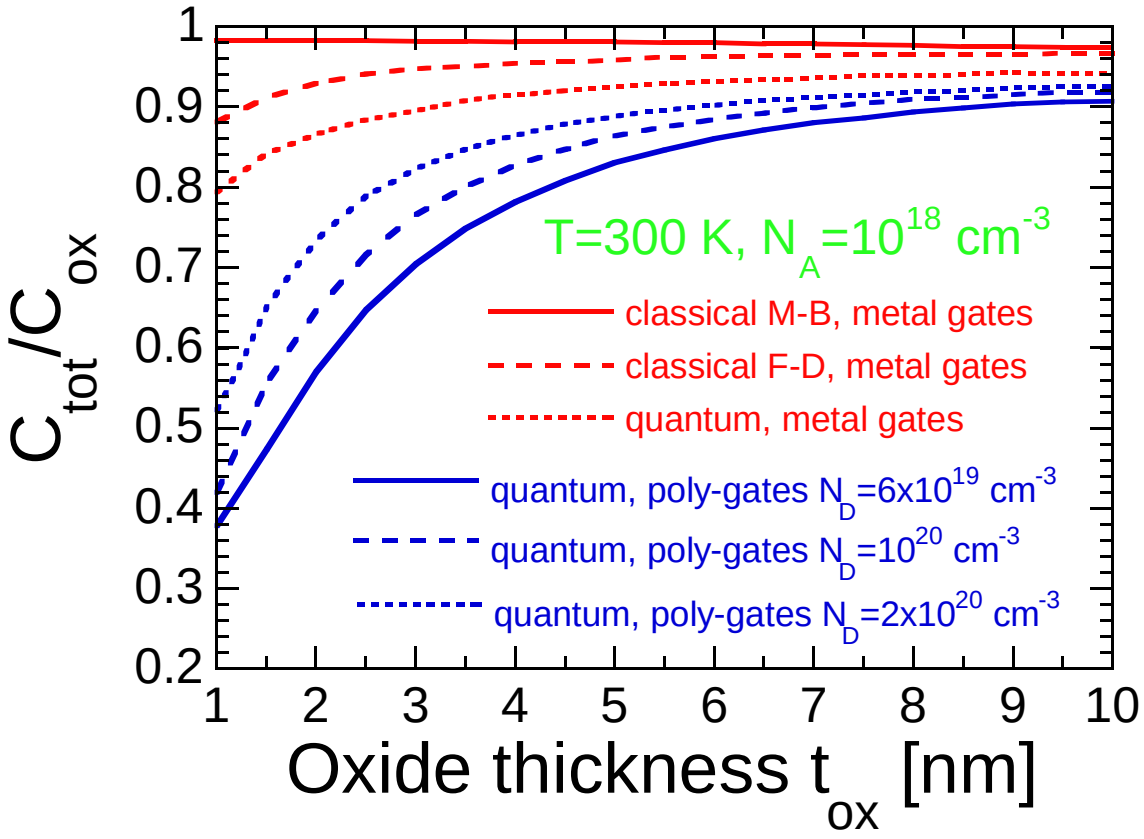




- The classical charge density peaks right at the SC/oxide interface.
- The quantum-mechanically calculated charge density peaks at a finite distance from the SC/oxide interface, which leads to larger average displacement of electrons from that interface.

- C_{inv} reduces C_{tot} by about 10%
- C_{poly}+ C_{inv} reduce C_{tot} by about 20%
- With poly-depletion C_{tot} has pronounced gate-voltage dependence

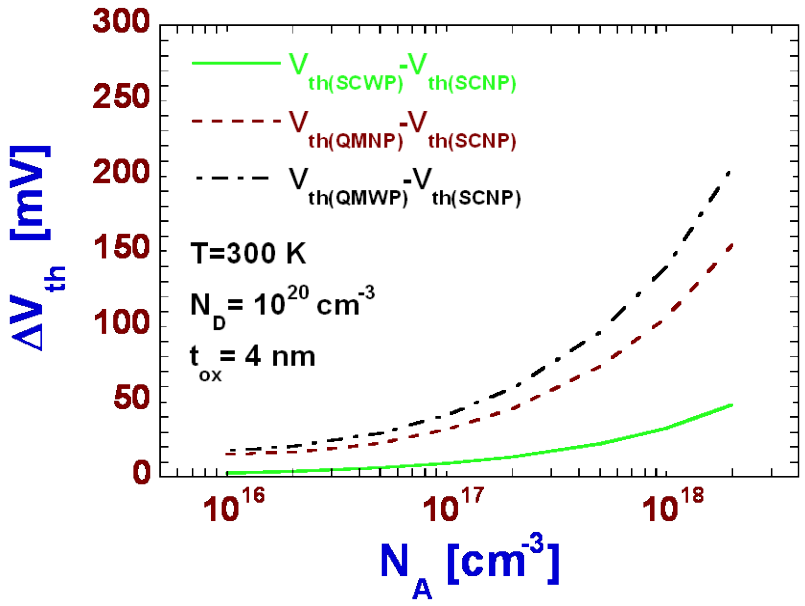
Simulation Results Obtained With SCHRED

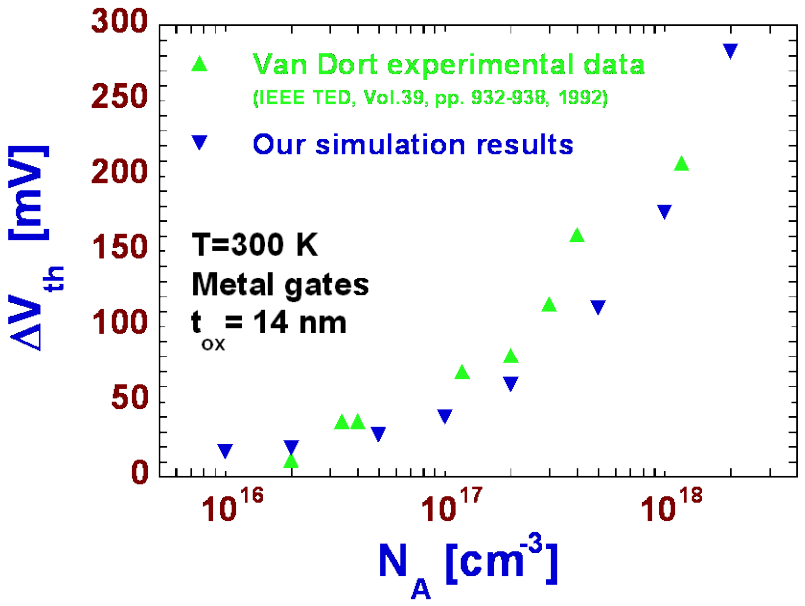


Degradation of the Total Gate Capacitance C_{tot} for Different Device Technologies

Simulation Results Obtained With SCHRED

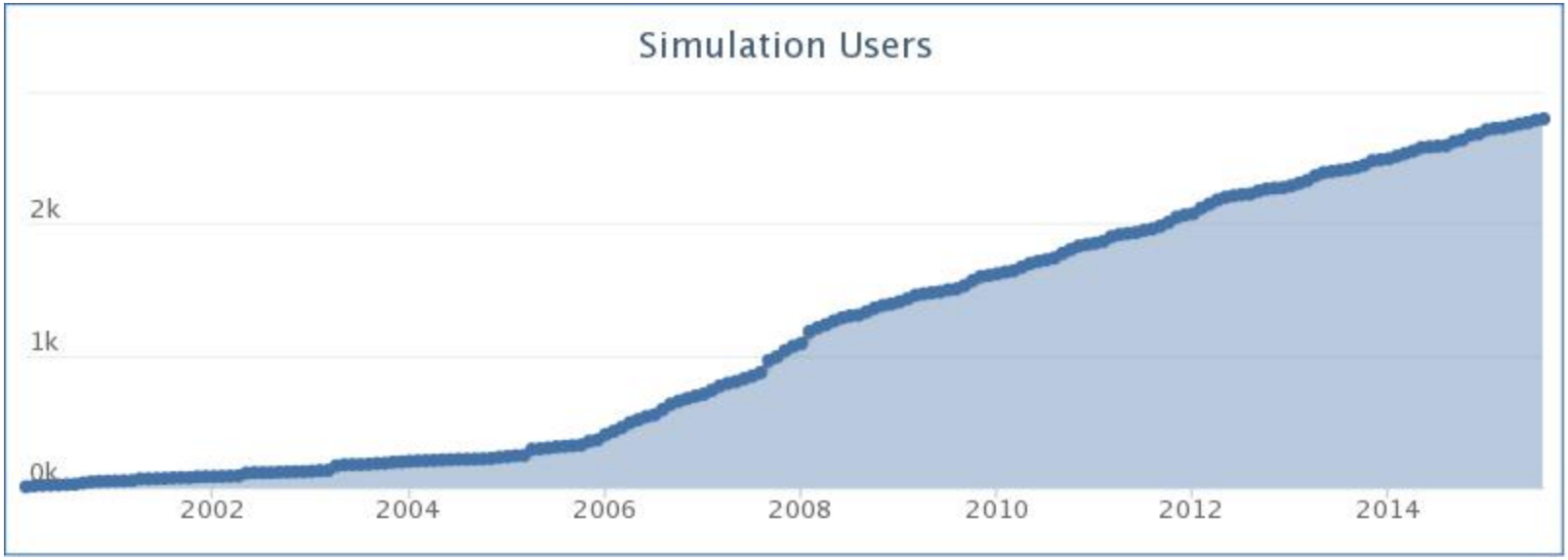
MOS Capacitor with both Metal and Poly-Silicon Gates





- ΔV_{th} shows strong substrate doping dependence when poly-gate depletion and QM effects in the channel are included
- There is close agreement between the experimentally derived threshold voltage shift and our simulation results

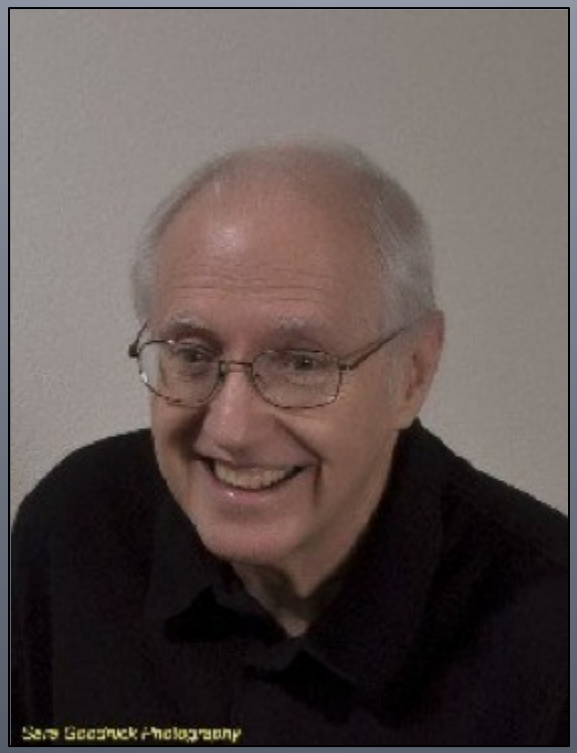
SCHRED Users Since Its Posting – 120 Citations



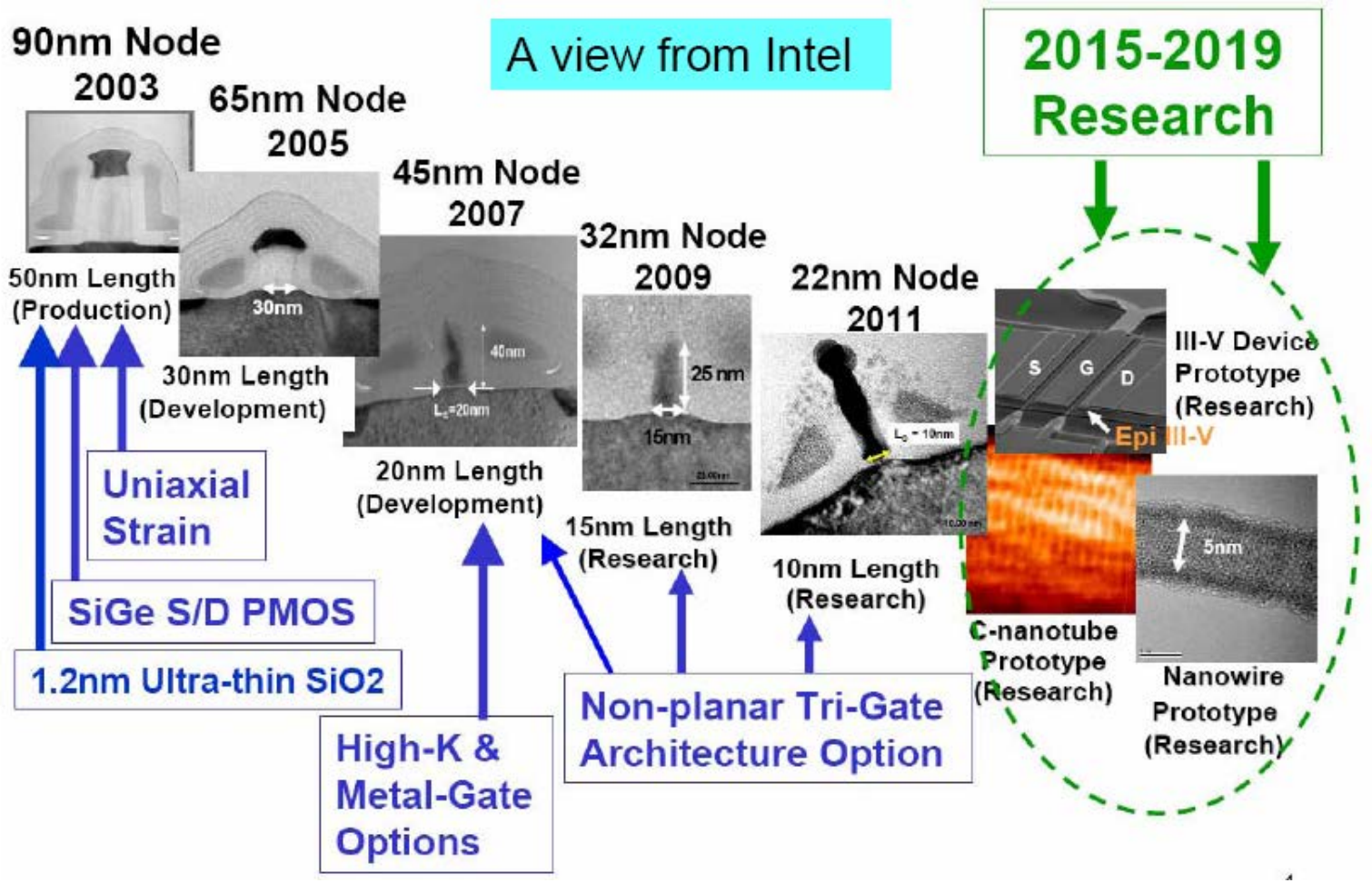
It is evident that many years of research by a great many people, both before and after the discovery of the transistor effect, has been required to bring our knowledge of semiconductors to its present development. We were fortunate to be involved at a particularly opportune time and to add another small step in the control of Nature for the benefit of mankind.

- John Bardeen, 1956 Nobel lecture

Diving Deeper into Quantum Mechanics: QUAMC2D



More Moore …


90nm Node
2003
65nm Node
2005
45nm Node
2007
32nm Node
2009
22nm Node
2011
A view from Intel
2015-2019
Research
50nm Length
(Production)
30nm Length
(Development)
20nm Length
(Development)
15nm Length
(Research)
10nm Length
(Research)
30nm
40nm
25nm
15nm
S
G
D
Epi III-V
5nm
III-V Device
Prototype
(Research)
C-nanotube
Prototype
(Research)
Nanowire
Prototype
(Research)
Uniaxial
Strain
SiGe S/D PMOS
1.2nm Ultra-thin SiO2
High-K &
Metal-Gate
Options
Non-planar Tri-Gate
Architecture Option

Welcome to the SOI World!

Highlights

- Reduced junction capacitance.
- Absence of latchup.
- Ease in scaling (buried oxide need not be scaled).
- Compatible with conventional Silicon processing.
- Sometimes requires fewer steps to fabricate.
- Reduced leakage.
- Improvement in the soft error rate.

Drawbacks

- Drain Current Overshoot.
- Kink effect
- Thickness control (fully depleted operation).
- Surface states.

Incorporation of Quantum-Mechanical Size-Quantization Effects Mandatory

- Quantum correction methods
  - Drift-diffusion + hydrodynamic models
    - Analytical corrections
      - Hansch method
      - Van Dort method
    - Numerical approaches
      - Density gradient method
  - Particle-based device simulators
    - Effective Potential Approach in Conjunction With Particle-Based Approaches
- Solution of the Schrodinger-Transport-Poisson Problem

Effective Potential Approach

In principle, the effective role of the potential can be rewritten in terms of the non-local density as (Ferry *et al*.[1]):

$$\bar{V} = \int dr V(\mathrm{r}) \sum_i n_i(\mathrm{r})$$

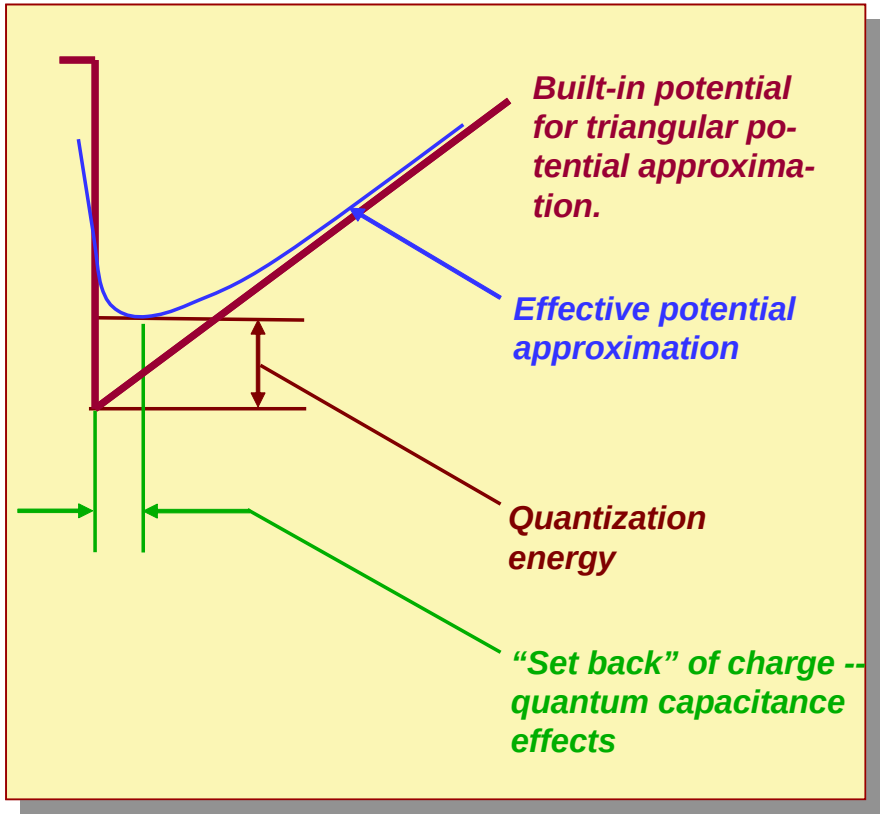
$$\sim \int dr V(\mathrm{r}) \sum_i \int d\mathrm{r}' \exp\left(-\frac{|\mathrm{r}-\mathrm{r}'|^2}{\alpha^2}\right) \delta(\mathrm{r}'-\mathrm{r}_i)$$

$$\sim \sum_i \int d\mathrm{r}\, \delta(\mathrm{r}-\mathrm{r}_i) \int d\mathrm{r}' V(\mathrm{r}') \exp\left(-\frac{|\mathrm{r}-\mathrm{r}'|^2}{\alpha^2}\right)$$

$$\sim \sum_i \int d\mathrm{r}\, \delta(\mathrm{r}-\mathrm{r}_i) V_{eff}(\mathrm{r})$$

Classical density

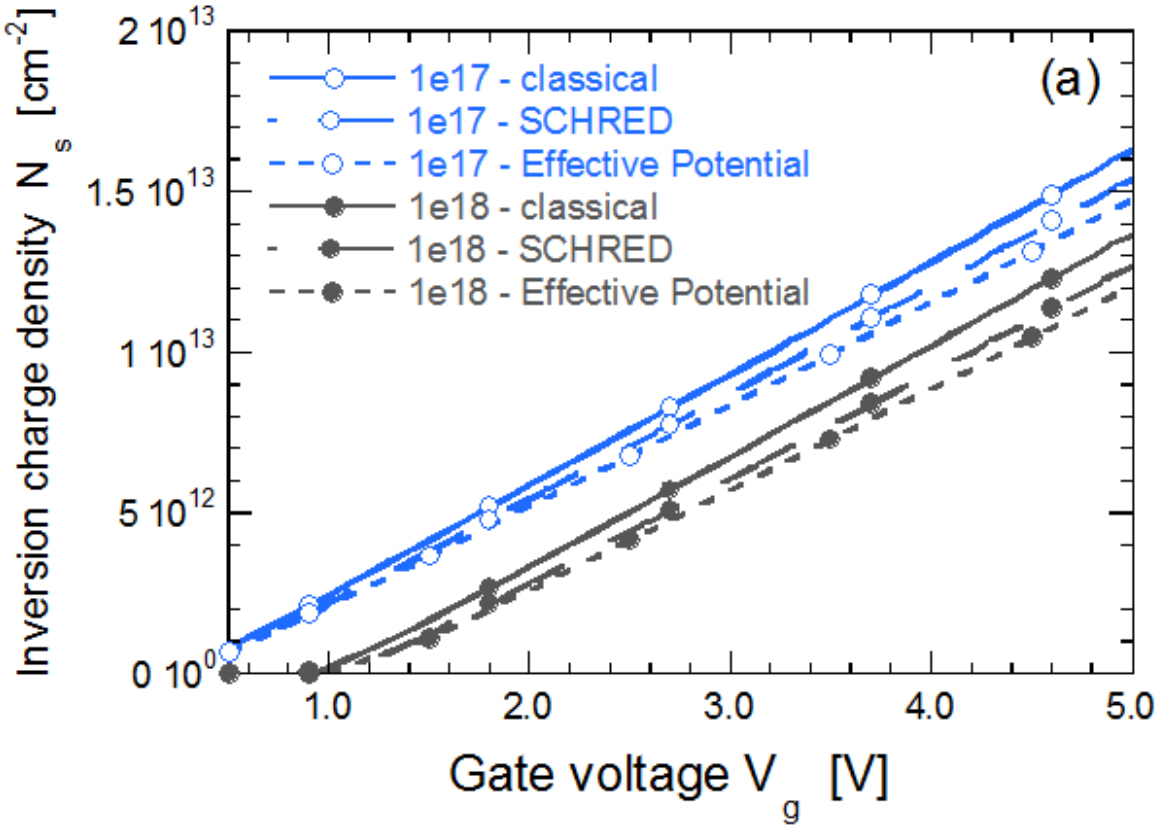
Smoothed, effective potential



[1] D. K. Ferry, *Superlatt. Microstruc.* **27**, 59 (2000);

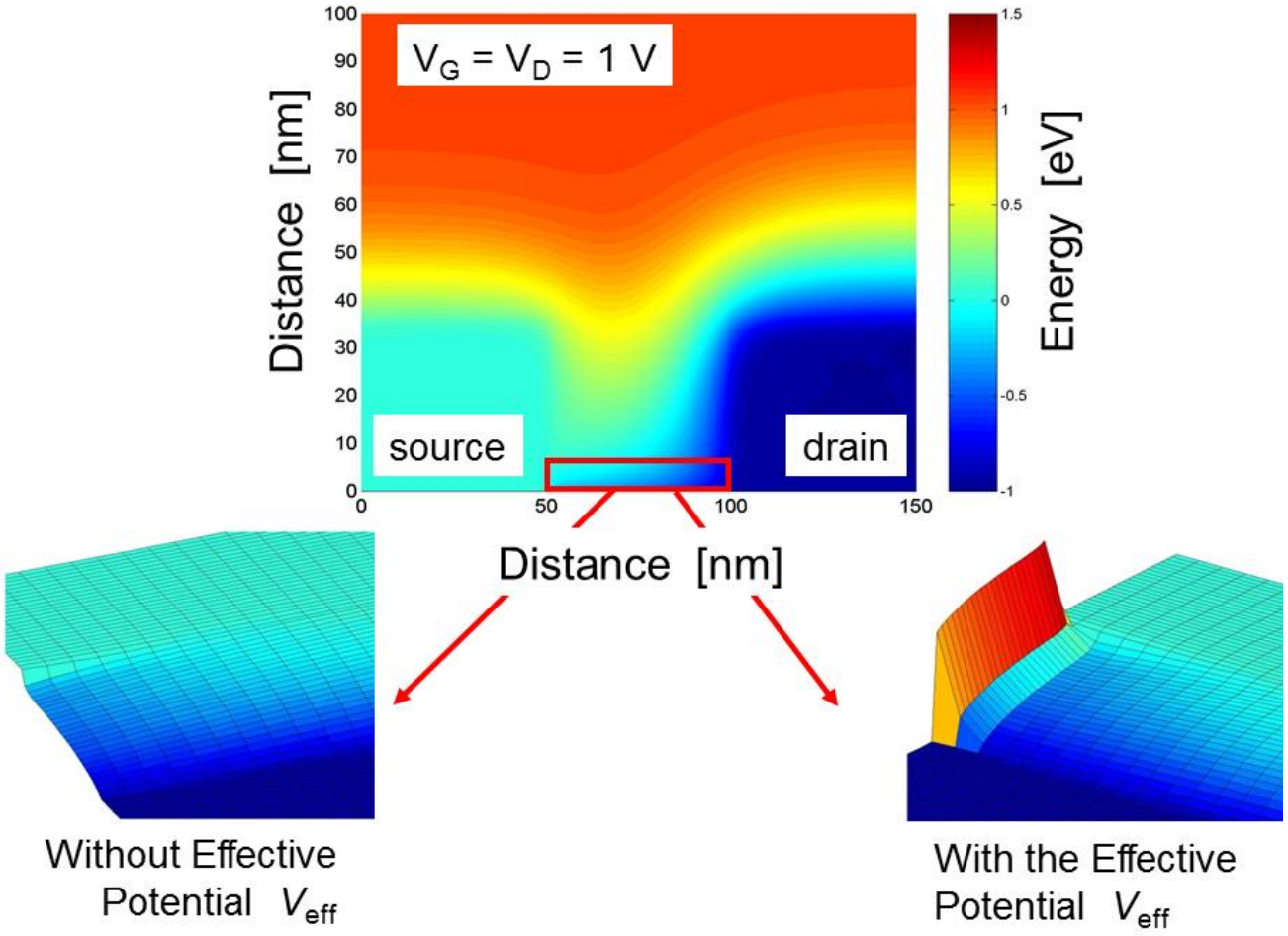
Comparison to 1D-SP

Method Validation!



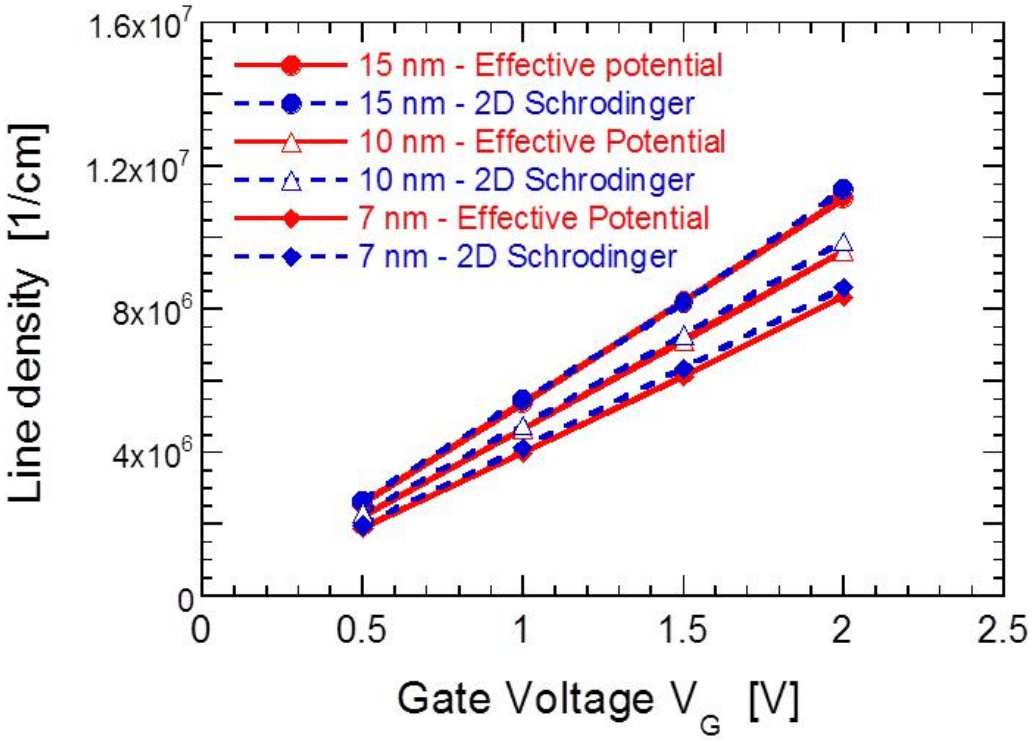
The Gaussian fitting parameter a_0 = 0.5 nm.

Simulation of a Conventional MOSFET



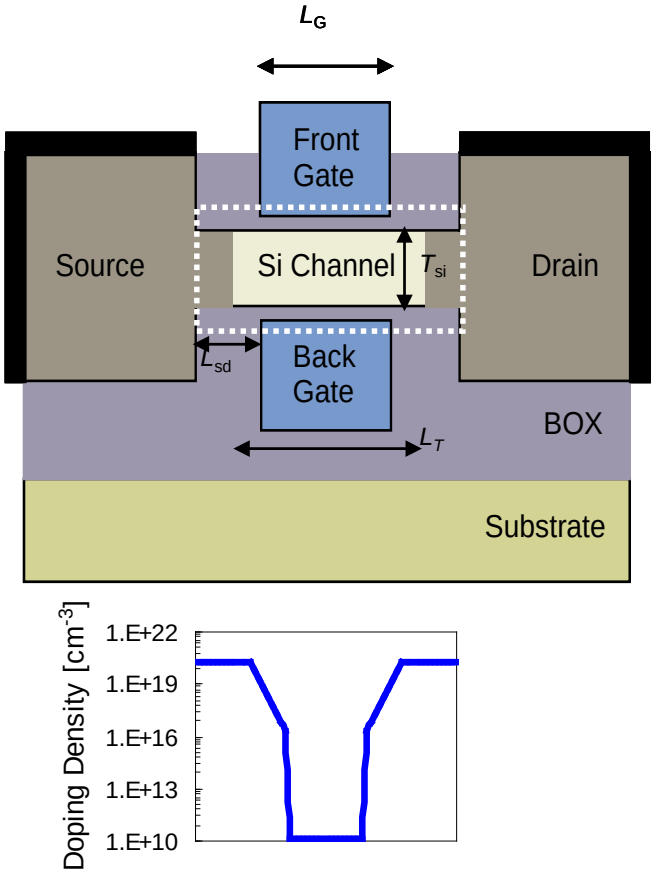
Comparison to 2D-SP

Method Validation!



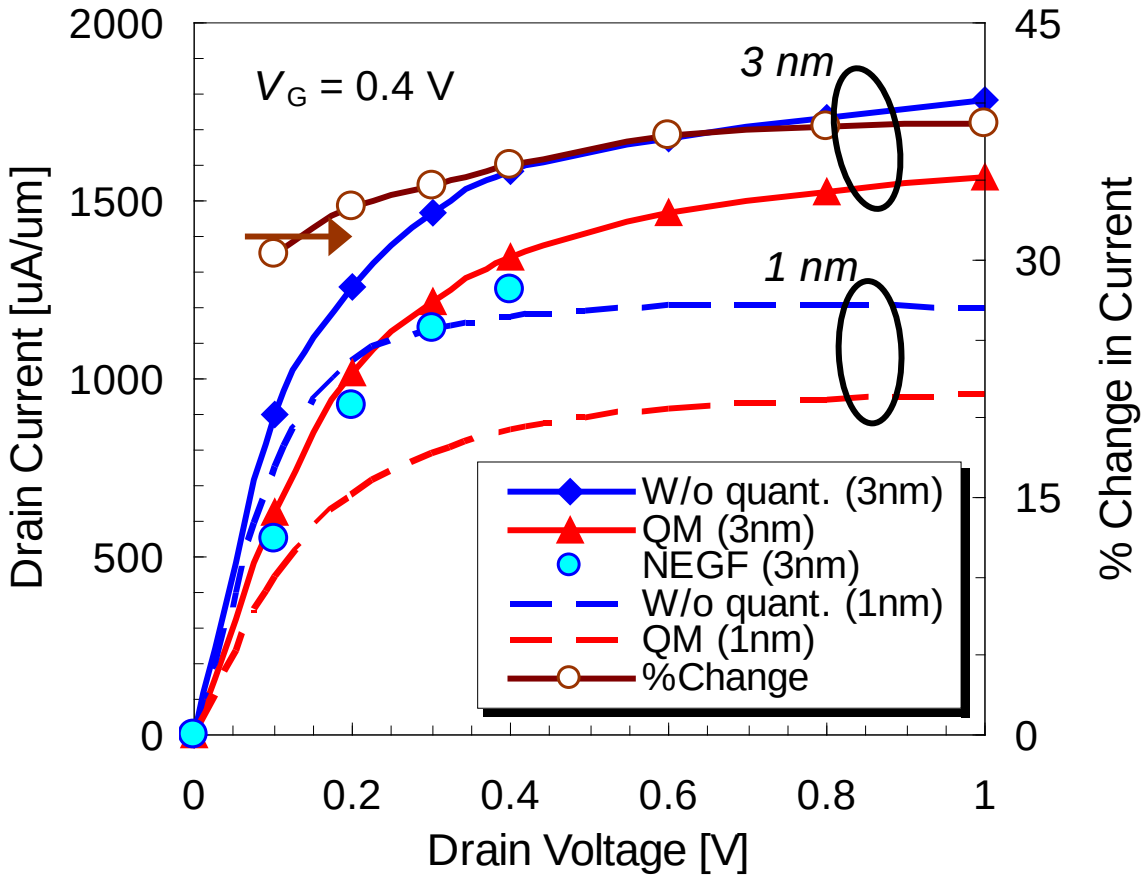
Excellent agreement is observed between the two approaches when using the theoretical value for the Gaussian smoothing parameter of 0.64 nm.

Application of the Effective Potential Approach and QUAMC3D



T_{ox} = 1 nm
L_G = 9 nm
L_{sd} = 10 nm
N_b = 0
Φ_G = 4.188

T_{si} = 3 nm
L_T = 17 nm
N_{sd} = 2 x 10^{20} cm^{-3}
g = 1 nm/decade
V_G = 0.4 V



Output characteristics of DG Structure

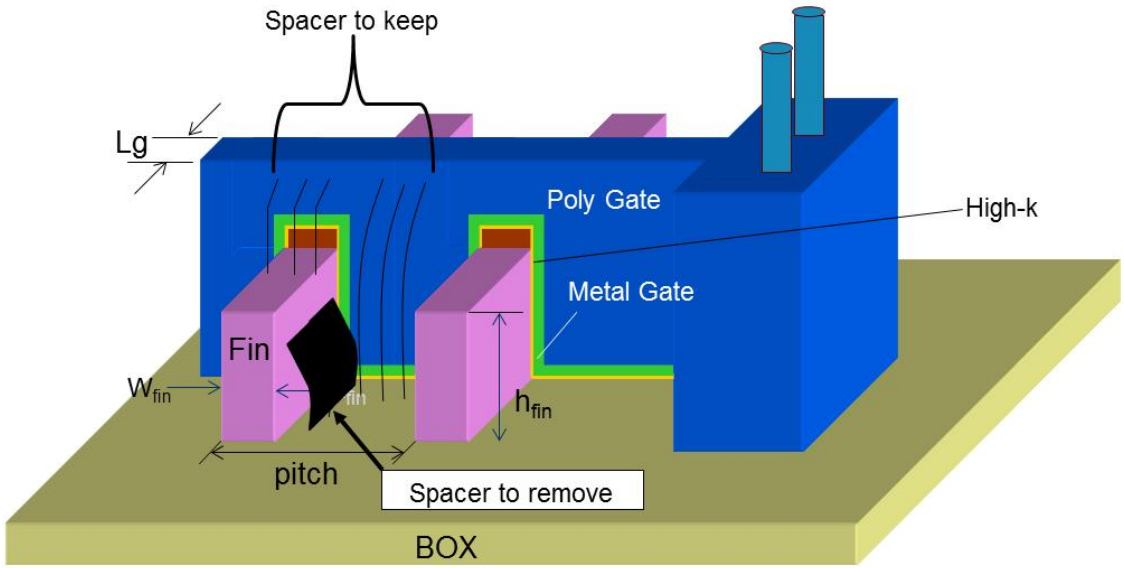
Drawbacks of the Effective Potential Approach

- Does not calculate the subband structure
- Does not calculate the 1D/2D density of states in nanowires/inversion layers

➔ Scattering is not treated accurately

Nanoelectronics: The Need for NEMO5

Towards Nanotransistors: More Moore … & More Than Moore



Intel's next technology node is a 14 nm FinFET.

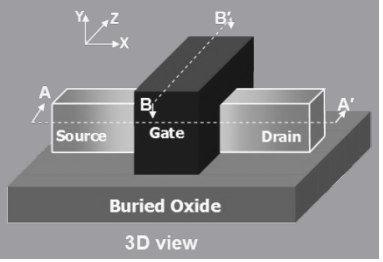
Ballistic Modeling of FinFET Device with Contact Block Reduction (CBR) Method

D. Mamaluy, H. R. Khan, D. Vasileska

- Exactness - Accomplished with comparison with experiments
- Speed (Optimization and Process Variation)

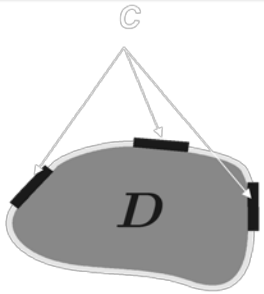
Experimental FinFET*
Gate length L_g = 10 nm
Fin width t_{Si} = 12 nm,
Gate oxide thickness t_{ox}= 1.7 nm
(110) channel orientation

*Bin Yu *et. al.*, "FinFET Scaling to 10 nm Gate Length", *IEDM Tech. Digest*, 2002

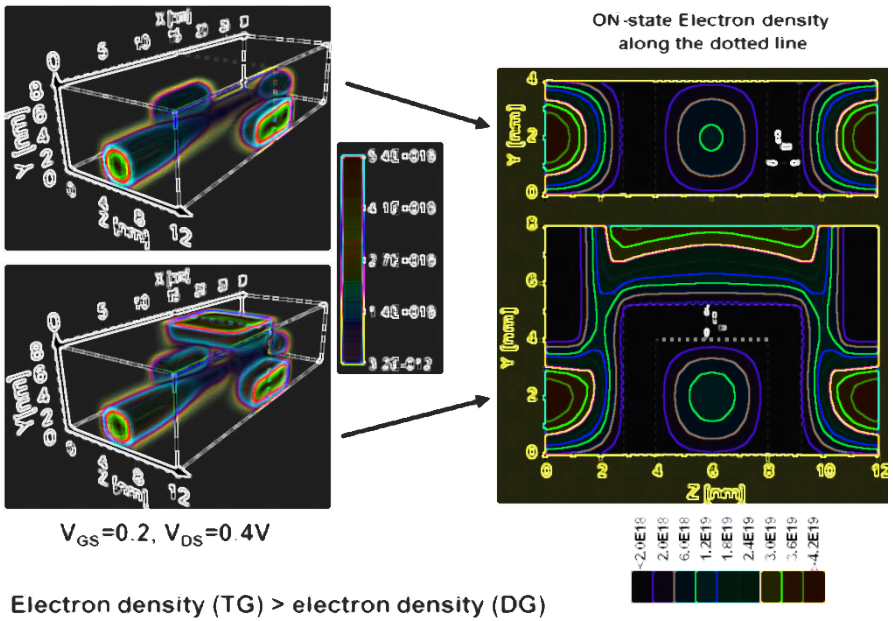


3D view

Properties of a GOOD Device simulator



DG vs. Tri-Gate



V_{GS}=0.2, V_{DS}=0.4V

Electron density (TG) > electron density (DG)

H. R. Khan, D. Mamaluy and D. Vasileska, "Quantum transport simulation of experimentally fabricated nano-FinFET", *IEEE Trans. Electron Devices*, Vol. 54 (4), pp. 784-796 (2007).

H. R. Khan, D. Mamaluy and D. Vasileska, "Approaching Optimal Characteristics of 10 nm High Performance Devices" a Quantum Transport Simulation Study of Si FinFET, *IEEE Trans. Electron Devices*, Vol. 55(1), pp. 743-753 (2008).

Ballistic Modeling of FinFET Device with CBR Method

D. Mamaluy, H. R. Khan, D. Vasileska

- Exactness - Accompli with experiments
- Speed (Optimization

Experimental FinFET*
Gate length L_g = 10 nm
Fin width t_{Si} = 12 nm,
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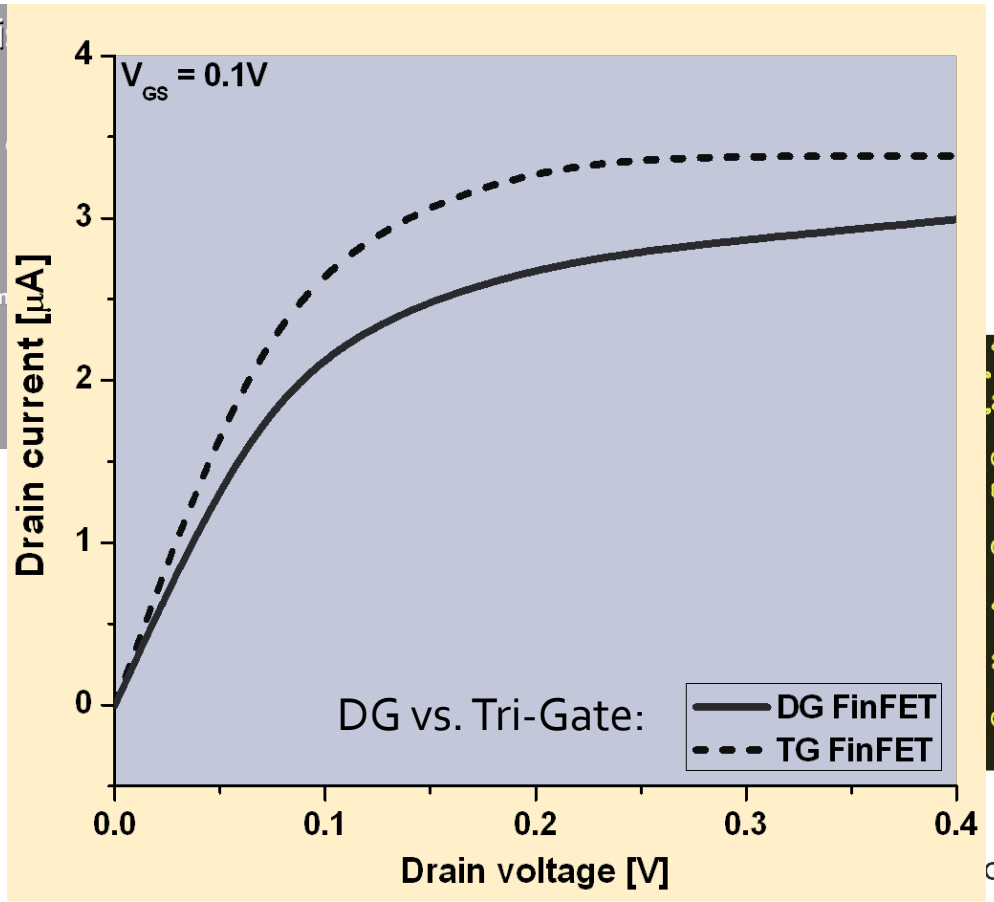
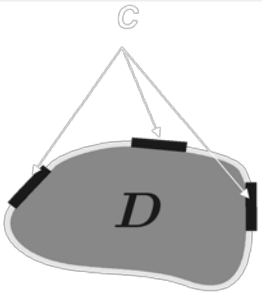
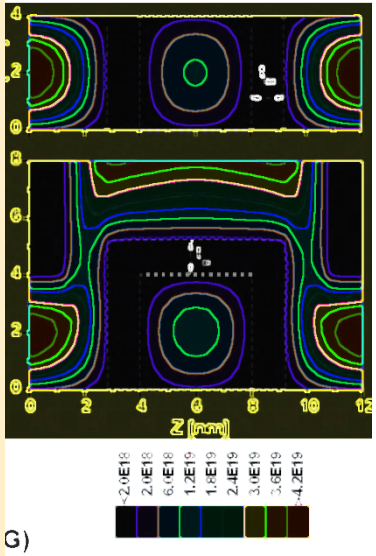




ON-state Electron density along the dotted line

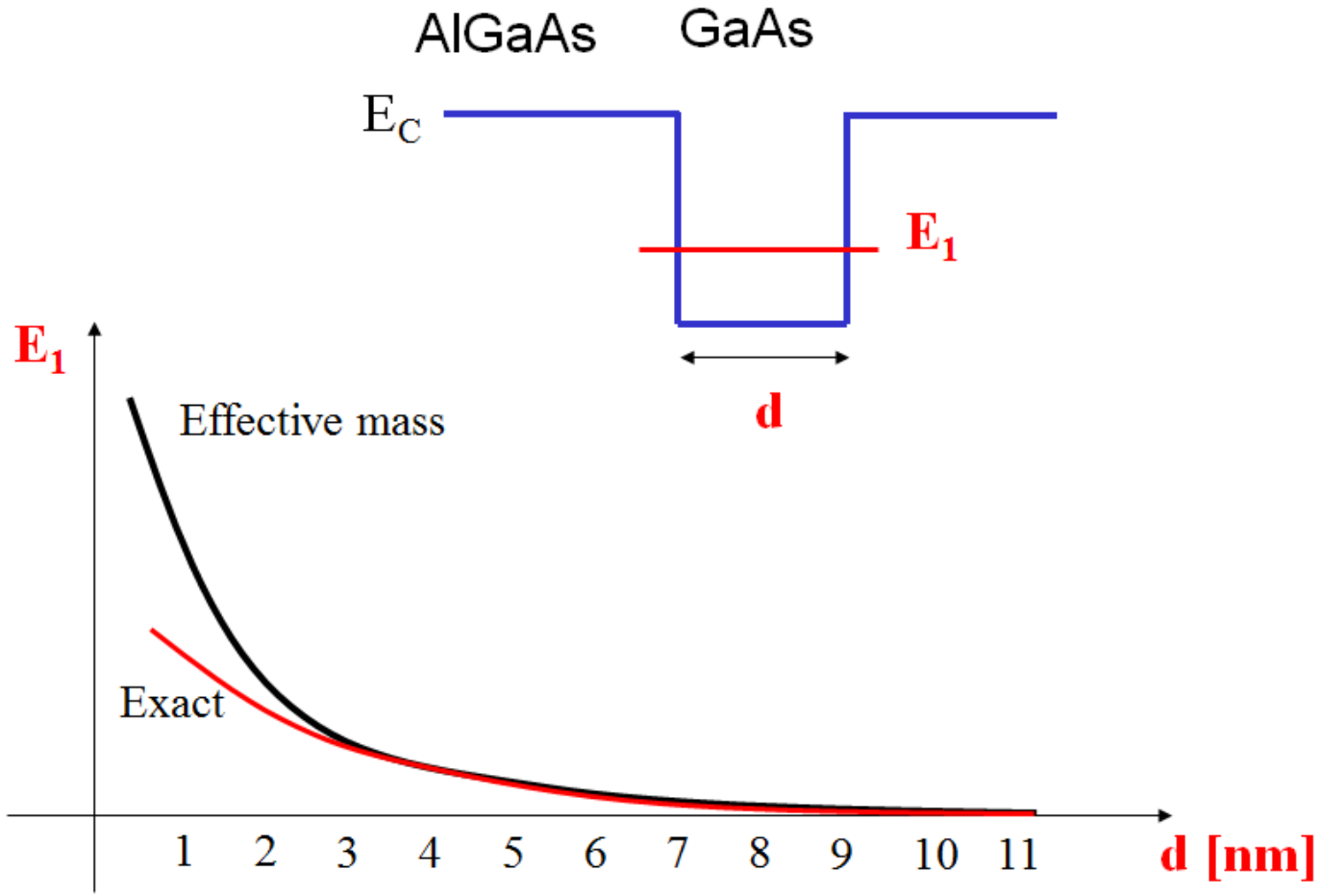


H. R. Khan, D. Mamaluy and D. Vasileska, *IEEE Transactions Electron Dev.* Vol. **55(8)**, pp. 2134 – 2141, August 2008.

Complexity of Methods

Method	Computational cost
Transfer matrix + QTBM	$N_E \times O\left(N_{TOTAL}^3\right)$
NanoMOS (Purdue University)	$N_E \times N_x \times O\left(\left[N_y N_z\right]^2\right) \approx N_E \times O\left(N_{TOTAL}^{5/3}\right)$
QDAME (IBM, S. Laux)	$N_{TOTAL} \times O\left(N_{eigen}^2\right) + N_E \times O\left(N_{TOTAL}^{3/2}\right)$
CBR	$N_{TOTAL} \times O\left(N_{eigen}^2\right) + N_E \times O\left(N_{TOTAL}\right)$
Notations N_E : number of energy steps; N_{TOTAL} : number of grid points N_{eigen} : number of eigenvalues	**CBR WINS !!!**

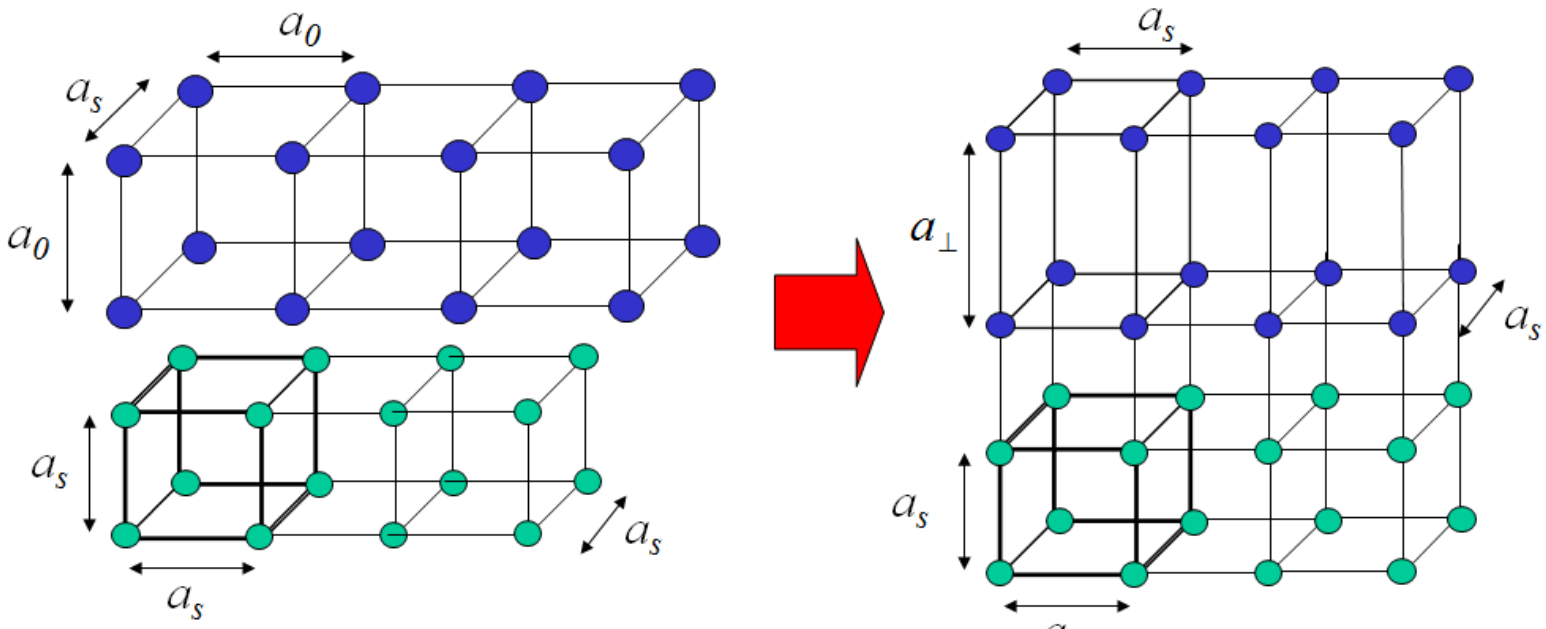
How good is effective mass approximation?



A. Di Carlo, private communication.

Strain

An epitaxial layer is grown, on a substrate with different lattice constant.
The epilayer deforms (strain)



$$a_\perp = a_0 - 2\frac{C_{12}}{C_{11}}[a_s - a_0] \quad \Longleftrightarrow \quad \mathbf{R}' = (1+\varepsilon)\mathbf{R}$$

A. Di Carlo, private communication.

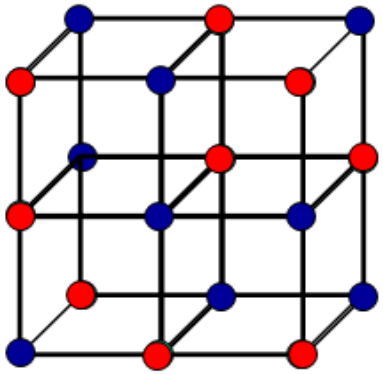
Disorder -Alloys

Usually, tight-binding parameterizations are made for single elments and binary compounds (Si, Ge, GaAs, InAs etc.). However, nanostructure are usually build by using also ternary (AlGaAs etc.) and quatrnary (InGaAsP etc.) alloys.

1) Supercell calculations

$A_{0.5}B_{0.5}C$

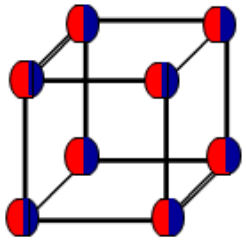
Average over an ensamble of configurations



2) Virtual crystal approximation

A new crystal is defined with averaged properties (P)

$$P(A_xB_{1-x}C) = x\,P(AC) + (1-x)\,P(BC)$$



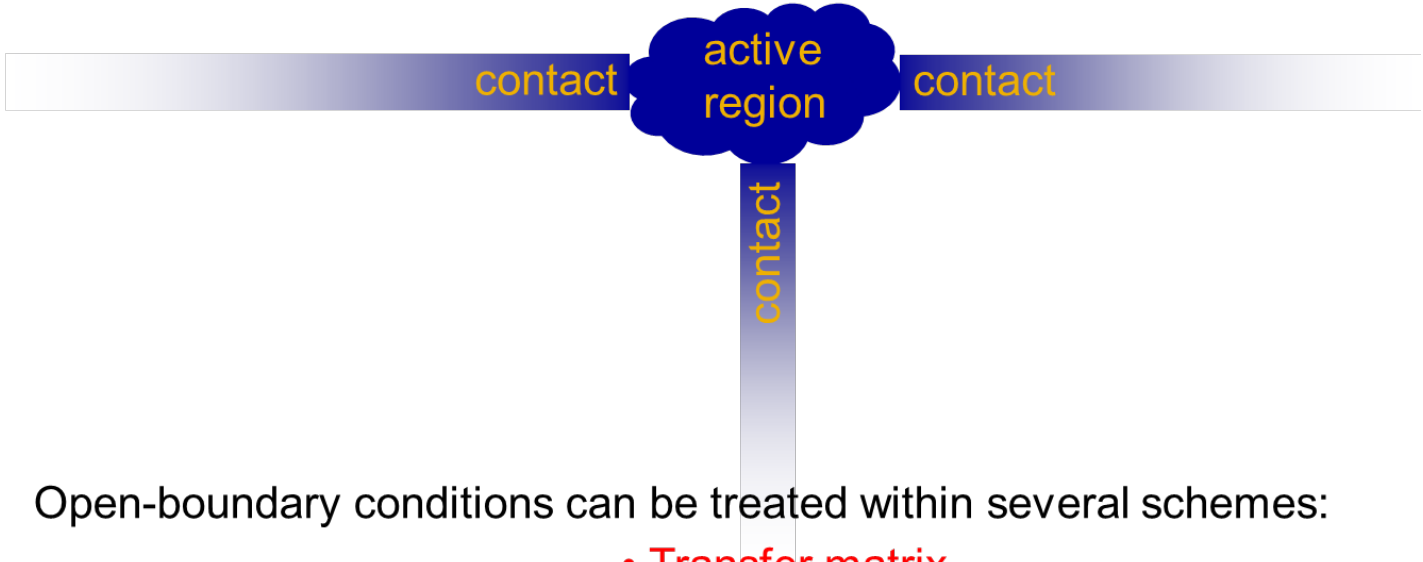
3) Other methods (Modified VCA, CPA, T-matrix etc.)

A. Di Carlo, private communication.

Boundary Conditions for Transport

The transport problem is:

active region where symmetry is lost
+
contact regions (semi-infinite bulk)



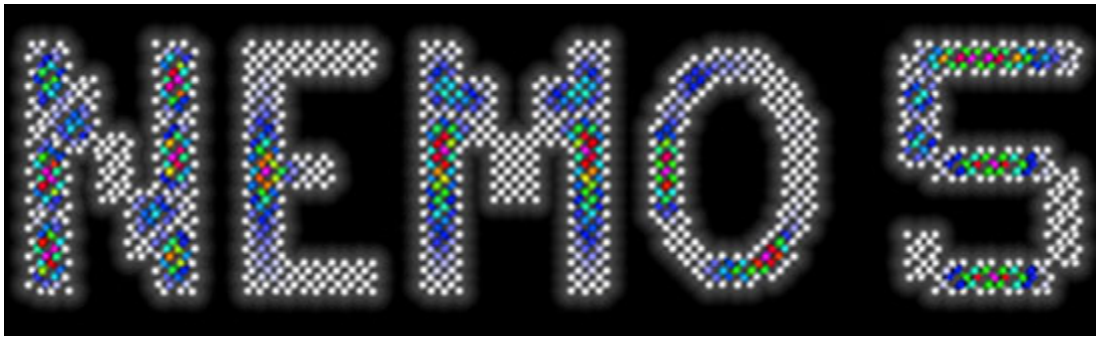
Open-boundary conditions can be treated within several schemes:

- Transfer matrix
- Green Functions

These schemes are well suited for localized orbital approach like TB

A. Di Carlo, Private Communication.

NEMO5: The Nanoelectronics Tool



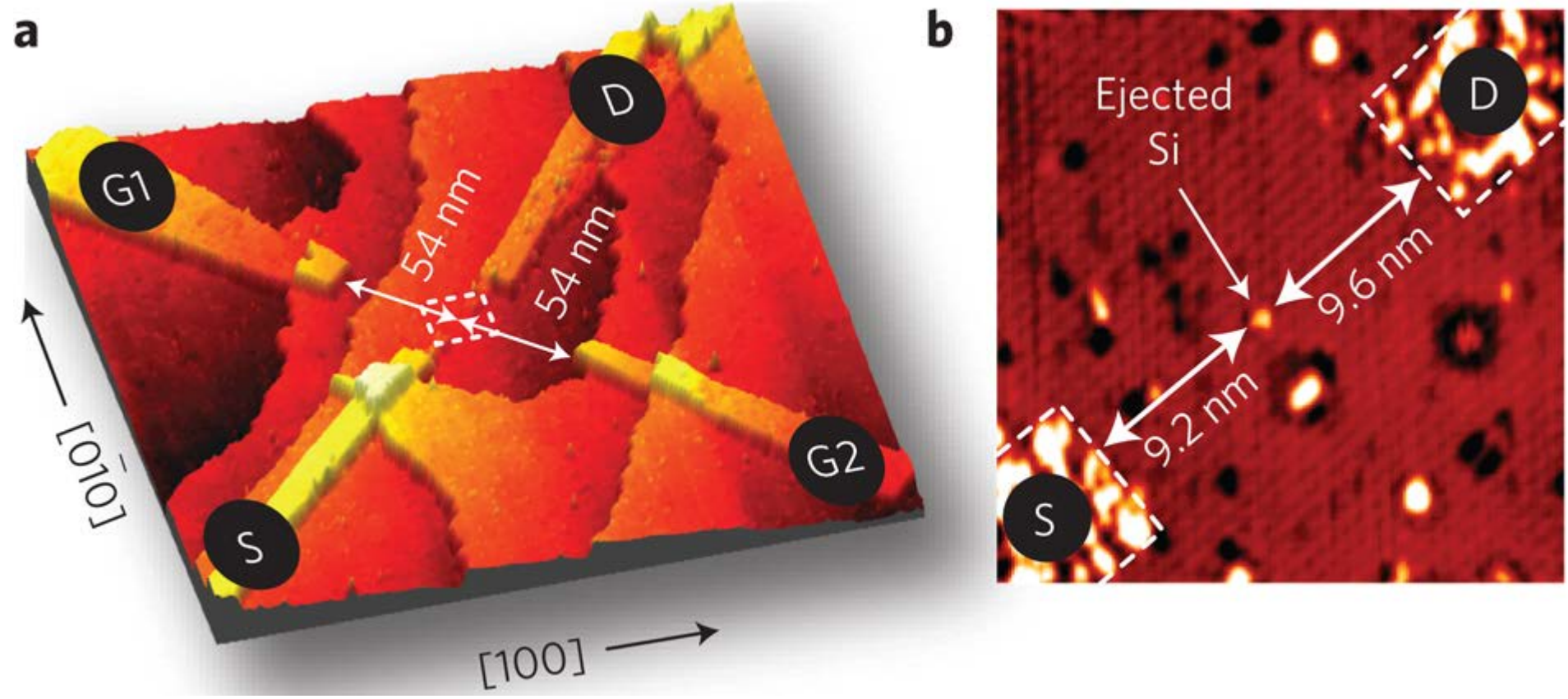
NEMO5 is the fifth edition of the NanoElectronics MOdeling Tools of the iNEMO group. It incorporates the core concepts and insights gained from 15 years of development of NEMO-1D, NEMO-3D, NEMO-3D-Peta and OMEN.

The core capabilities of NEMO5 lie in the atomic-resolution calculation of nanostructure properties:

strain relaxation, phonon modes, electronic structure using the tight-binding model, self-consistent **Schroedinger-Poisson calculations**, and **quantum transport**.

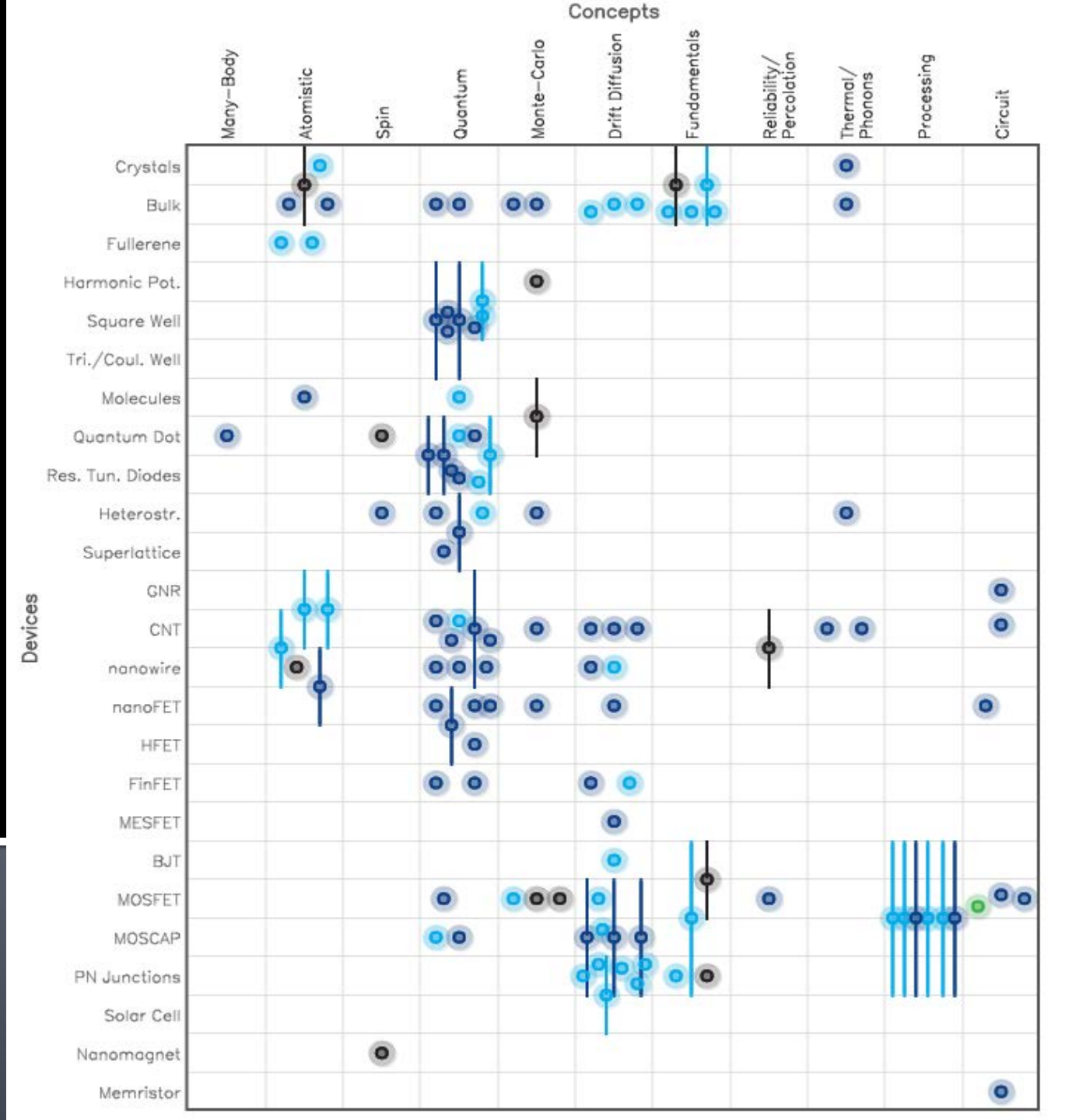
A representative Example: Single Atom Transistor

Martin Fuechsle, Jill A. Miwa, Suddhasatta Mahapatra, Hoon Ryu, Sunhee Lee, Oliver Warschkow, Lloyd C. L. Hollenberg, Gerhard Klimeck & Michelle Y. Simmons, *Nature Nanotechnology* **7**, 242–246 (2012) doi:10.1038/nnano.2012.21

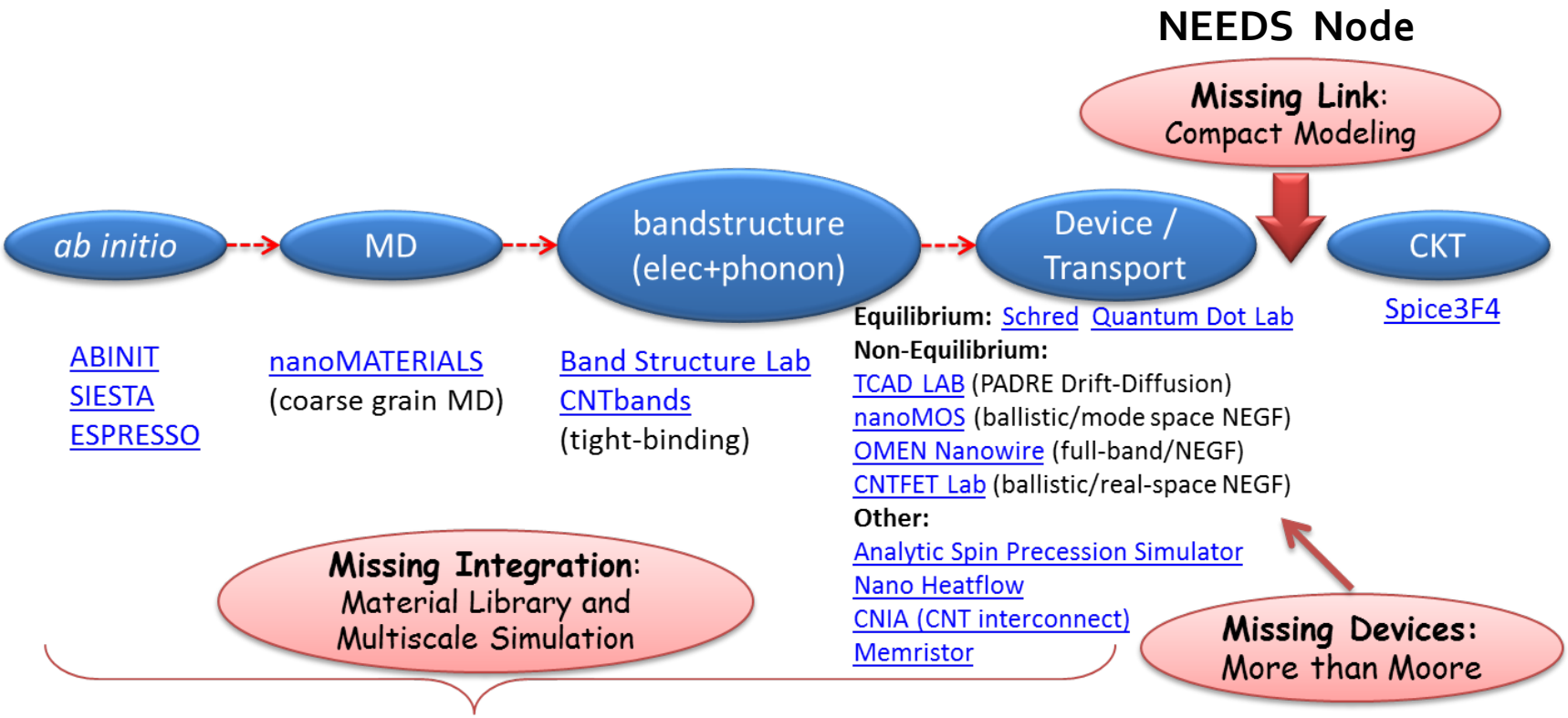


What nanoHUB Tools Can and Can't Do

A One Person's View


Concepts
Many–Body
Atomistic
Spin
Quantum
Monte–Carlo
Drift Diffusion
Fundamentals
Reliability/ Percolation
Thermal/ Phonons
Processing
Circuit
Devices
Crystals
Bulk
Fullerene
Harmonic Pot.
Square Well
Tri./Coul. Well
Molecules
Quantum Dot
Res. Tun. Diodes
Heterostr.
Superlattice
GNR
CNT
nanowire
nanoFET
HFET
FinFET
MESFET
BJT
MOSFET
MOSCAP
PN Junctions
Solar Cell
Nanomagnet
Memristor

What nanoHUB Can /Can't Do

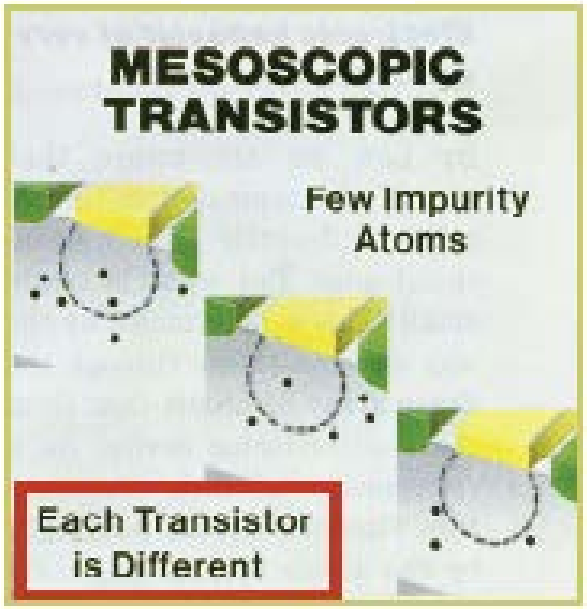


Can't Do Random Dopant Fluctuations

Random Dopants

PAST

PRESENT



all transistors are similar because of *self averaging*

Experimental Evidence of RDF

Experimental Study of Threshold Voltage Fluctuation Due to Statistical Variation of Channel Dopant Number in MOSFET's

Tomohisa Mizuno, *Member, IEEE*, Jun-ichi Okamura, *Member, IEEE*, and Akira Toriumi, *Member, IEEE*

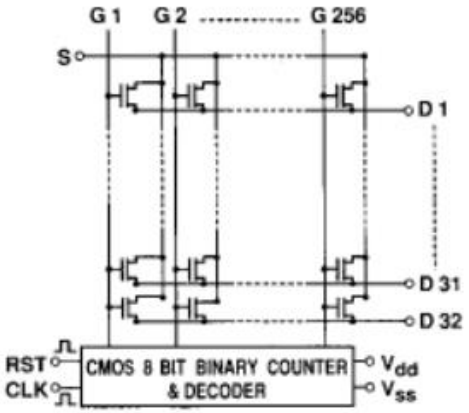


Fig. 1. New test structure which consists of the 8 k-NMOSFET array and the CMOS peripheral circuits (the CMOS counter and the CMOS decoders). RST and CLK show the reset and the clock terminals, respectively. *(Reprinted from: T. Mizuno, J. Okamura, and A. Toriumi, "Experimental Study of Threshold Voltage Fluctuations Using an 8K MOSFET's Array," Technical Papers of Symposium on VLSI Technology, Kyoto, Japan, p. 41, 1993.)*

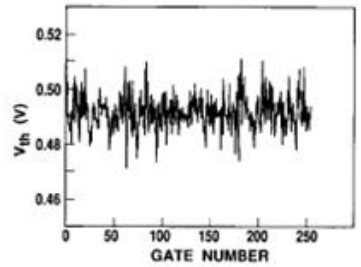


Fig. 4. Threshold voltage versus the gate number in 256 NMOSFET's, where $L_{ef} = 0.5\ \mu m$, $T_{ox} = 11 nm$, and $\overline{N}_a = 7.1 \times 10^{16}\ cm^{-3}$. *(Reprinted from: T. Mizuno, J. Okamura, and A. Toriumi, "Experimental Study of Threshold Voltage Fluctuations Using an 8K MOSFET's Array," Technical Papers of Symposium on VLSI Technology, Kyoto, Japan, p. 41, 1993.)*

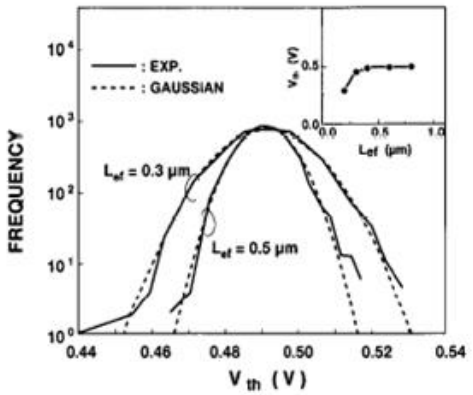
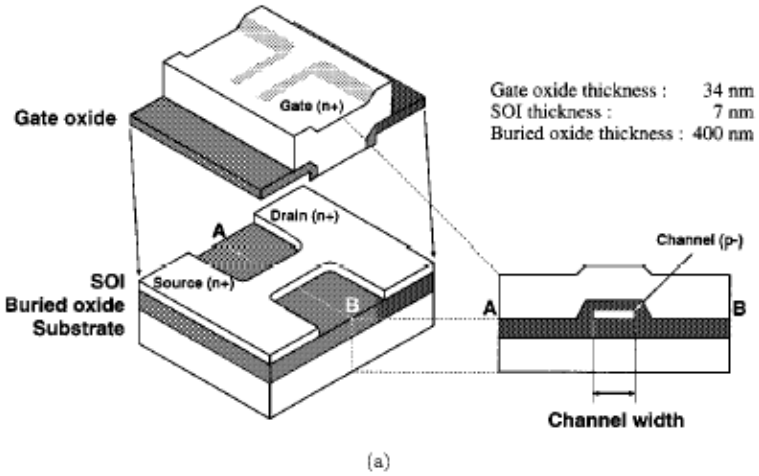


Fig. 6. V_{th} distribution of 8 k-MOSFET array at $L_{ef} = 0.5\ \mu m$ and 0.3 μm, where $T_{ox} = 11$ nm and $\overline{N}_a = 7.1 \times 10^{16}\ cm^{-3}$. The vertical axis shows the frequency. The solid and the dashed lines show the experimental data and the calculated Gaussian distribution, respectively. The inset shows V_{th} as a function of L_{ef}.

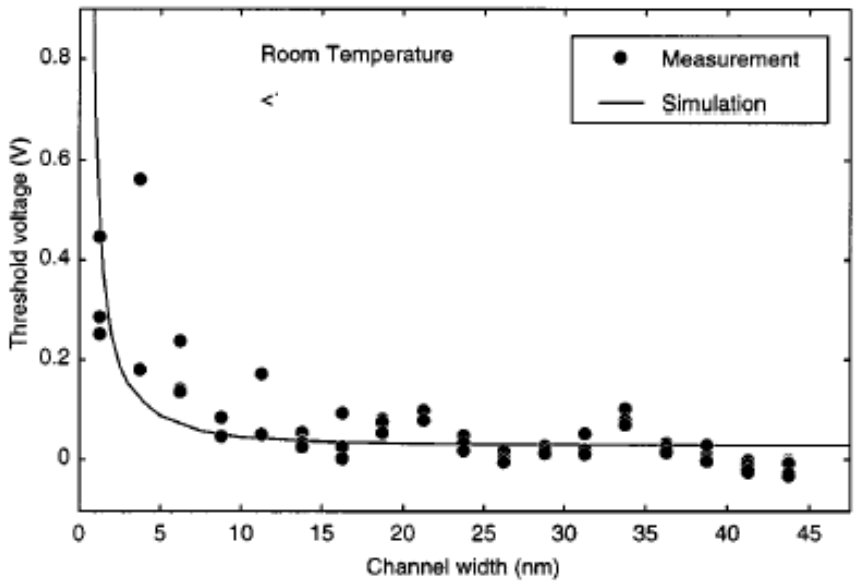
Unintentional Dopants?



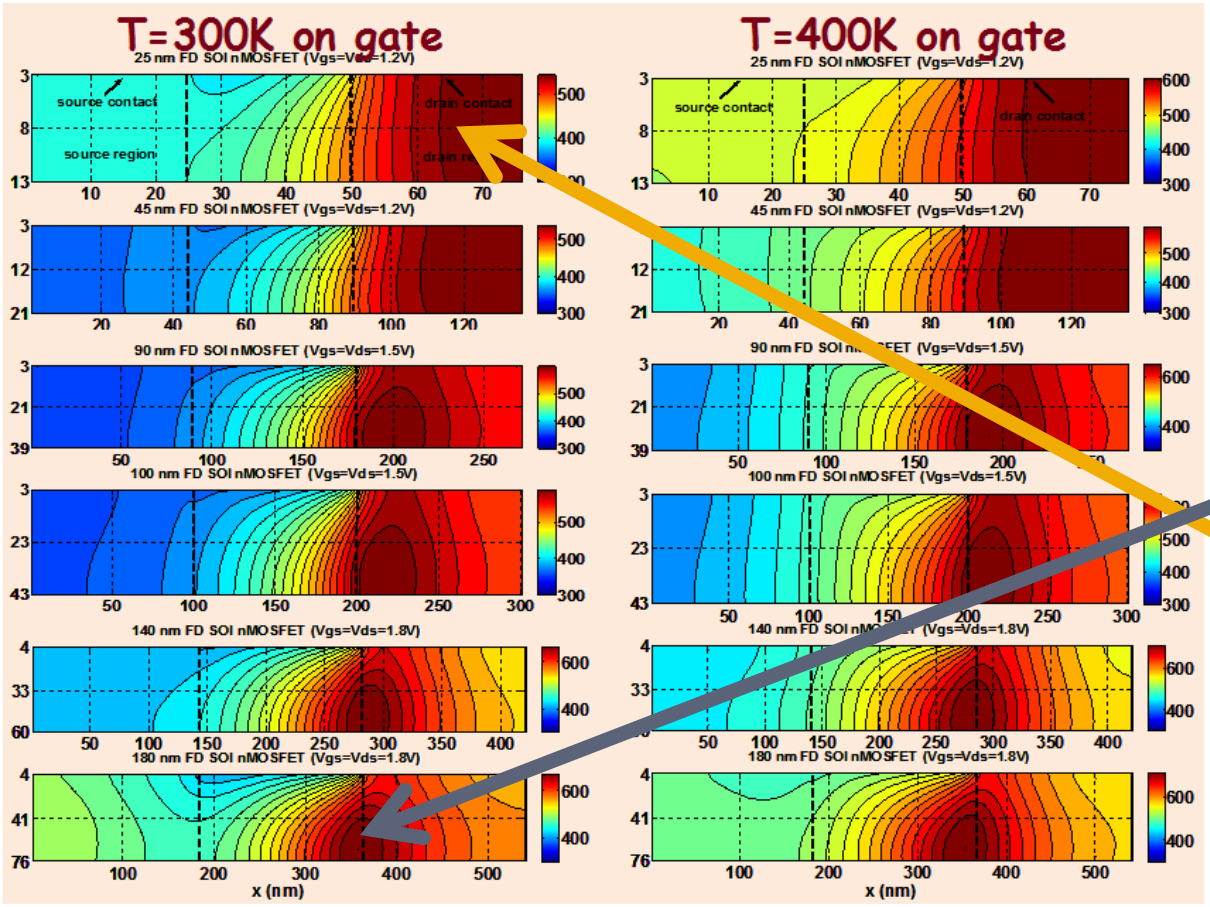
396 IEEE ELECTRON DEVICE LETTERS, VOL. 21, NO. 8, AUGUST 2000

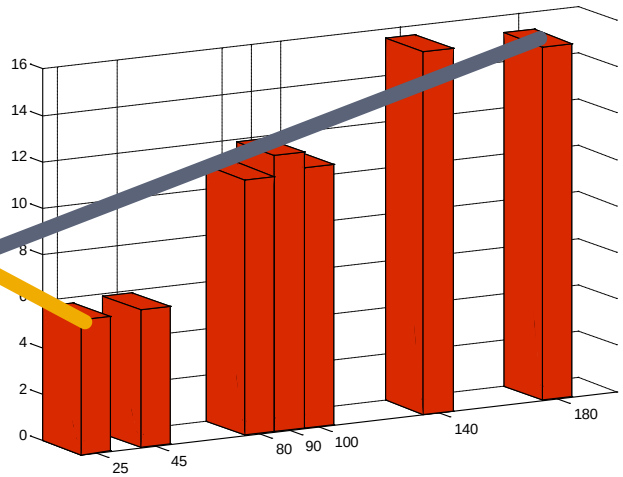
Experimental Evidence for Quantum Mechanical Narrow Channel Effect in Ultra-Narrow MOSFET's

H. Majima, H. Ishikuro, and T. Hiramoto, *Member, IEEE*



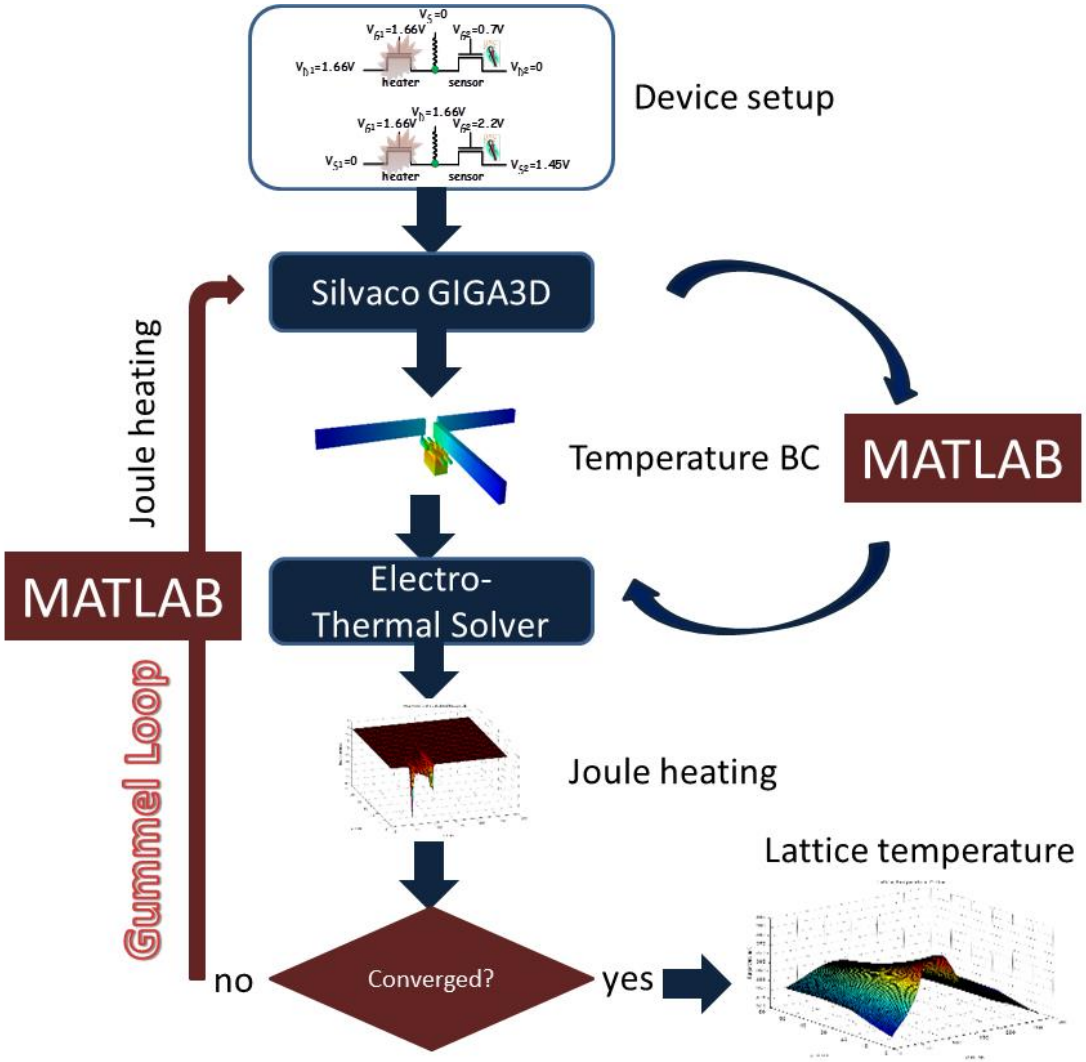
Can't Do Self-Heating at the Device Level



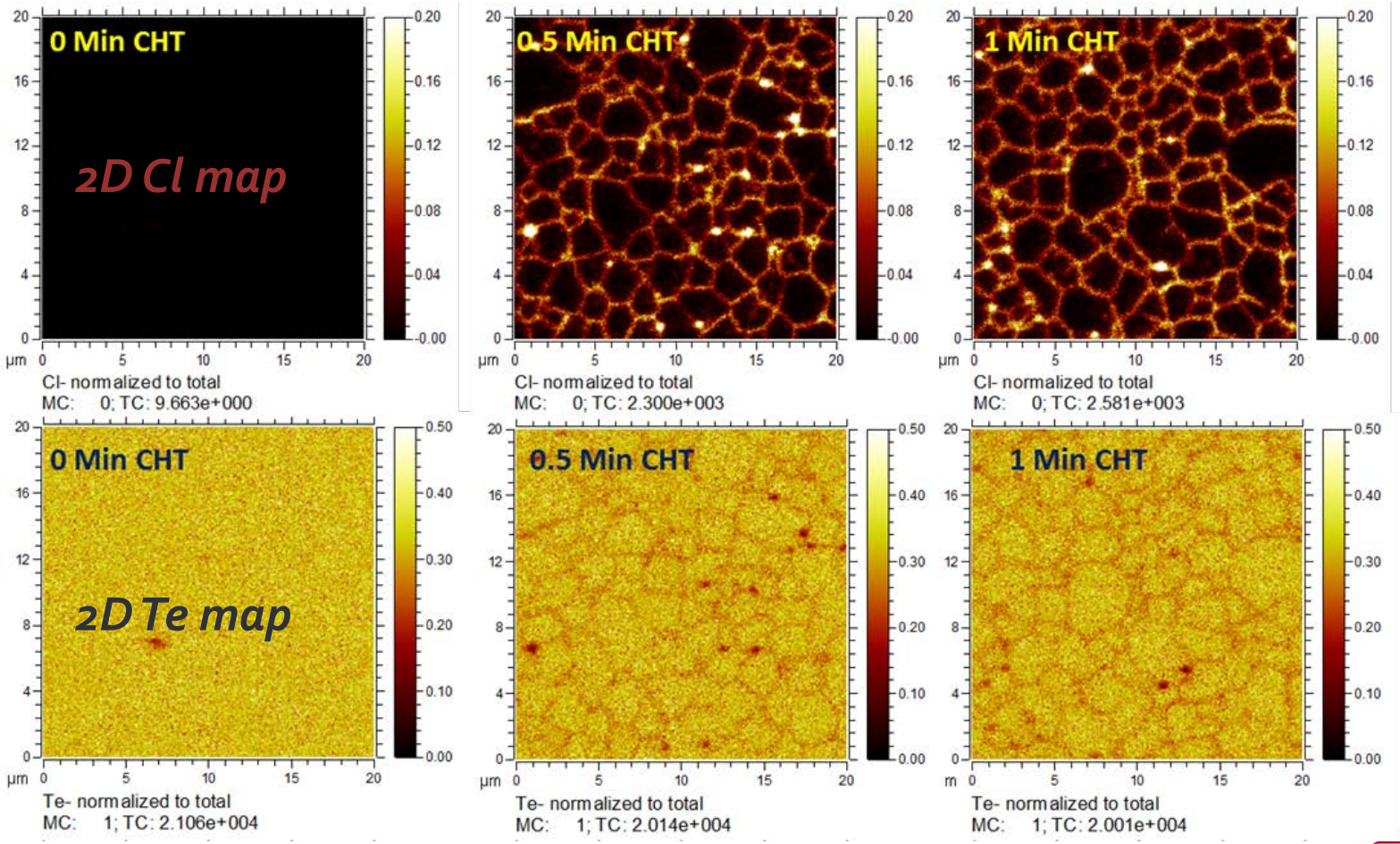


K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov, Modeling Thermal Effects in Nanodevices, IEEE Transactions on Electron Devices, vol. 55, issue 6, pp. 1306-1316, June 2008

Multi-Scale Simulations

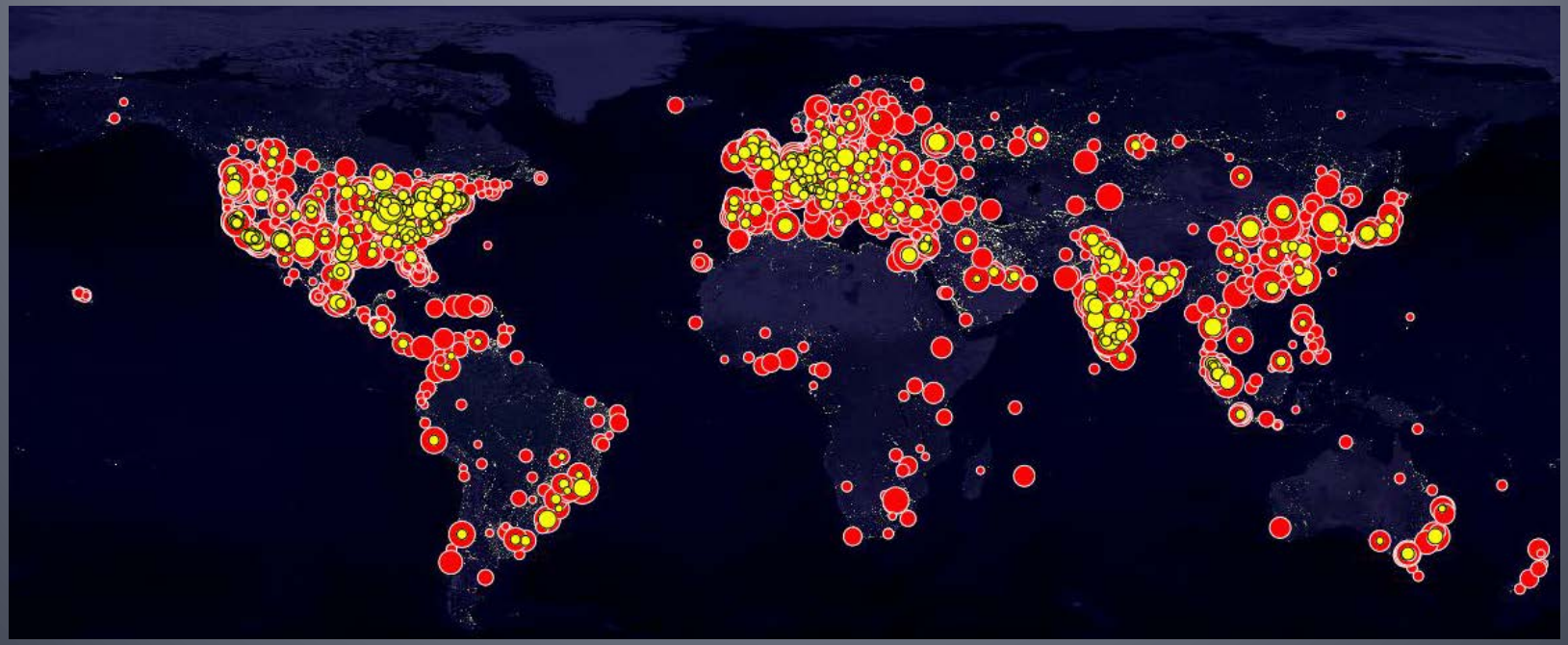


Optoelectronics? What are we missing?



Conclusions

One picture is worth a million words!



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