

Silvaco Atlas TCAD

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Listing 1. Simulation of SAL TFT.

```
#
# 30 nm IGZO SAL TFT with interface traps
#
go atlas simflags="-P 8"

# Simulated device is scaled in x-z direction
# by 0.1x relative to real device (for finer mesh)
mesh width=200 outf=tft_IGZO.str master.out

x.m l=0 s=1
x.m l=4 s=0.1
x.m l=26 s=0.1
x.m l=30 s=1

y.m l=0 s=0.002
y.m l=0.03 s=0.0005
y.m l=0.13 s=0.010

# IGZO layer
region num=1 material=igzo y.min=0.000 y.max=0.030
# GI
region num=2 material=sio2 y.min=0.030 y.max=0.130

# Electrodes
elec num=1 name=gate bottom
elec num=2 name=source y.max=0.0 x.min=0.0 x.max=5
elec num=3 name=drain y.max=0.0 x.min=25 x.max=30
# Gate
contact num=1 p.poly
# Source/drain
contact num=2 workf=4.16
contact num=3 workf=4.16

# Set IGZO band gap, mobility, electron affinity, rel. permittivity, and effective CB/VB DOS
material region=1 eg300=3.20 mun=15 affinity=4.16 permit=10 nc300=5e18 nv300=3e19 print

# Use Fermi statistics
models fermi

# IGZO bulk DOS
defects nta=1.21e20 ntd=1.55e20 wta=0.030 wtd=0.110 \
ngd=1e16 egd=2.95 wgd=0.1 \
nga=3.2e17 ega=2.0 wga=0.1 \
dfile=IGZO_bulk_don.dat afile=IGZO_bulk_acc.dat continuous numa=200 numd=200

# IGZO interface DOS
intdefects intnumber=1/2 nta=0 ntd=0 wta=0 wtd=0 \
ngd=6.0e11 egd=2.95 wgd=0.1 nga=0 ega=0 wga=0 \
dfile=IGZO_int_don.dat afile=IGZO_int_acc.dat continuous numa=200 numd=200

# Probe Fermi level position
output con.band val.band
probe name=my_fermi_front x=15 y=0.0298 QFN
probe name=my_con_front x=15 y=0.0298 CON.BAND
probe name=my_con_back x=15 y=0.0 CON.BAND
```

```

# Simulate transfer curve
solve init
save outf=tftIGZO_init.str
# Ramp drain bias
solve vdrain=0 vstep=0.1 vfinal=0.5 name=drain
save outf=tftIGZO_D05V.str

# Ramp gate bias
log outf=tftIGZO_neg.log
solve vgate=0 vstep=-0.1 vfinal=-5 name=gate
solve vstep=-0.2 vfinal=-10 name=gate
save outf=tftIGZO_negG10V.str
log off
load inf=tftIGZO_D05V.str master
solve prev
log outf=tftIGZO_pos.log
solve vstep=0.1 vfinal=5 name=gate
solve vstep=0.2 vfinal=20 name=gate
save outf=tftIGZO_G20V.str
log off

exit

```

Listing 2. Simulation of DAL TFT.

```

#
# 3 nm ITO / 27nm IGZO DAL TFT
#
go atlas simflags="-P 8"

# Simulated device is scaled in x-z direction
# by 0.1x relative to real device (for finer mesh)
mesh width=200 outf=tft_IGZO.str master.out

x.m l=0 s=1
x.m l=4 s=0.1
x.m l=26 s=0.1
x.m l=30 s=1

y.m l=0.000 s=0.002
y.m l=0.027 s=0.0005
y.m l=0.030 s=0.0005
y.m l=0.130 s=0.010

# IGZO layer
region num=1 material=igzo y.min=0.000 y.max=0.027
# ITO layer
region num=3 material=igzo y.min=0.027 y.max=0.030
# GI
region num=2 material=sio2 y.min=0.030 y.max=0.130

# Electrodes
elec num=1 name=gate bottom
elec num=2 name=source y.max=0.0 x.min=0.0 x.max=5
elec num=3 name=drain y.max=0.0 x.min=25 x.max=30
# Gate
contact num=1 p.poly
# Source/drain
contact num=2 workf=4.16
contact num=3 workf=4.16

```

```

# Set IGZO band gap, mobility, electron affinity, rel. permittivity, and effective CB/VB DOS
material region=1 eg300=3.20 mun=15 affinity=4.16 permit=10 nc300=5e18 nv300=3e19 print
# Set ITO band gap, mobility, electron affinity, rel. permittivity, and effective CB/VB DOS
material region=3 eg300=3.20 mun=35 affinity=4.16 permit=9 nc300=4.1e18 nv300=3e19 print
# ITO carrier concentration
doping region=3 uniform n.type concentration=3.63e18

# Use Fermi statistics
models fermi

# IGZO bulk DOS
defects number=1 nta=1.21e20 ntd=1.55e20 wta=0.030 wtd=0.110 \
ngd=1e16 egd=2.95 wgd=0.1 \
nga=3.2e17 ega=2.0 wga=0.1 \
dfile=IGZO_bulk_don.dat afile=IGZO_bulk_acc.dat continuous numa=200 numd=200

# ITO bulk DOS
defects number=3 nta=2.2e20 ntd=1.55e20 wta=0.018 wtd=0.110 \
ngd=0 egd=2.95 wgd=0.1 \
nga=0 ega=2.0 wga=0.1 \
dfile=ITO_bulk_don.dat afile=ITO_bulk_acc.dat continuous numa=200 numd=200

# Probe Fermi level position
output con.band val.band
probe name=my_fermi_front x=15 y=0.0298 QFN
probe name=my_con_front x=15 y=0.0298 CON.BAND
probe name=my_con_back x=15 y=0.0 CON.BAND

# Simulate transfer curve
solve init
save outf=tftIGZO_init.str
# Ramp drain bias
solve vdrain=0 vstep=0.1 vfinal=0.5 name=drain
save outf=tftIGZO_D05V.str
# Ramp gate bias
log outf=tftIGZO_neg.log
solve vgate=0 vstep=-0.1 vfinal=-5 name=gate
solve vstep=-0.2 vfinal=-10 name=gate
save outf=tftIGZO_negG10V.str
log off
load inf=tftIGZO_D05V.str master
solve prev
log outf=tftIGZO_pos.log
solve vstep=0.1 vfinal=5 name=gate
solve vstep=0.2 vfinal=20 name=gate
save outf=tftIGZO_G20V.str
log off

exit

```