p-bits for Probabilistic Spin Logic (PSL)

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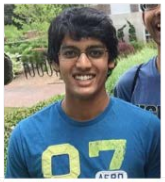

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Sponsors

NSF

SRC

C-SPIN The Center for Spintronic Materials

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INDEX INSTITUTE FOR NANOELECTRONICS DISCOVERY AND EXPLORATION

1a. Bits, q-bits and p-bits

Hard disks
MRAM / MTJ's

CMOS /
Stable magnets

Single
spins

Bits

either
0 or 1

Digital
computing

q-bits

delicate
superposition
of 0 & 1

Quantum
computing

1b. Bits, q-bits and p-bits

Hard disks
MRAM / MTJ's

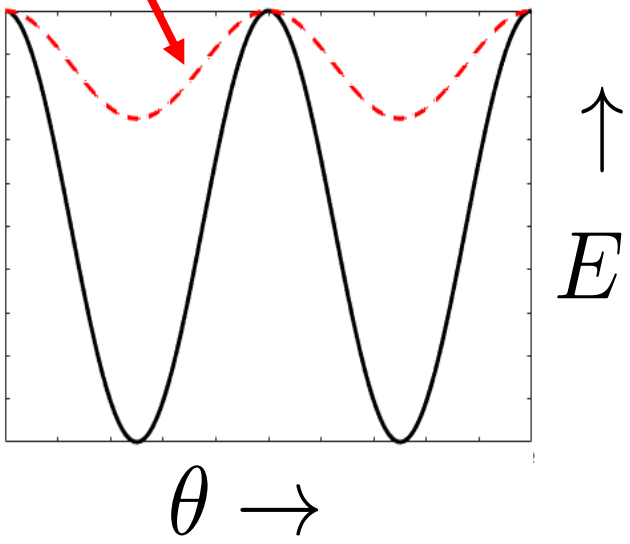
Stable magnets

Bits

either
0 or 1

Digital
computing

Unstable magnets

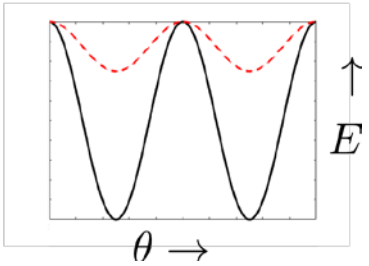


Single spins

q-bits
delicate
superposition
of 0 & 1

Quantum
computing

1c. Bits, q-bits and p-bits



CMOS / Stable magnets

Unstable magnets

Single spins

Bits

p-bits

q-bits

either 0 or 1

fluctuate between 0 & 1

delicate superposition of 0 & 1

Room temperature

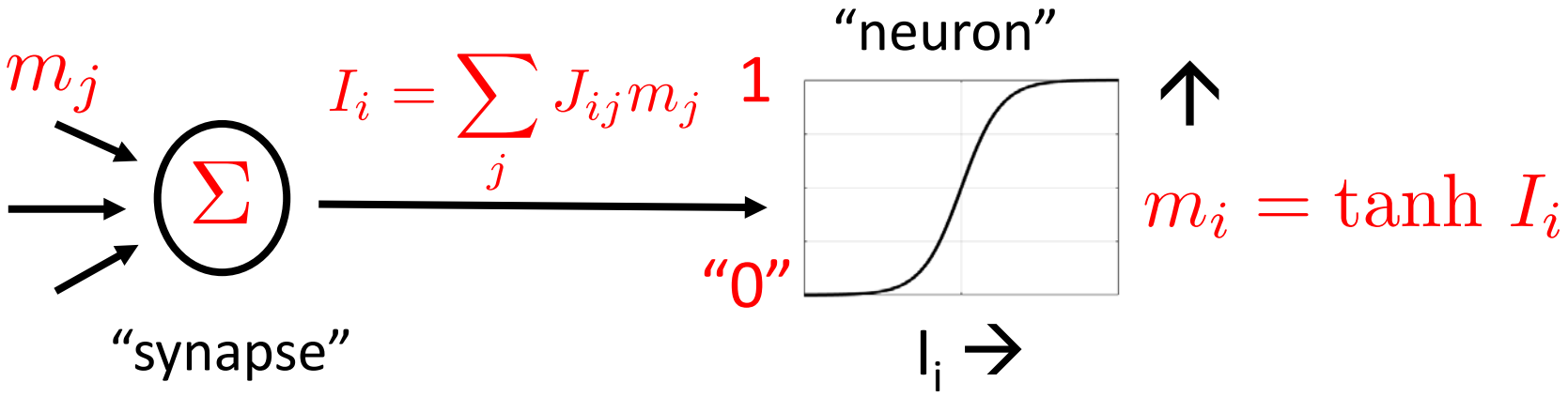
Digital computing

p- circuits
p- computing

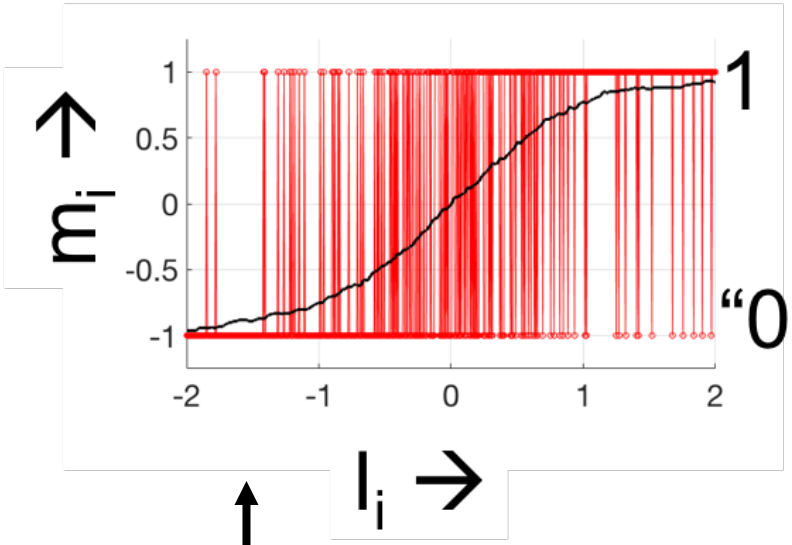
Quantum computing

Feynman 1982

2a. *p-bit:* Binary stochastic neuron



2b. p-bit: Binary stochastic neuron



$$I_i = \sum_j J_{ij} m_j$$

m_j

Σ

"synapse"

"neuron"

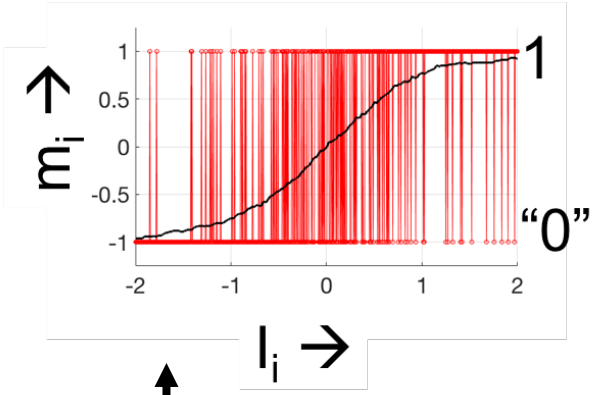
1

"0"

$m_i = \tanh I_i$

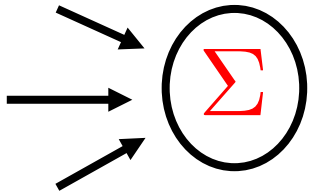
I_i

2c. p-bit: Binary stochastic neuron



$$I_i = \sum_j J_{ij} m_j$$

m_j

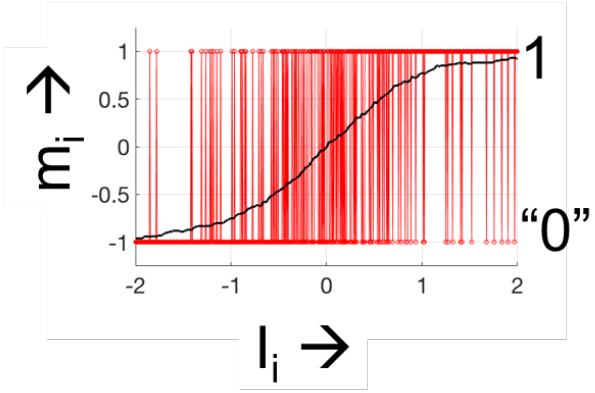


"synapse"

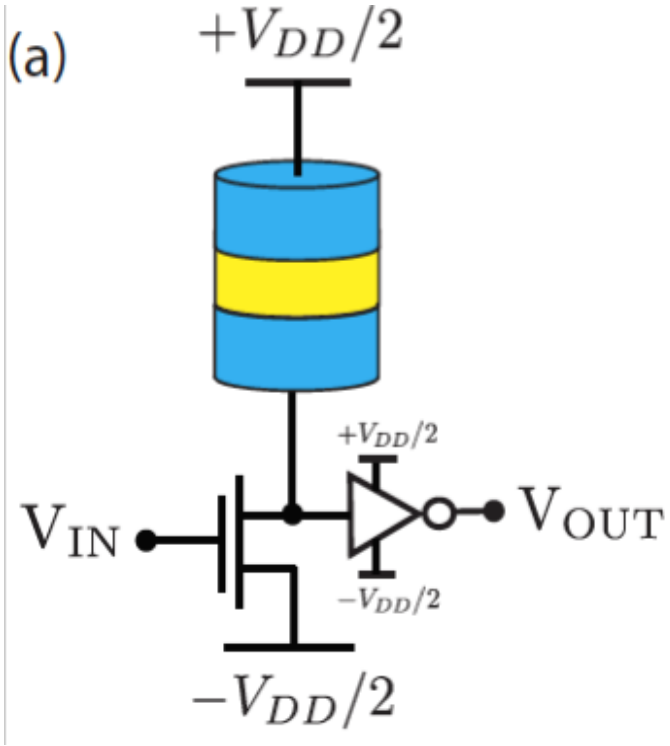
V_{OUT} V_{IN}

$$m_i = \mathrm{sgn}\{\tanh I_i + \mathrm{rand}(-1,1)\}$$

3. p-bit: nMOS + MTJ



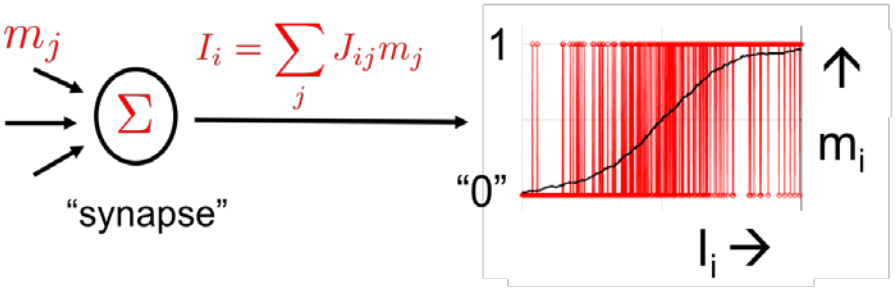
$$m_i = \mathrm{sgn}\{\tanh I_i + \mathrm{rand}(-1,1)\}$$



$$\overbrace{\frac{V_{OUT,i}}{V_{DD}/2}}^{m_i} \approx \mathrm{sgn}\left\{\tanh \overbrace{\frac{V_{IN,i}}{V_0}}^{I_i} + \mathrm{rand}(-1,1)\right\}$$

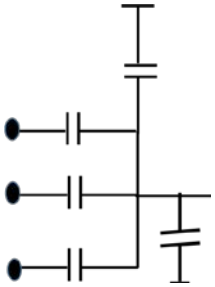
nMOS + MTJ Camsari et al. EDL 2017

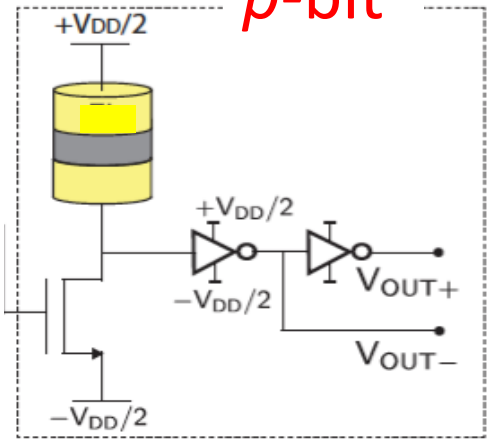
4a. Applications



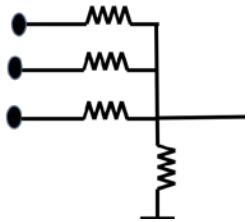
Building Block

p-bit

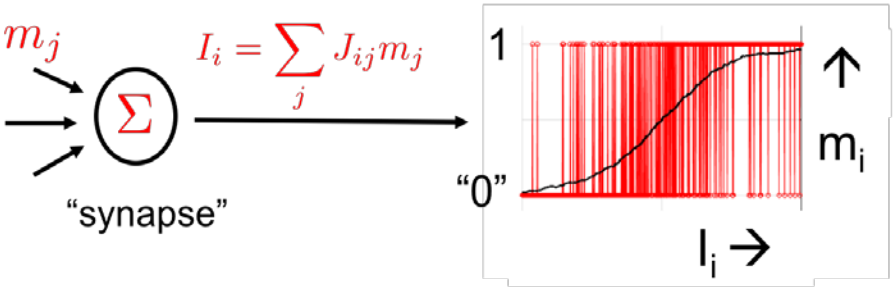




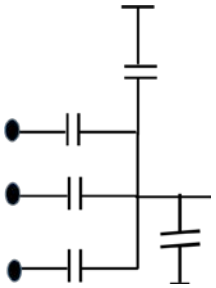
Many other possibilities



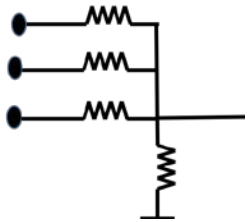
4b. Applications



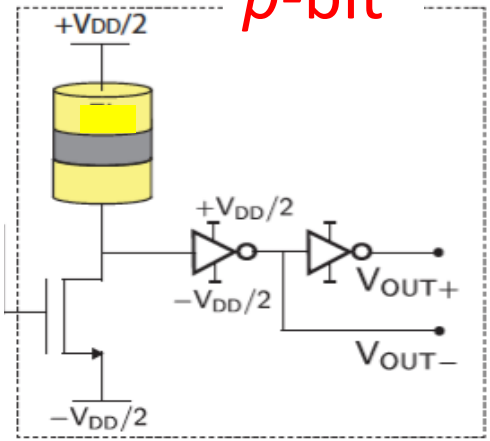
Building Block



Many other possibilities



p-bit



New application spaces for embedded MRAM

- Bayesian
- Invertible Boolean
- Image recognition
- Optimization

.... Machine Learning ....

Discussed in separate 45-minute talk

For more details …

➢ Bayesian Inference and Optimization

[1] B.Behin-Aein, V.Diep and S.Datta
"A Building Block for Hardware Belief Networks", Scientific Reports **6**, 29893 (2016).
[2] B.M. Sutton, K.Y. Camsari, B. Behin-Aein and S.Datta
"Intrinsic optimization using stochastic nanomagnets" Scientific Reports, **7**, 44370 (2017).

➢ Invertible Boolean

[3] K.Y. Camsari, R.Faria, B.M.Sutton and S.Datta
"Stochastic p-bits for Invertible Boolean Logic" Phys. Rev. X, **3,** 031014 (2017).
[4] R. Faria, K.Y. Camsari and S. Datta
" Low Barrier Nanomagnets as p-bits for Spin Logic" IEEE Magnetics Letters, **8**, 4105305 (2017).

➢ Non-magnetic implementation

[5] A.Z.Pervaiz, L.A.Ghantasala, K.Y. Camsari and S.Datta,
"Hardware Emulation of Stochastic p-bits for Invertible Logic," Scientific Reports, **7,** 10994 (2017).
[6] A.Z.Pervaiz, L.A.Ghantasala, B.M.Sutton and K.Y. Camsari
"Weighted p-bits for FPGA implementation of probabilistic circuits," *arxiv.org/abs/1712.04166*

➢ Embedded MRAM based implementation

[7] K.Y. Camsari, S. Salahuddin and S.Datta
"Implementing p-Bits with Embedded MTJ's," IEEE Electron Device Letters, **38,** 1767 (2017).
[8] O.Hassan, K.Y.Camsari and S.Datta
"Voltage-driven Building Block for Hardware Belief Networks," *arxiv.org/abs/**1801.09026***
[9] R.Faria, K.Y.Camsari and S.Datta
"Implementing Bayesian Networks with Embedded MRAM," *AIP Advances,* **8,** 045101