ME290R: Topics in Manufacturing
Fall 2017

Nanoscale manipulation of materials

Lecture 1: Introduction
August 23, 2017

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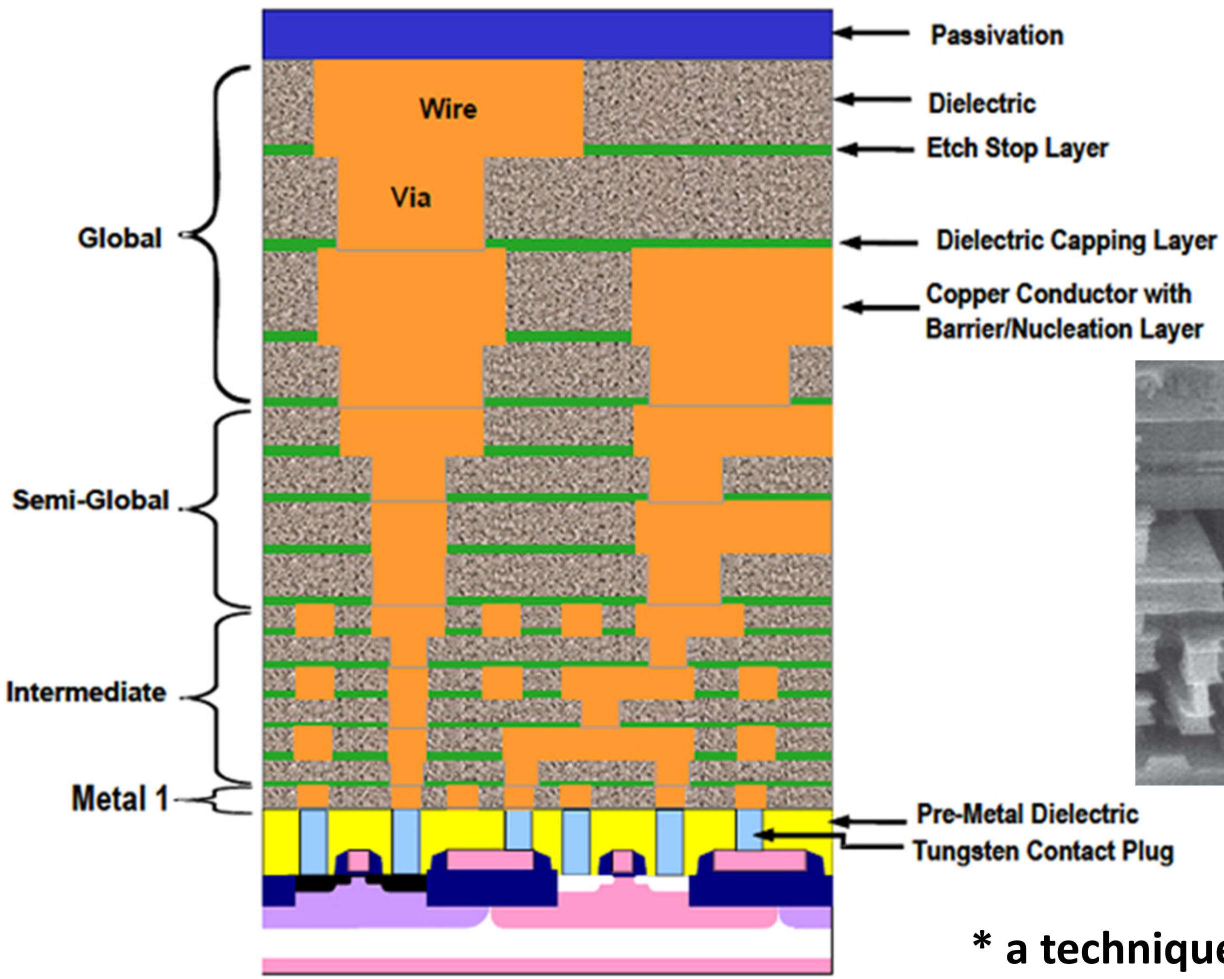
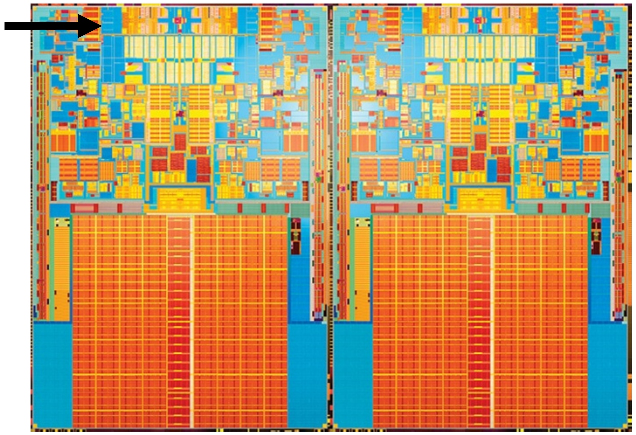
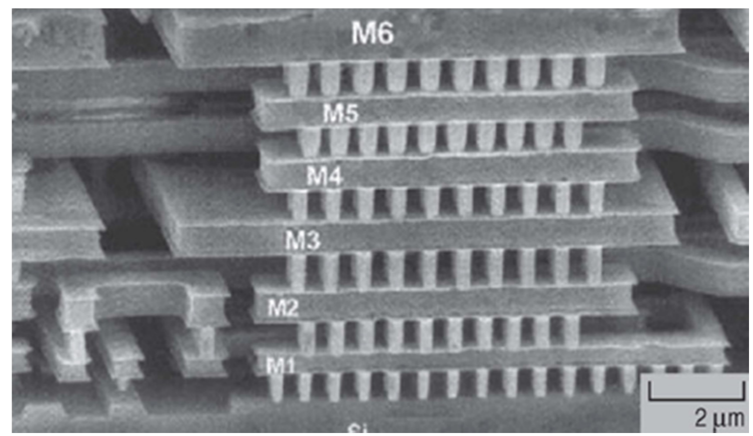
The semiconductor industry drives innovation in nanoscale *lithography**



Quad core die photo (Intel)



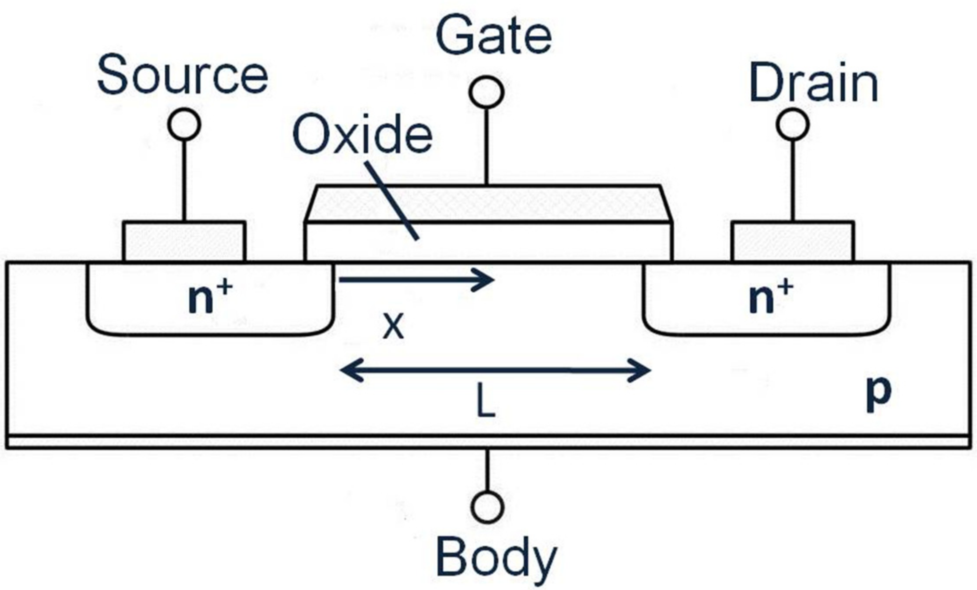


*** a technique for repeatable pattern transfer on to a solid surface**

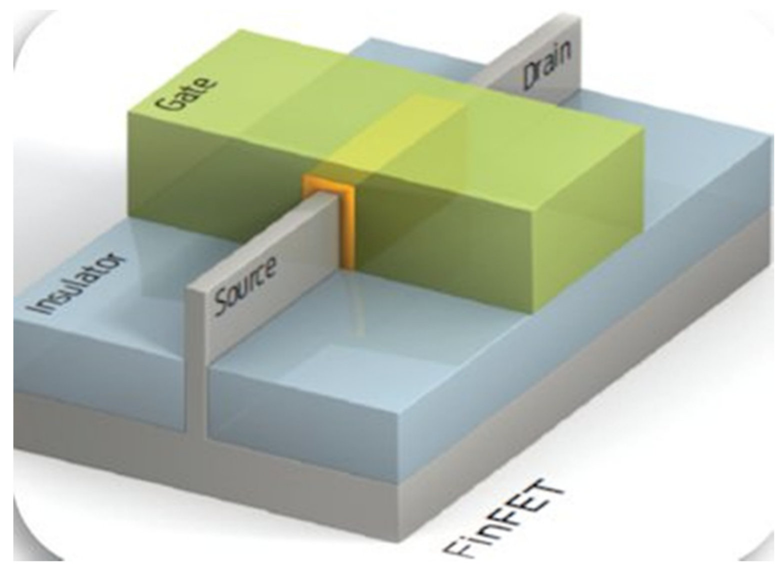
ITRS, tms.org, Intel

Field effect transistors in integrated circuits have undergone changes in physical structure, involving increasingly fine features

Traditional planar structure



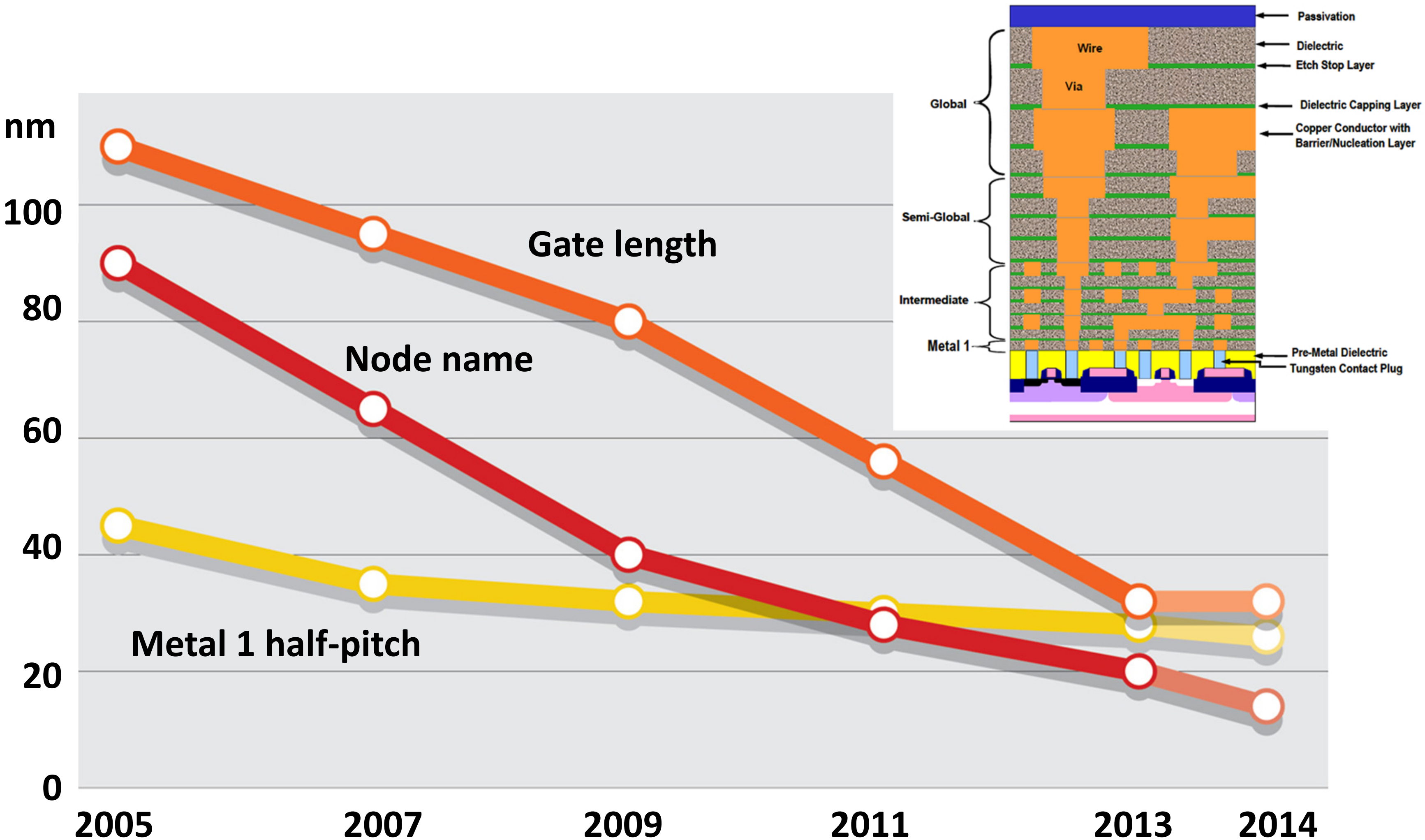
FinFET structure:
Gate 35 nm long, 8 nm wide in Intel's "22 nm" node technology



Alternative structure: silicon-on-insulator (SOI)

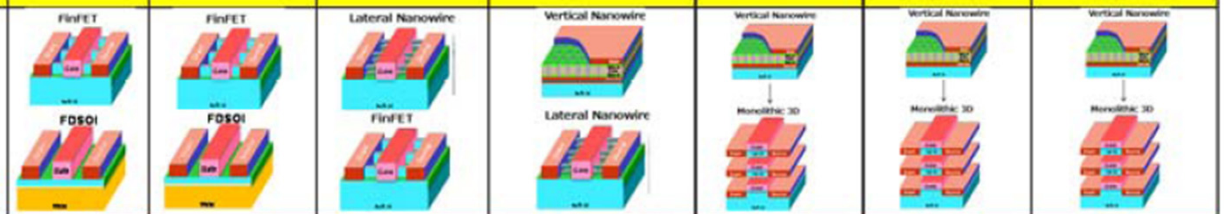
NUS, techreport.com

What does the “node” name mean in semiconductor manufacturing?



Global Foundries / IEEE Spectrum Oct 2013

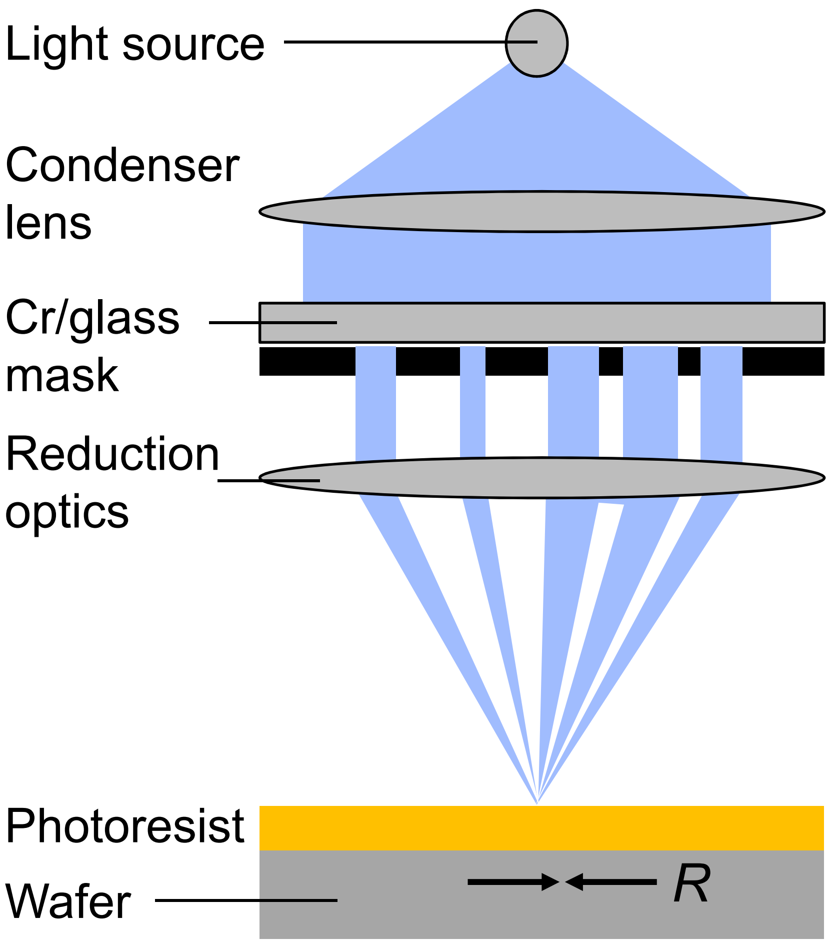
Features sizes are projected to shrink for just a couple more years…

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P54M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
							
LOGIC DEVICE GROUND RULES							
MPU/SoC Metalx ½ Pitch (nm)[1,2]	28.0	18.0	12.0	10.0	6.0	6.0	6.0
MPU/SoC Metal0/1 ½ Pitch (nm)	28.0	18.0	12.0	10.0	6.0	6.0	6.0
Contacted poly half pitch (nm)	35.0	24.0	21.0	16.0	12.0	12.0	12.0
L_g: Physical Gate Length for HP Logic (nm) [3]	24	18	14	10	10	10	10
L_g: Physical Gate Length for LP Logic (nm)	26	20	16	12	12	12	12
Channel overlap ratio - two-sided	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Spacer width (nm)	12	8	6	5	4	4	4
Contact CD (nm) - finFET, LGAA	22	14	16	12	11	11	11
Device architecture key ground rules							

International Roadmap for Devices and Systems 2016

Optical lithography is facing resolution and cost limitations: what are the alternatives?

Photolithography system (hugely simplified diagram)



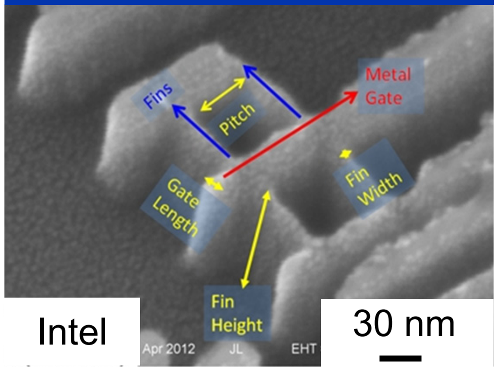
Process-dependent constant, *k*

- **Source–mask optimization**
- **Double/triple patterning**
- **Optical proximity correction**

Wavelength
193 nm (ArF)

$$\text{Resolution, } R = k\frac{\lambda}{\text{NA}}$$

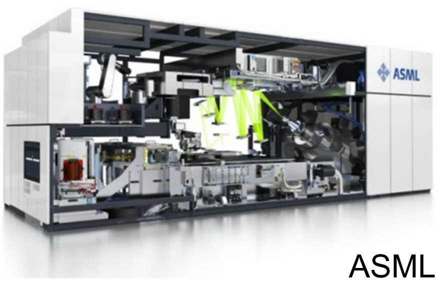
Today: $R \geq 22$ nm (Intel, 2012)



Numerical aperture (NA ~ 0.5–0.6)

- **Larger lenses**
- **Immersion lithography: increases NA by 30–40%**

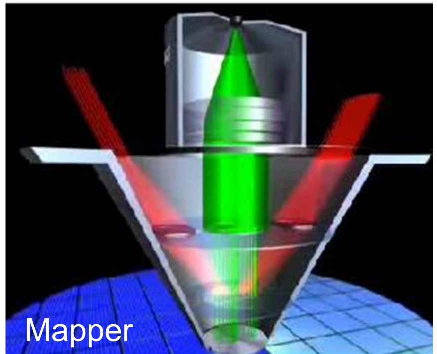
Optical lithography is facing resolution and cost limitations: what are the alternatives?



ASML

Extreme ultraviolet (EUV)

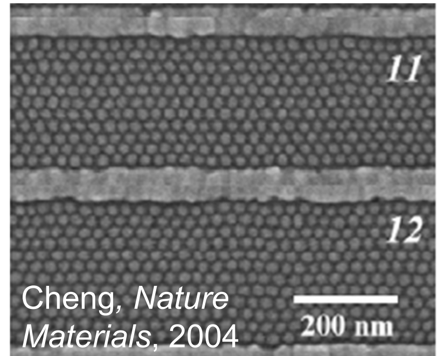
- ~14 nm radiation
- Reflective optics
- ~$100M per tool
- Semiconductor industry-centric



Mapper

Multiple electron beam

Exposure of an e-beam-sensitive resist by multiplexed beams



Cheng, *Nature Materials*, 2004

Directed self-assembly

A mixture (*e.g.* PS/PMMA block copolymer) forms structures, guided by a template

Molecular Imprints

Nanoimprint lithography (NIL)

Mechanical deformation of a polymeric film by a nanopatterned stamp

Nanoscale material manipulation

- There are many methods of giving order and structure to material to achieve a particular function
- Much of what we’ll discuss can be termed “lithography”
- Lithography processes relate to many other manufacturing processes: etch, deposition, growth, doping, polishing, *etc*.
- Examples of applications:
  - Semiconductor circuit geometries ($300B industry)
    - *Established* technology: planar silicon wafers
    - *Emerging* materials: Carbon nanotubes (1D); graphene/MoS_2 (2D)
  - Micro/nano-fluidic devices (*e.g.* lab-on-chip diagnostics, pharmaceutical screening, DNA sequencing, chemical synthesis)
  - Superhydrophobic/superoleophobic surfaces
  - Optical surface engineering: structural color, anti-counterfeiting, diffractive optics
  - Hundreds of others

Nanoscale material manipulation

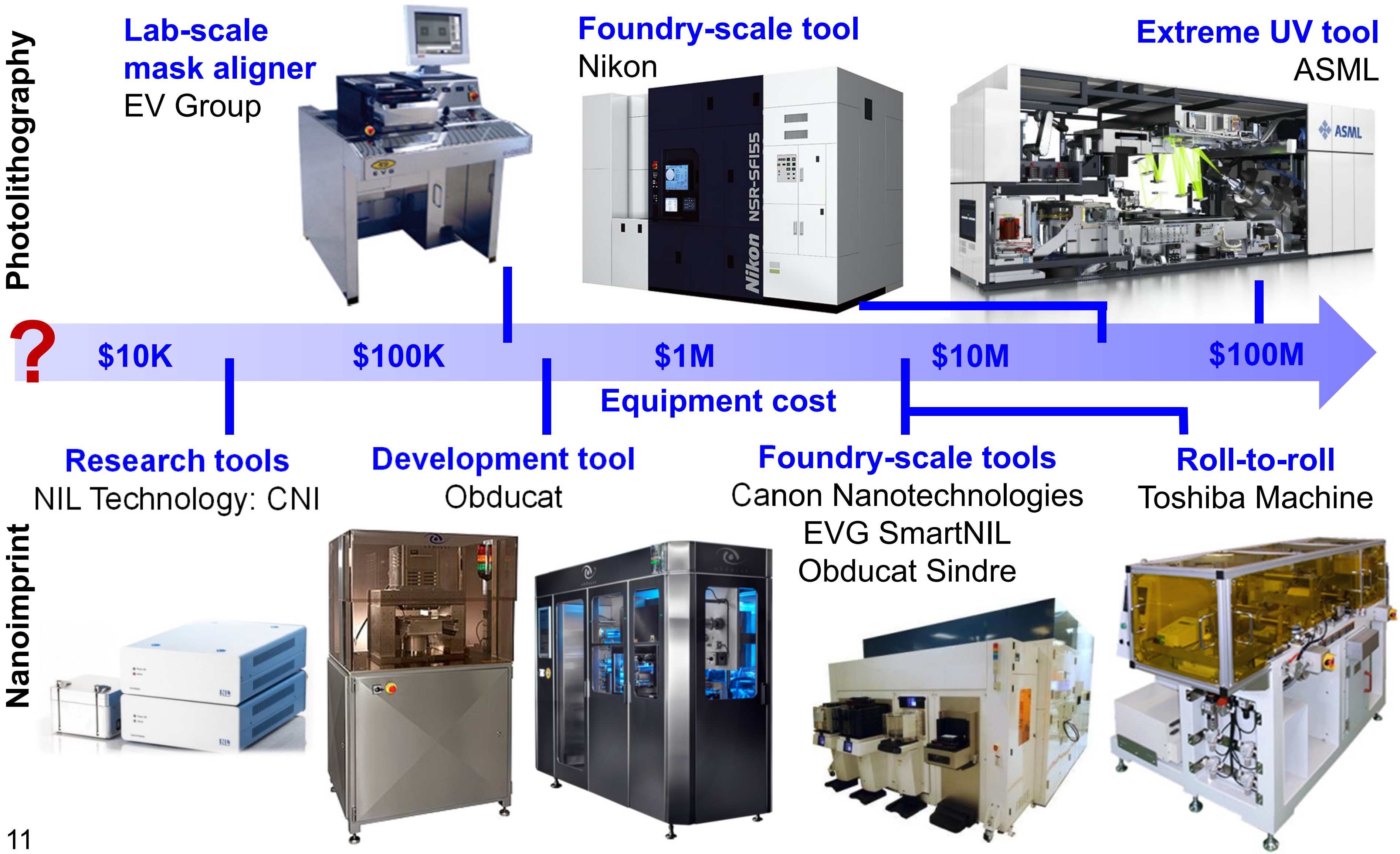
- *Top-down*: take bulk material and selectively remove or deform parts to create patterns – optically, mechanically, with electron beams (analogous to *subtractive* macro-scale manufacturing)
- *Bottom-up*: exploit material properties and reactions to form micro/nanostructures (analagous to *additive* macro-mfg)
  - *Emergent*: may have tight feature size distributions but typically little long-range geometric order
  - *Directed*: more long-range order (e.g. top-down guide structures)
- *Imaging and characterization*: crucial for process control
  - Optical (microscopy, interferometry, scatterometry)
  - Scanning electron microscopy
  - Scanning probe methods (atomic force microscopy, profilometry)

Class activities

- Design and Prototyping project (55%)
- Three simulation mini-projects (36%)
    1. Nanoimprint lithography (contact mechanics)
    2. Photolithography/photopatterning (optical diffraction)
    3. Scanning beam lithography (electron scattering)
- Focused literature review and peer feedback (14%)

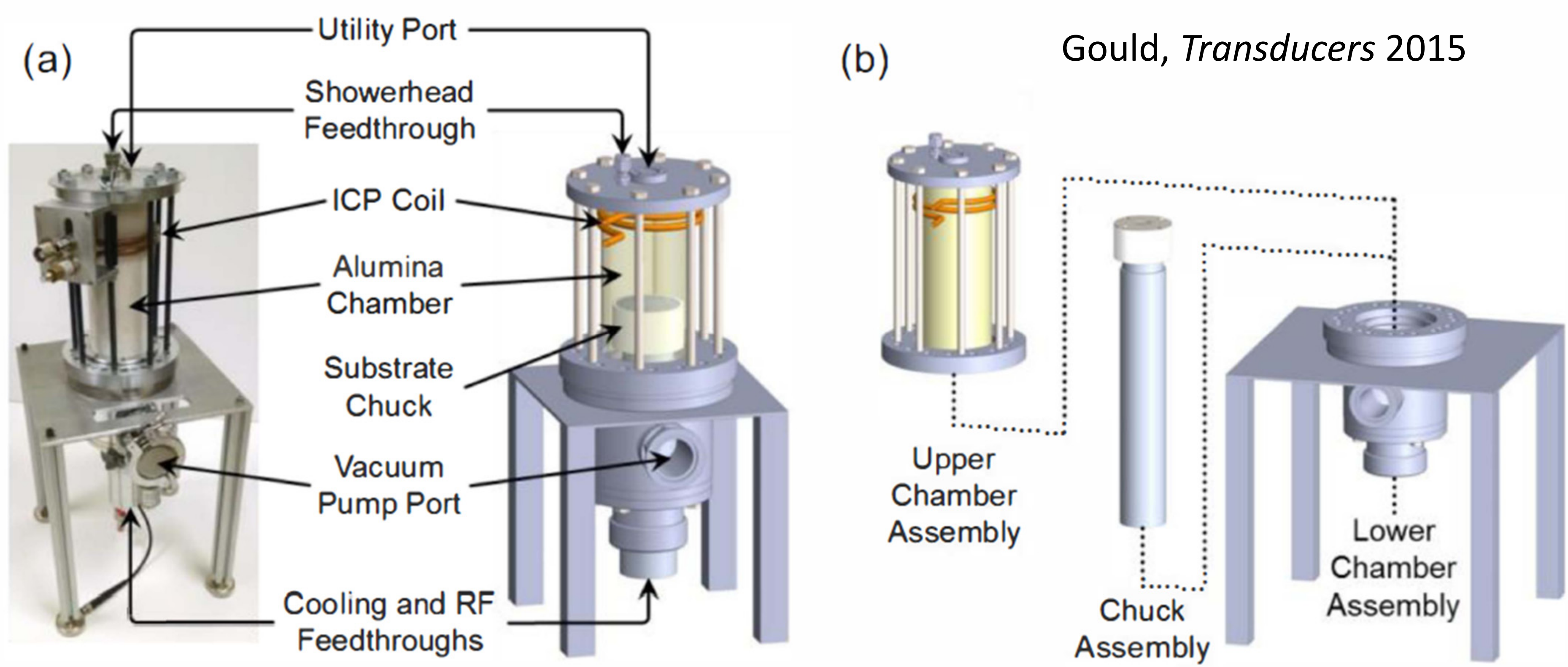
Plus optional problem sets (uncollected, ungraded) for practice of lecture material

Micro and nanomanufacturing equipment costs seem to be quantized on a log scale…



Low-cost hardware: etching

- Deep reactive ion etch, 1” substrates, for ~$32K



Gould, *Transducers* 2015

- cf. basic commercial research-grade systems: single 6-8” wafers, >$500K

Adaptation of existing equipment

- Cellphone as:
  - Virtual reality headset (Google Cardboard)
  - Microscope (Cellscope, Dan Fletcher lab, Berkeley)
  - 3D printer (ONO 3D)
  - Projector (Pizza Hut, past E27 project)
  - …A micro/nano-lithography system?
  - …A micro/nano-scale 3D imaging system?

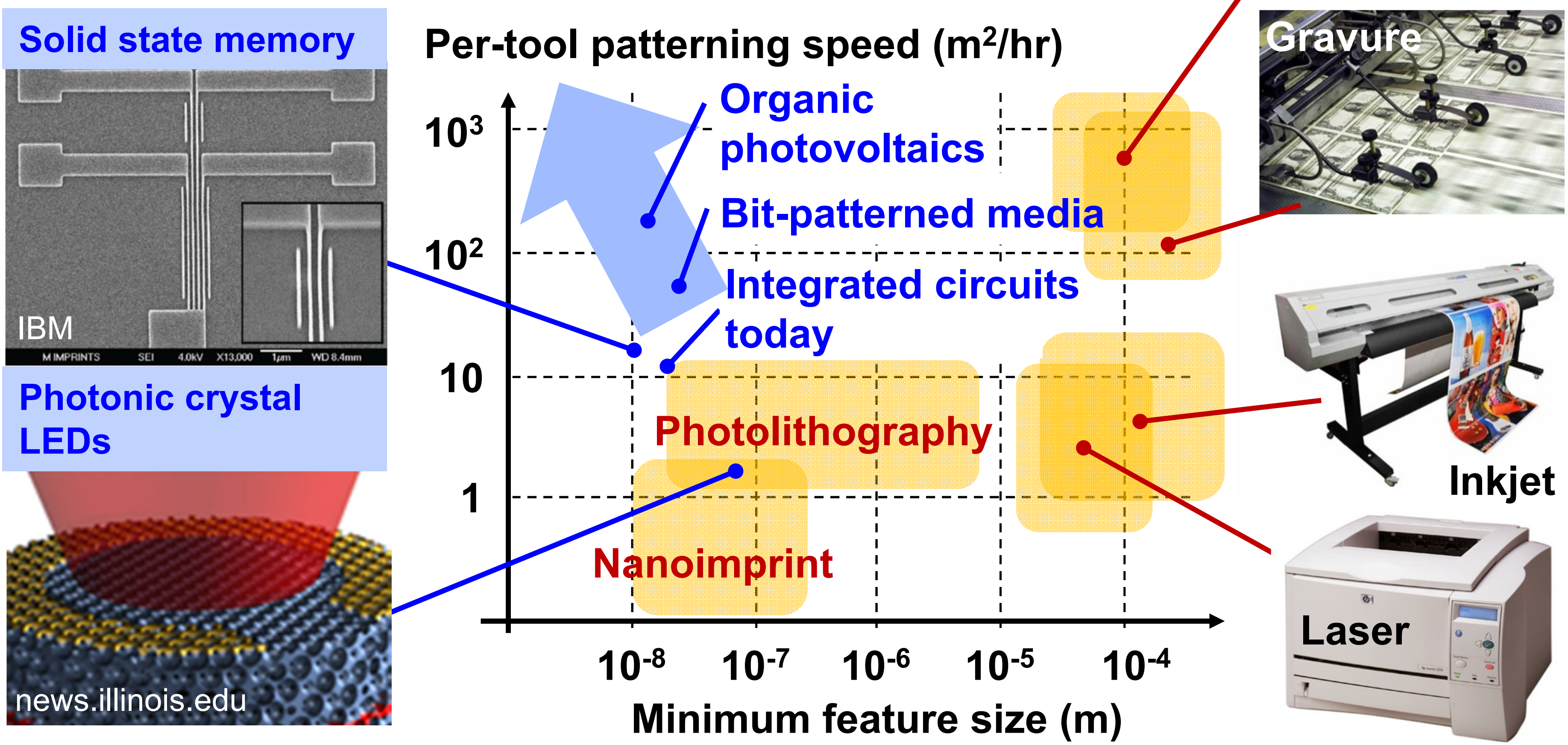
http://www.3ders.org/articles/20120605-uc-berkeley-showcases-cellscope-with-3d-printed-iphone-stand.html
https://www.ono3d.net/
https://vr.google.com/cardboard/

Design and Prototyping project

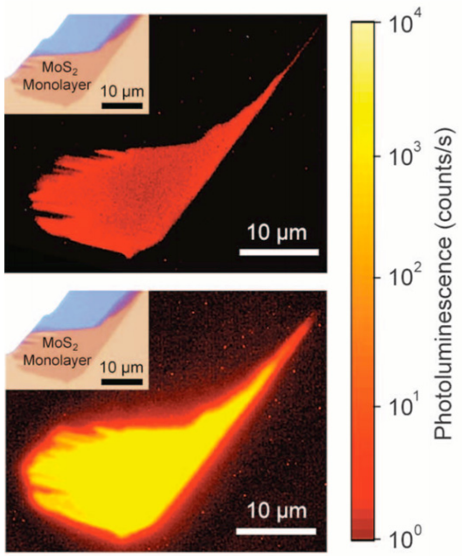
- Objective: conceive, design and prototype a piece of extremely low-cost (say <$1000) apparatus that usefully *manuipulates, images or characterizes material* at the micro- (say < 100 μm) or nano- (< 100 nm) scales.
- Must address a demonstrable need in research, teaching or outreach.
- Teams of about 3-5
- Full access to Jacobs facilities – just get trained
- Free to use any other facilities to which you have or can secure access
- Design it to be easy to disseminate your design over the web, so others can produce and use your tool (“open-source” hardware)

Emerging technologies demand patterning of smaller features across larger areas

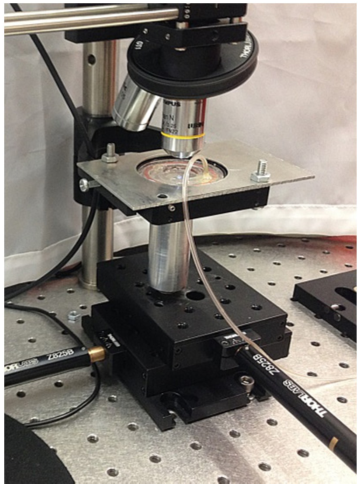
- Many technologies for energy generation and conservation rely on nanopatterning
- Developing leadership in nanolithography is a key opportunity for the US economy

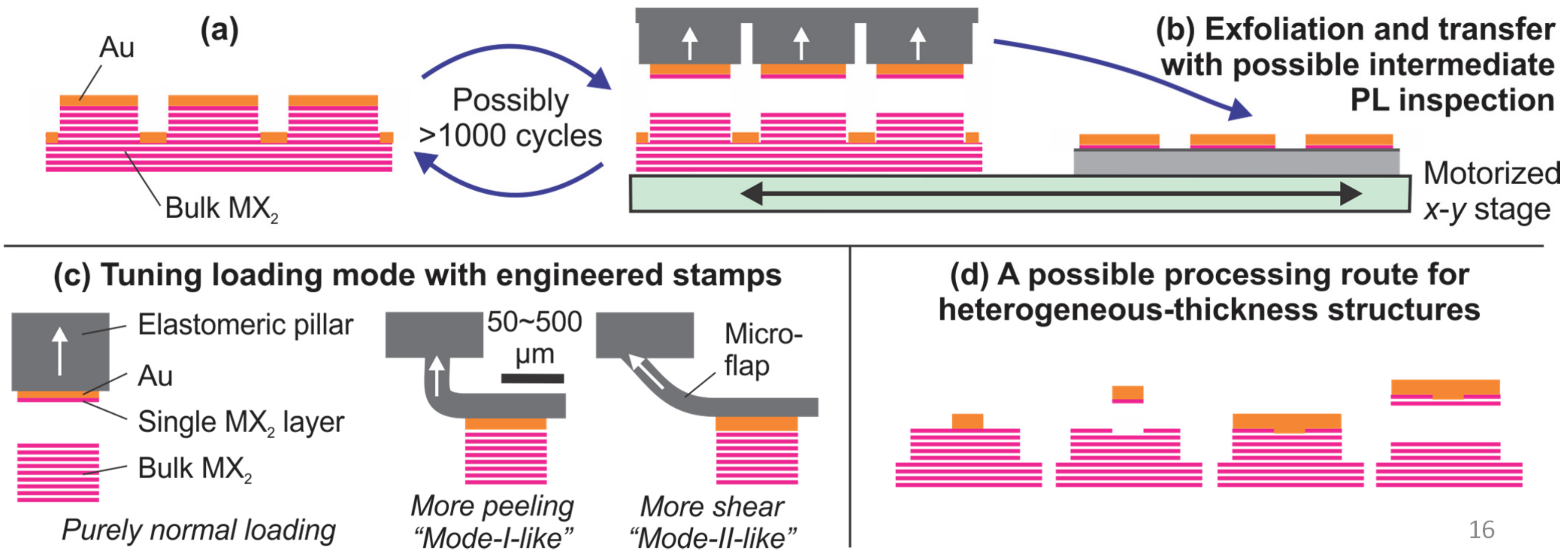


Area in need of hardware innovation: 2D material handling

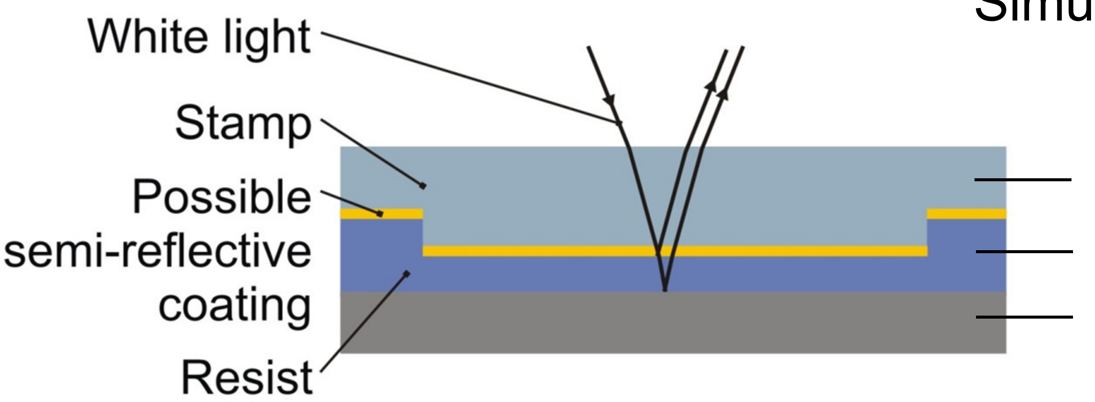


- Need to isolate and identify single atomic layers from bulk crystals – automate the "sticky tape" method.
- Optical imaging is preferred mode of layer thickness and defectivity identification – can it be automated?



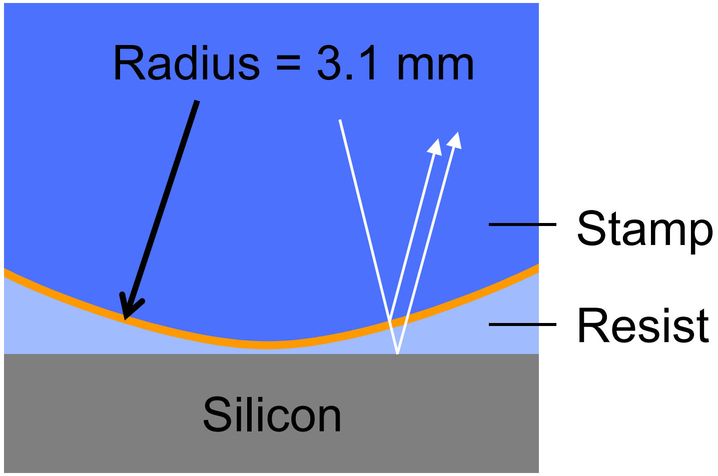


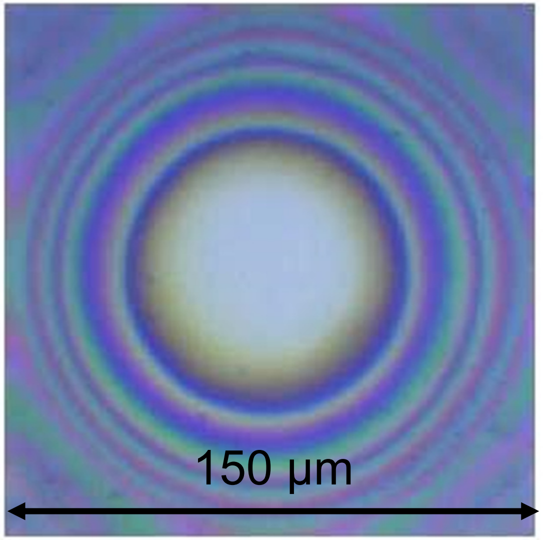
Real-time observation of evolving RLT could accelerate material/stamp characterisation

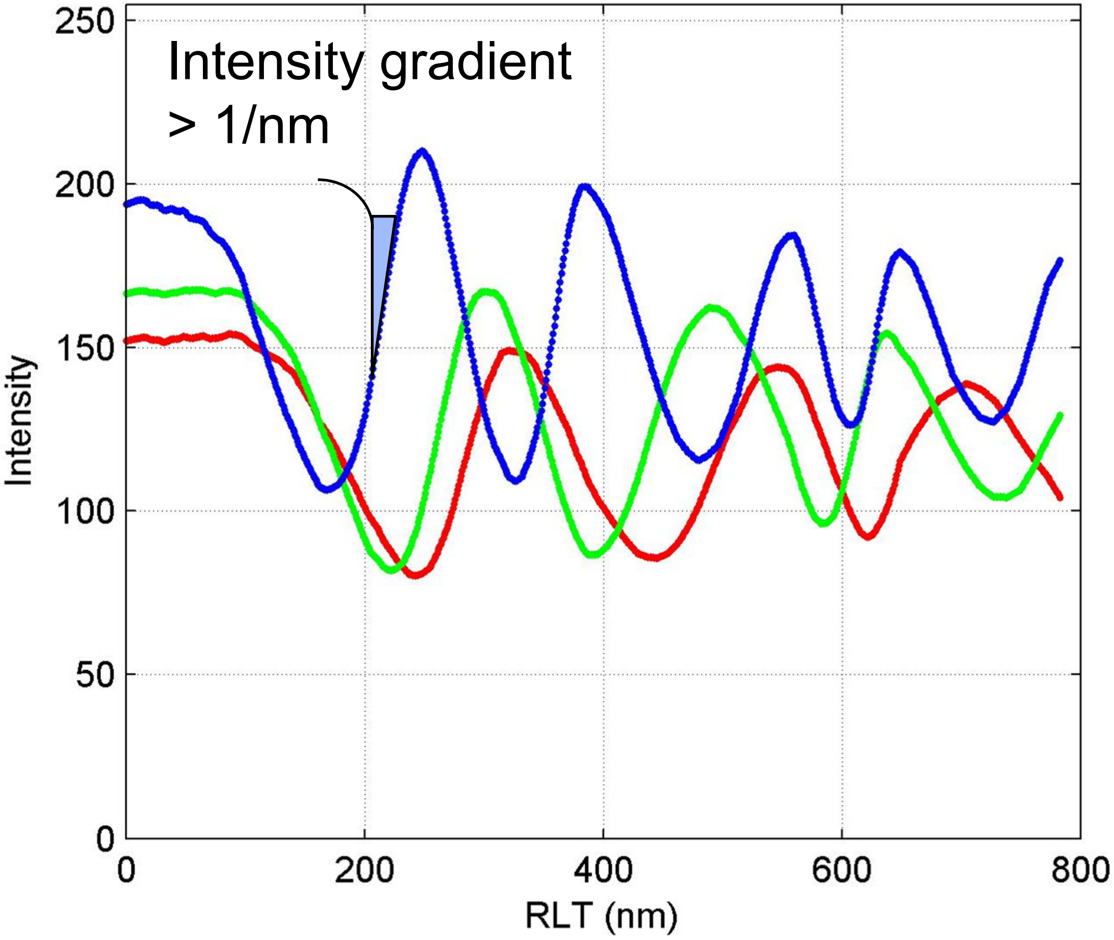


Simulations

RLT–colour relationships are calibrated using a known stamp topography



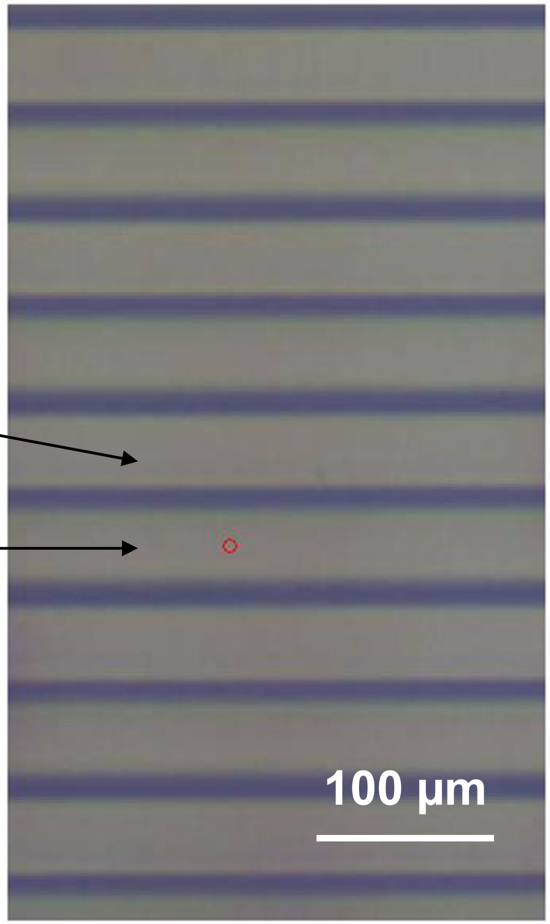


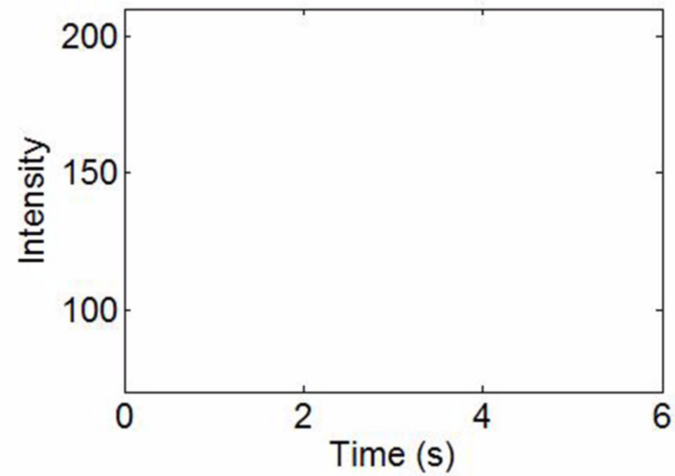


Videos of the imprinting process allow the temporal response of resist to be extracted

Stamp cavity

Residual layer region

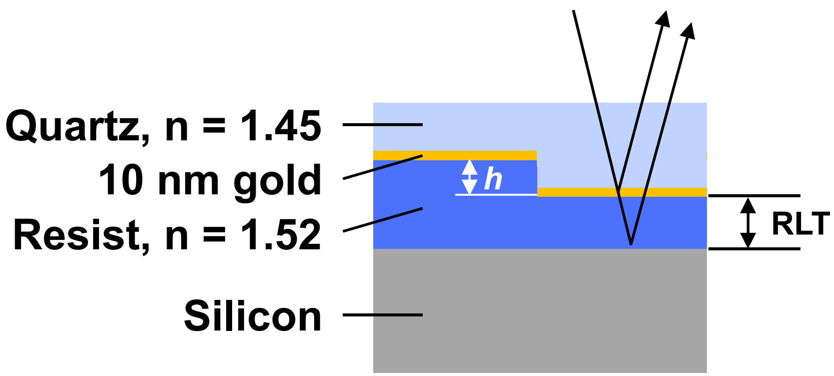


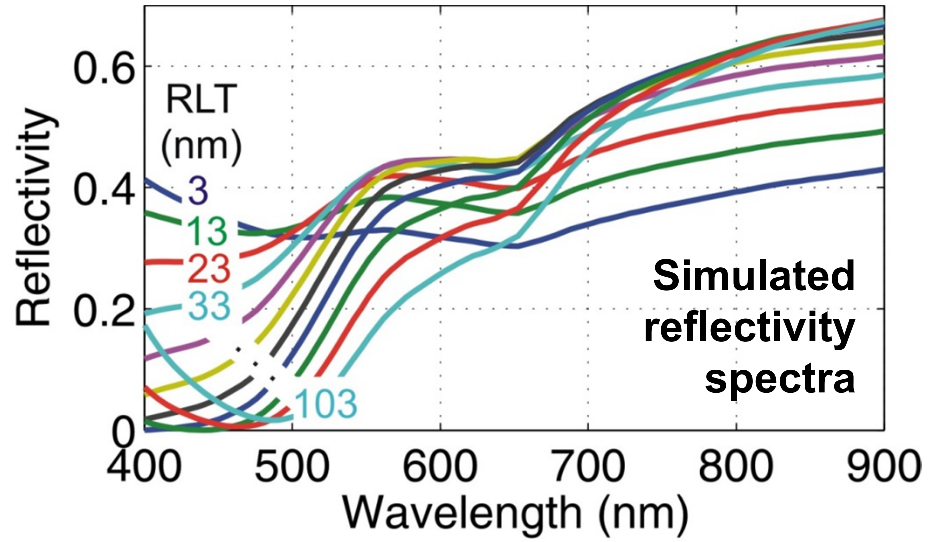


- **Material: MRT mr-UVCur-21**
- **Stamp-average pressure 20 kPa**

If features are sub-wavelength, plasmonic effects could enhance RLT detection

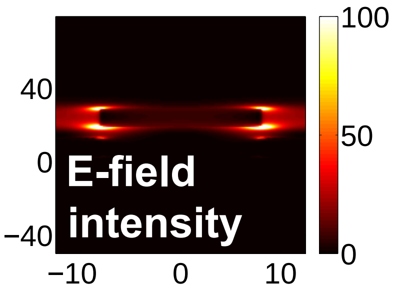
Large features

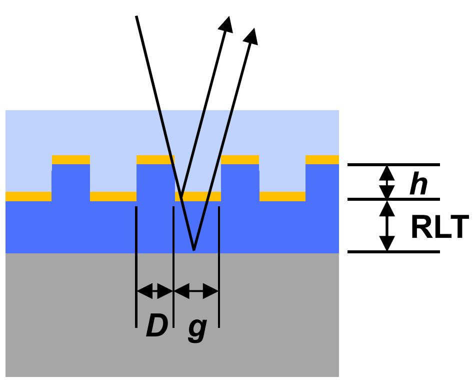


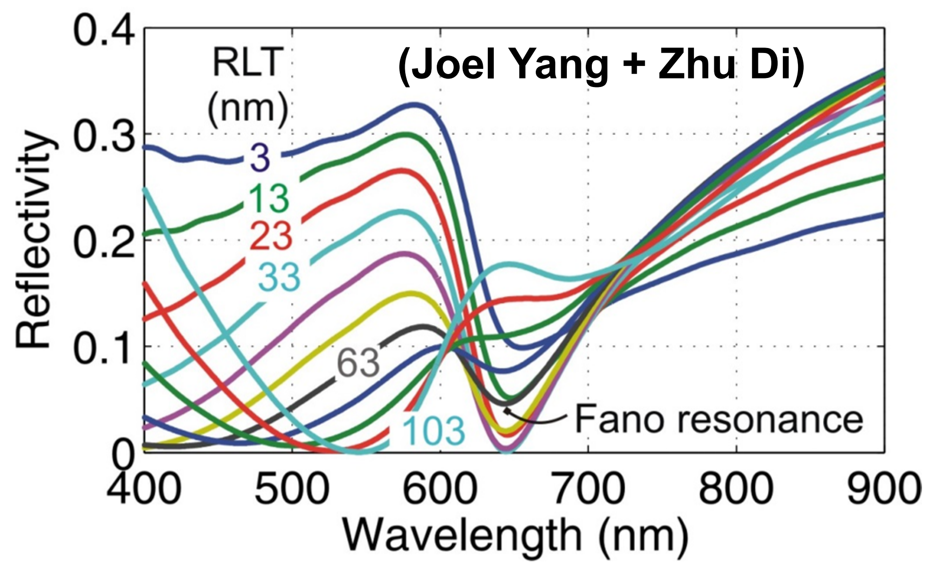


25 nm-pitch dot array

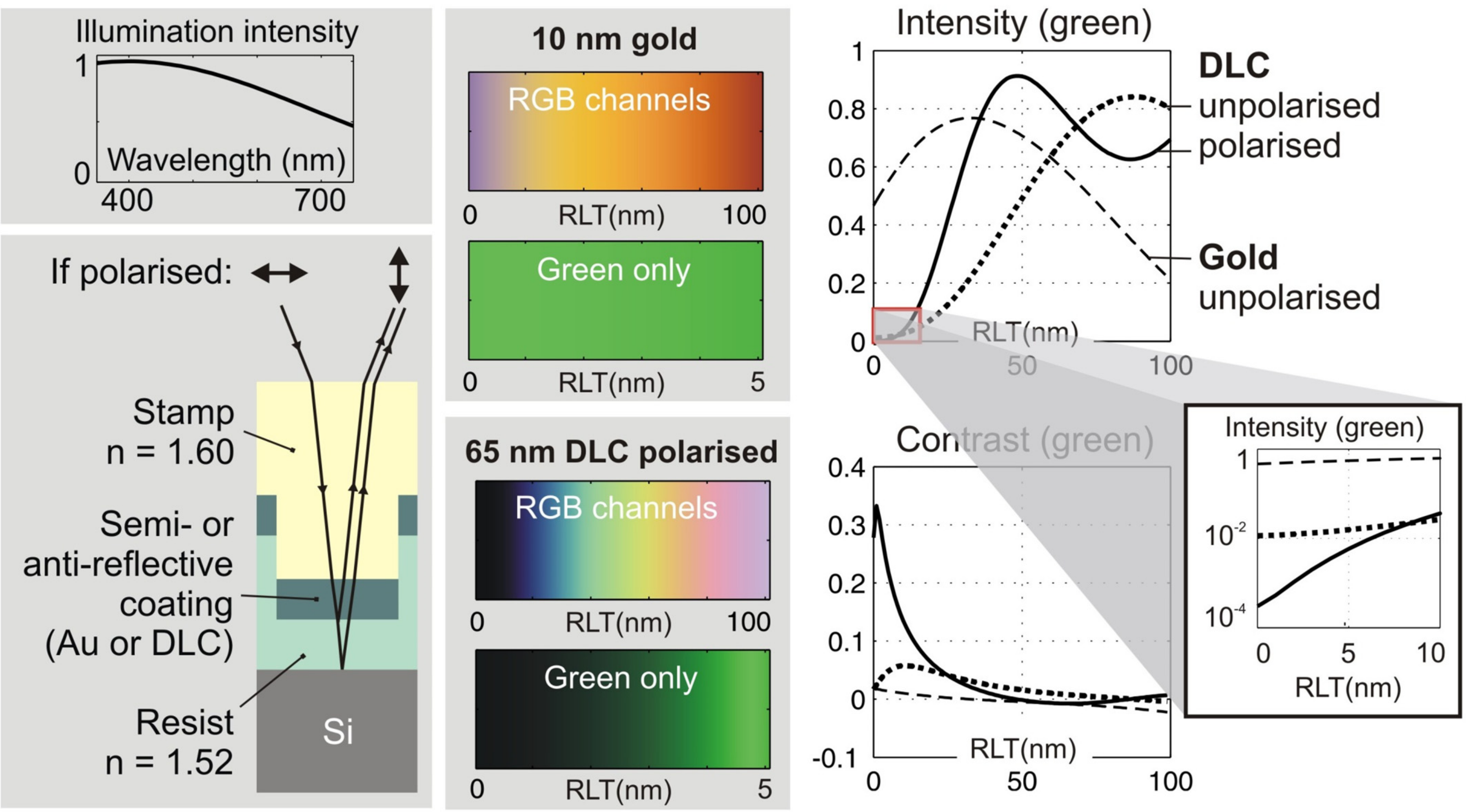
h = *D* = 16 nm
g = 9 nm







An anti-reflective stamp coating and light polarisation could enhance RLT contrast



Contrast: relative change in intensity for a 1 nm change in RLT about a given RLT

Substrate-enhanced ellipsometric contrast: Ausserré, *Optics Express*, **15** 8329 (2007)