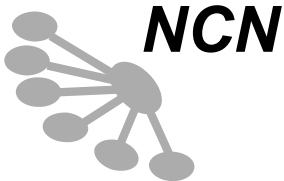


Purdue Nanotechnology 101 Series

CMOS Nanotechnology 101

Mark Lundstrom
Purdue University
Network for Computational Nanotechnology
West Lafayette, IN USA

- 1) Introduction
- 2) CMOS Tutorial
- 3) CMOS Today
- 4) Summary



www.nanohub.org

PURDUE
UNIVERSITY

1. Introduction: the scale of things

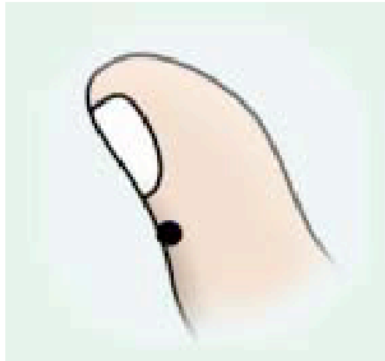


Billions of nanometers

A two meter tall male is two billion nanometers.

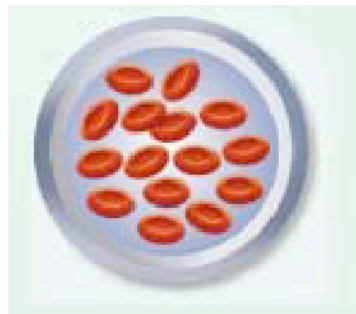
A million nanometers

The pinhead sized patch of this thumb is a million nanometers across.



Nanometers

Ten shoulder-to-shoulder hydrogen atoms span 1 nanometer. DNA molecules are about 2.5 nanometers wide.



Thousands of nanometers

Biological cells have diameters in the range of thousands of nanometers.

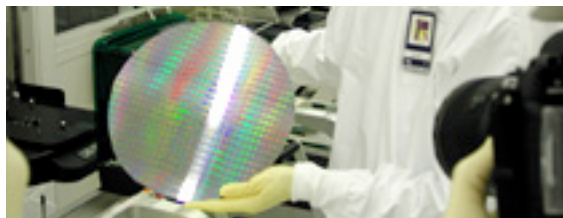
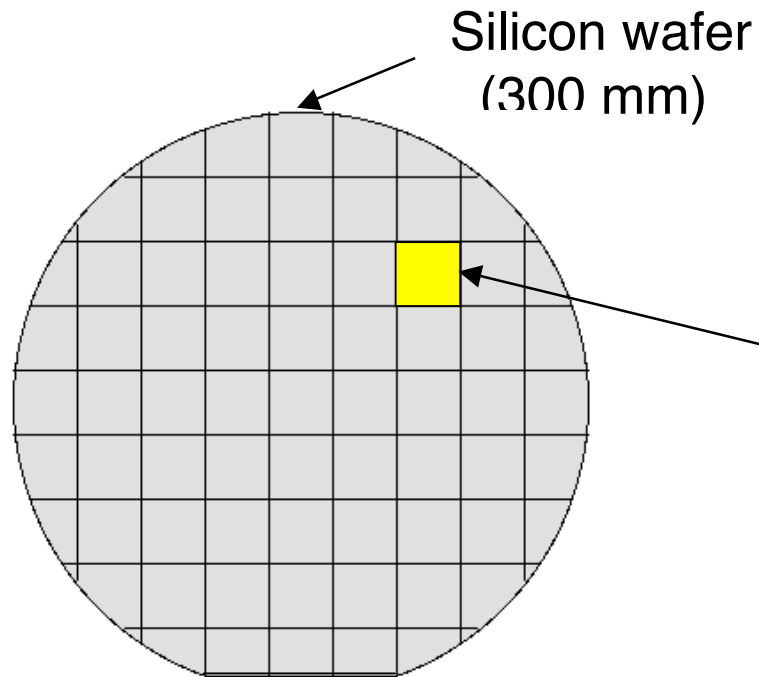


Less than a nanometers

Individual atoms are up to a few tenths of a nanometer, in diameter.

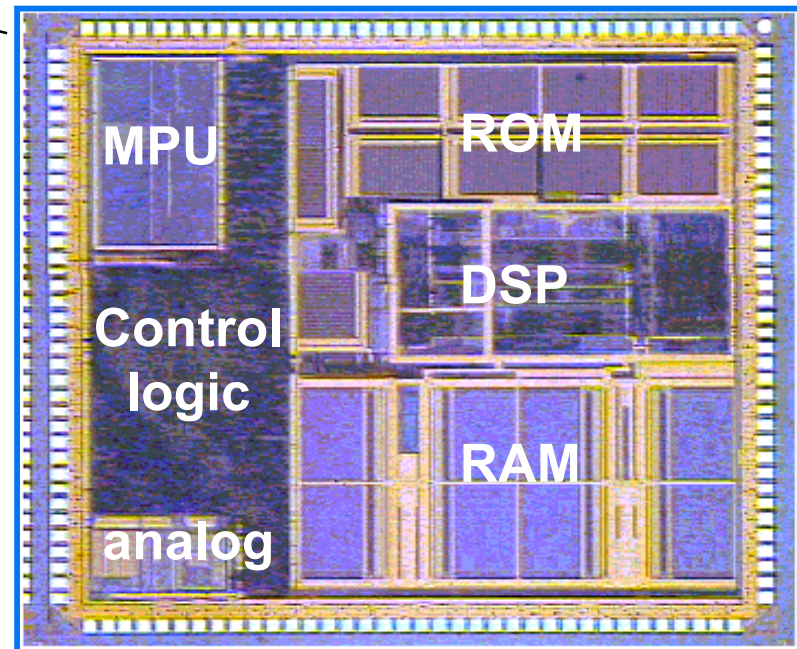
(from Prof. Mildred Dresselhaus, MIT)

1. Introduction: **microelectronics**



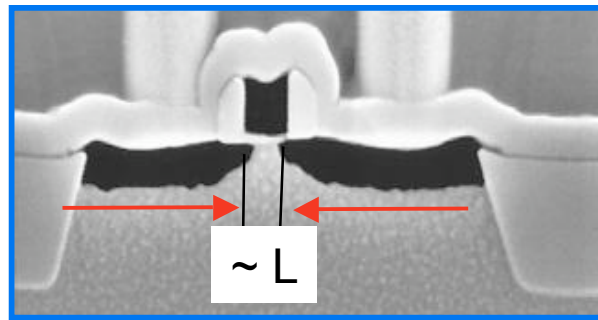
Intel

Silicon "chip"
(~ 2 cm x 2 cm)



TI cell phone chip

1. Introduction: transistors



Each technology generation:

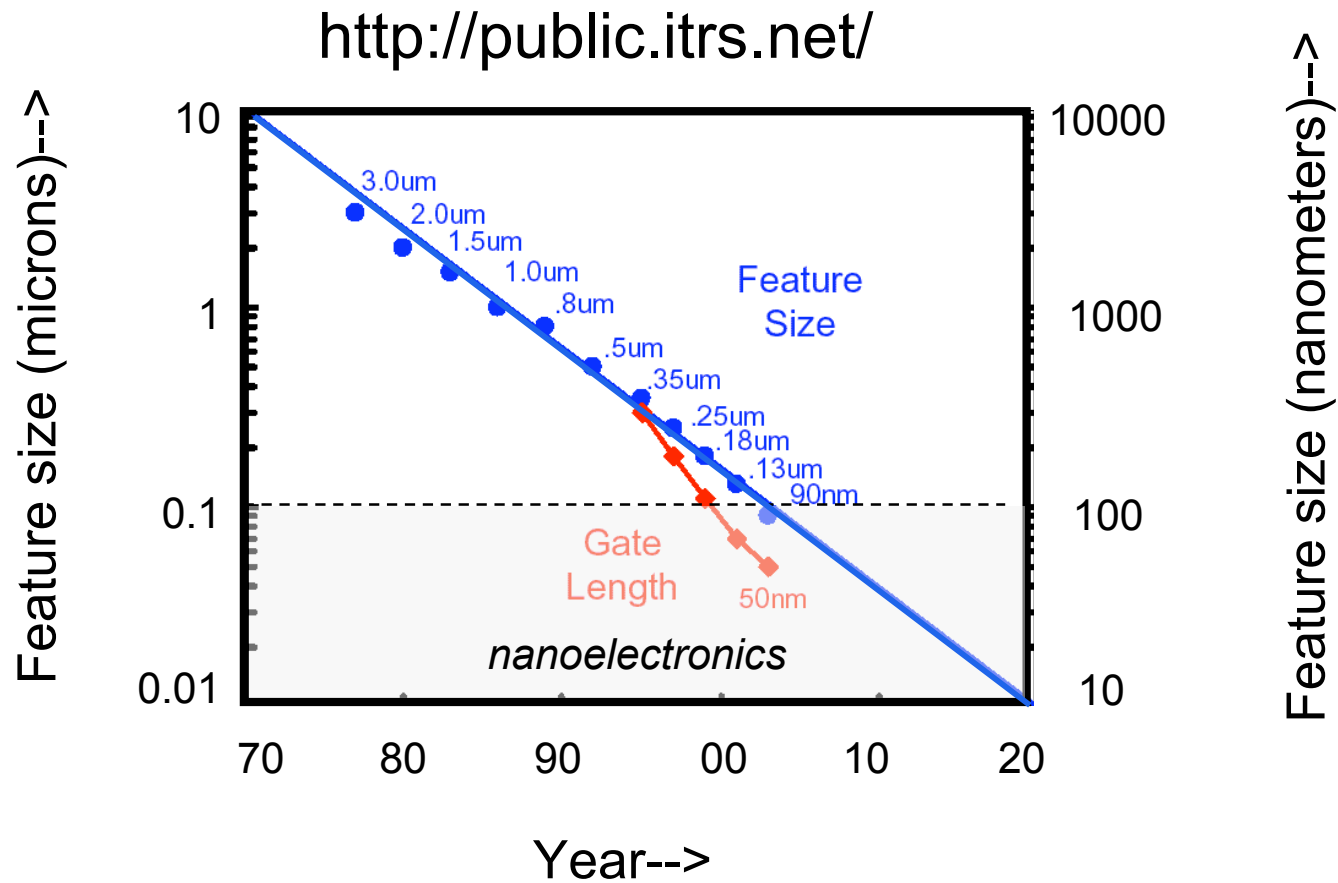
(scaling)

$$L \rightarrow L/\sqrt{2} \quad A \rightarrow A/2$$

Number of transistors per chip doubles

(Moore's Law)

1. Introduction: Moore's Law and the ITRS



(L = 6 nm (IBM, 2002)
L = 5 nm (NEC, 2003))

1. Introduction

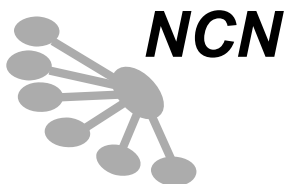
The promise of (bottom-up) nanoelectronics.....

- *understanding devices at the molecular scale*
- *new tools for metrology*
- *new materials*
- *unit processes for directed self-assembly*
- *new devices for new applications*
- *new architectures for ultra-dense systems*
- *terascale electronics*

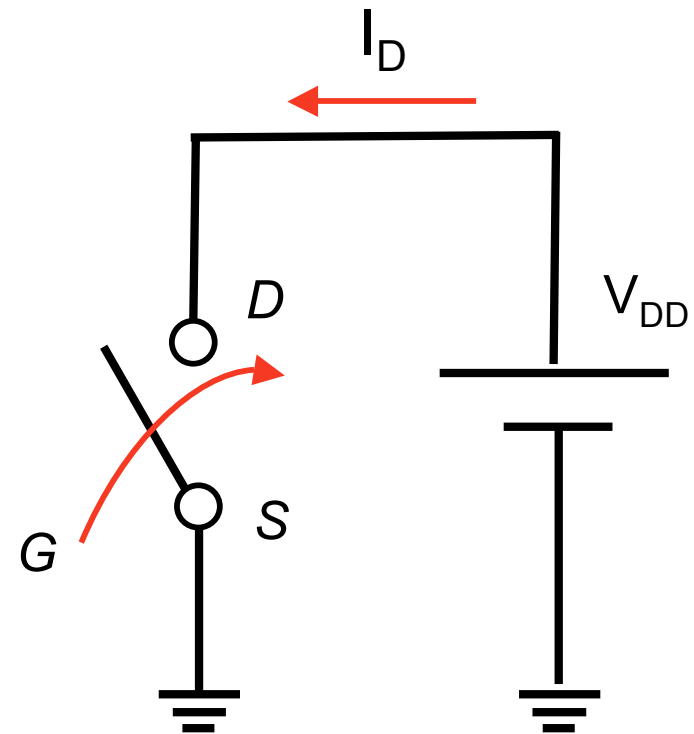
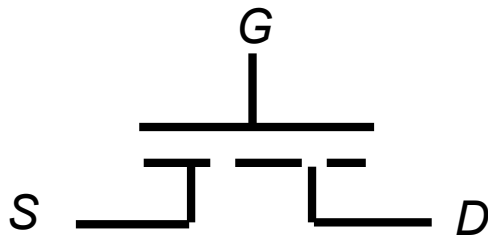
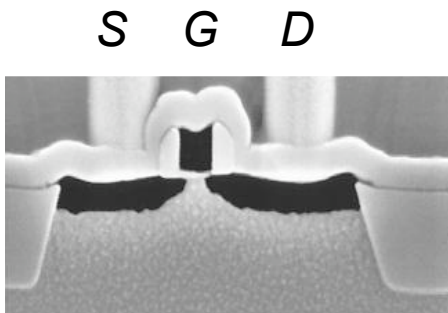
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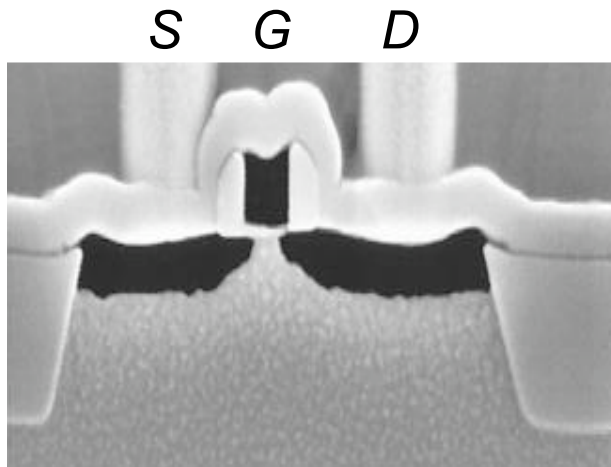
2. CMOS Tutorial: MOSFETs



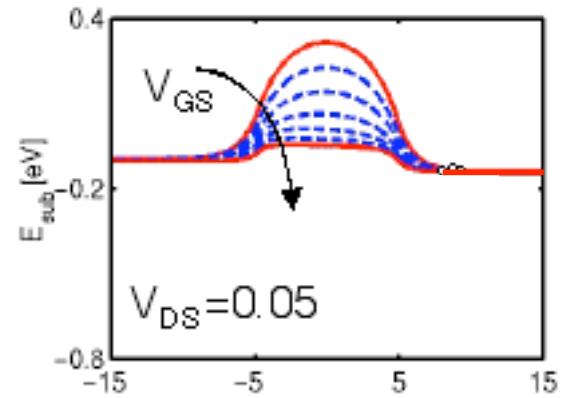
$V_G > V_T: I_D \rightarrow \infty$ “on-current”

$V_G < V_T: I_D = 0$ “off-current”

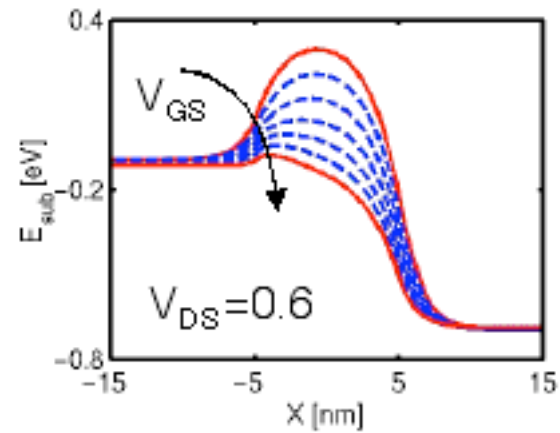
2. CMOS Tutorial: MOSFETs



electron energy vs. position

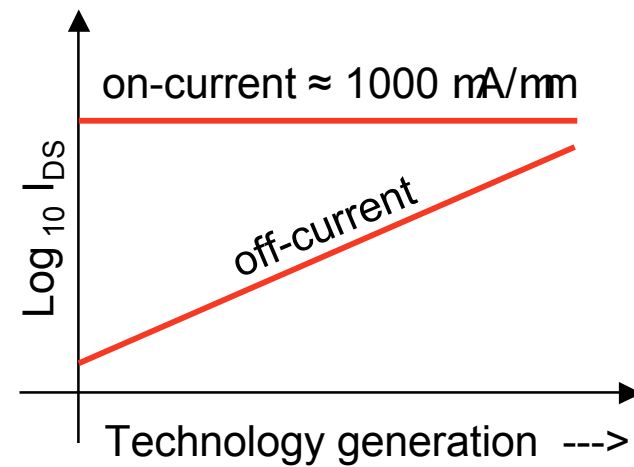
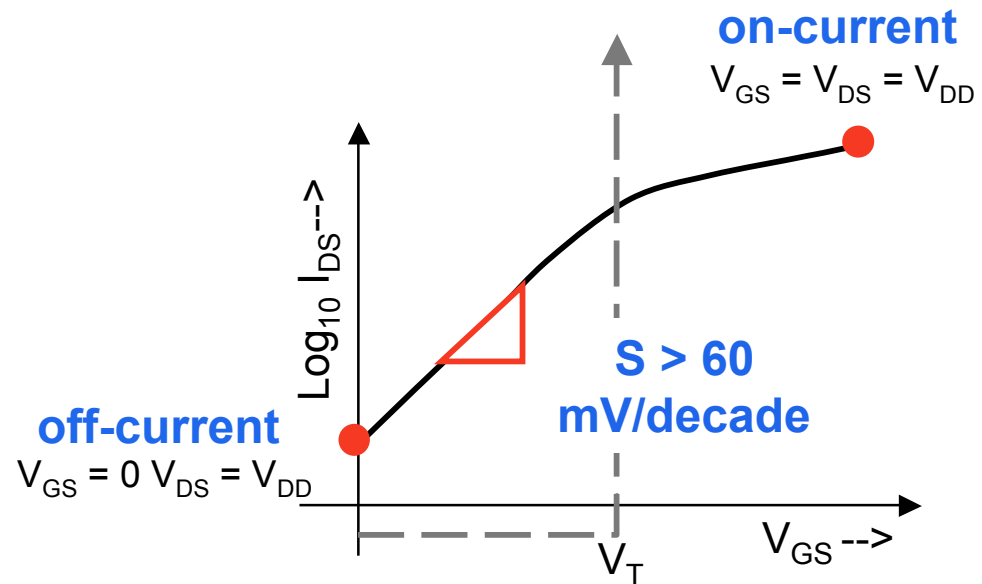
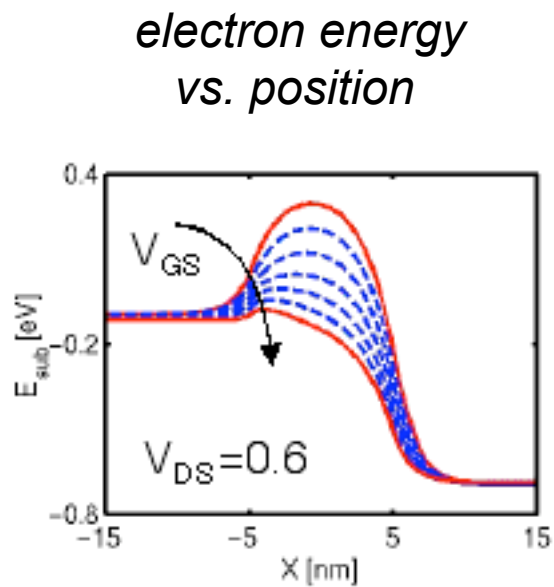


$V_{\text{D}} \approx 0\text{V}$

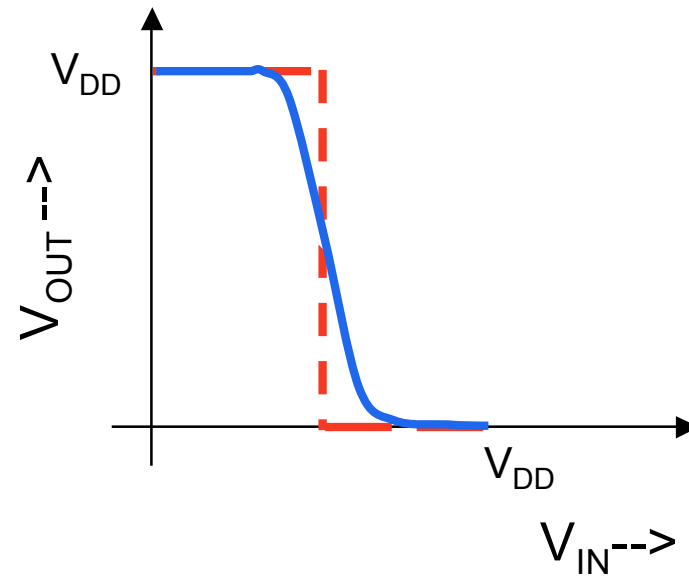
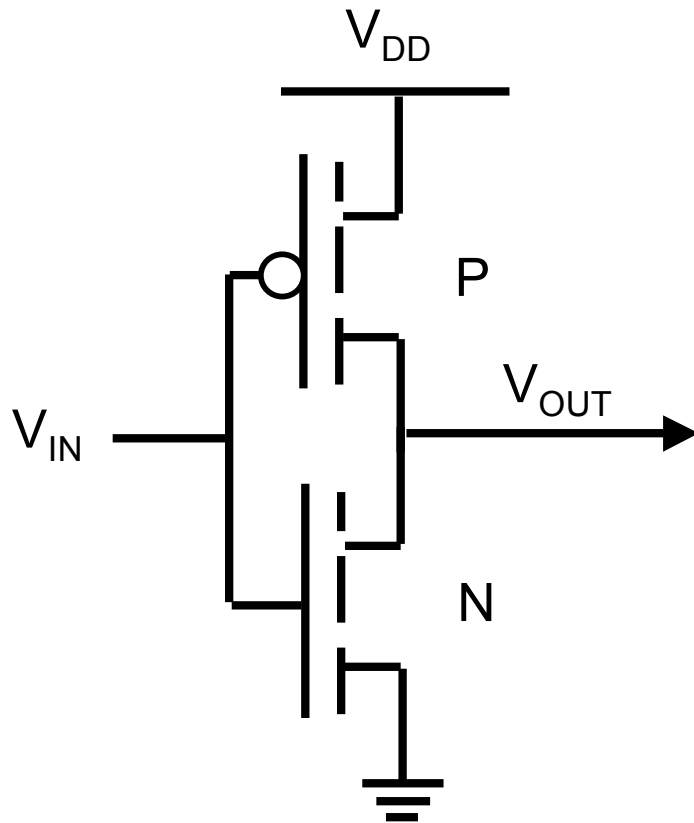


$V_{\text{D}} = V_{\text{DD}}$

2. CMOS Tutorial: MOSFETs

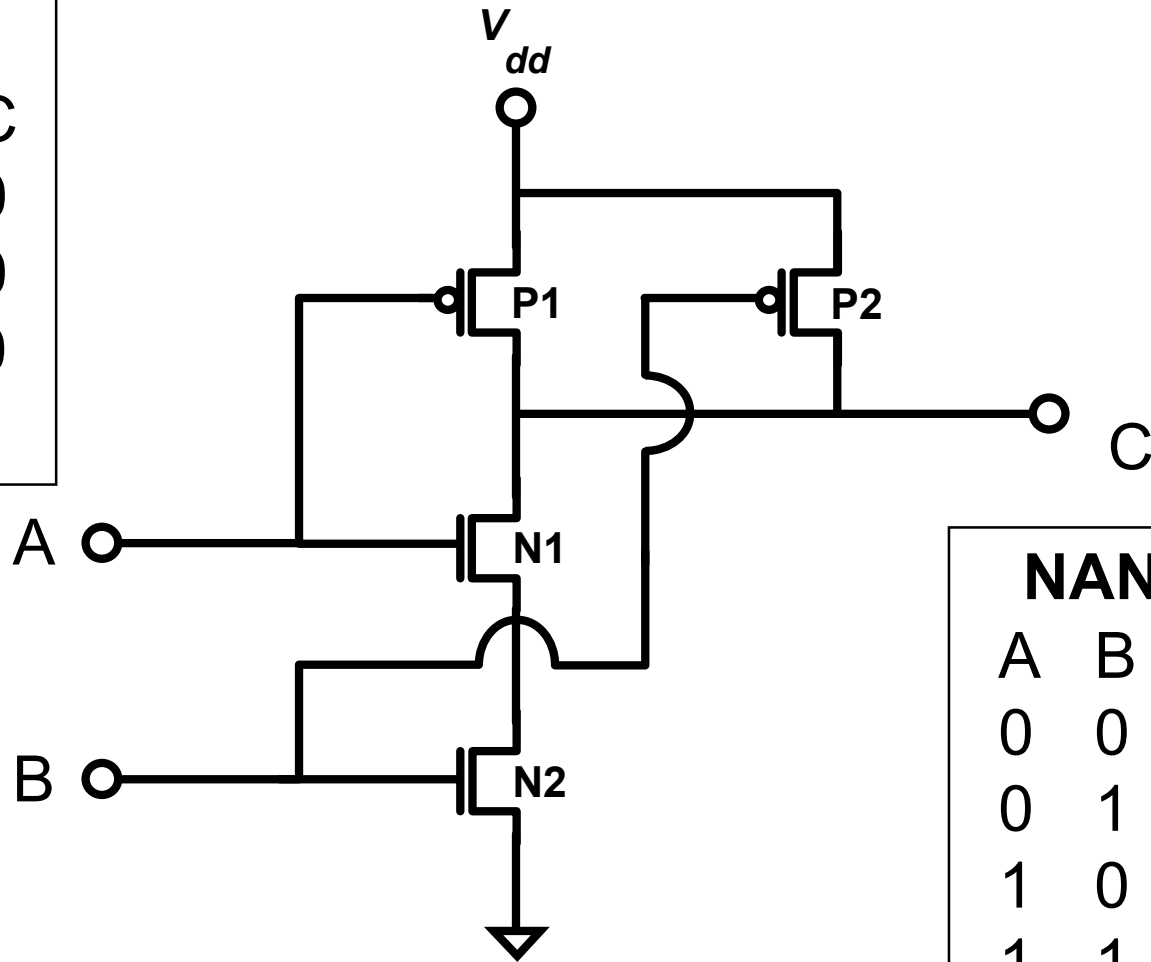


2. CMOS Tutorial: [circuits](#)



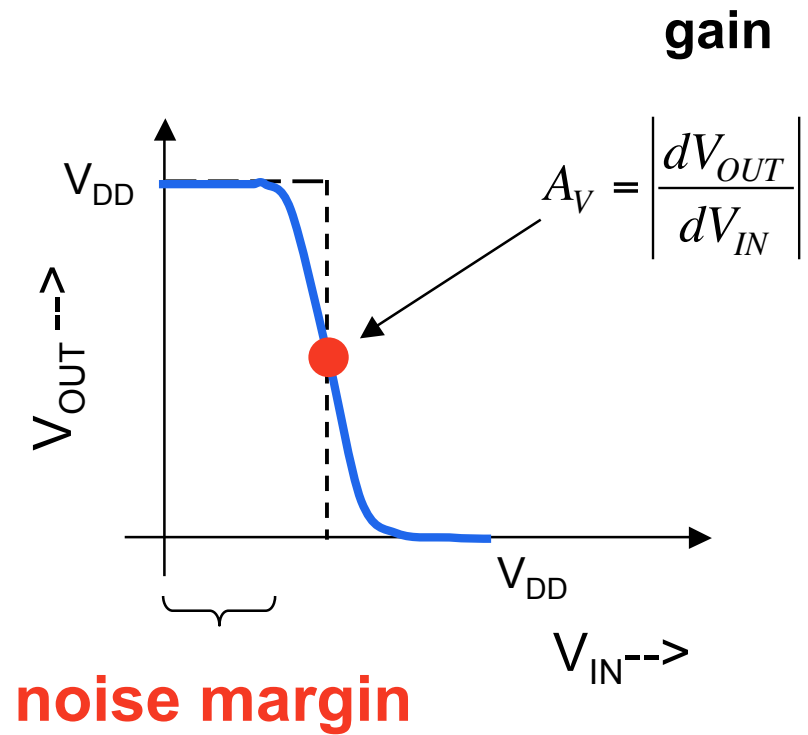
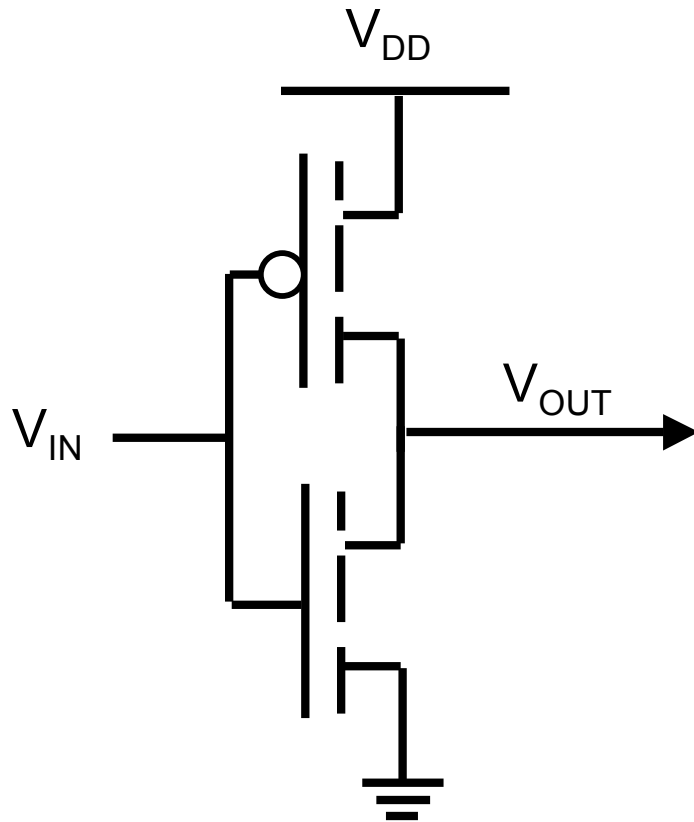
2. CMOS Tutorial: Two input NAND gate

AND		
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



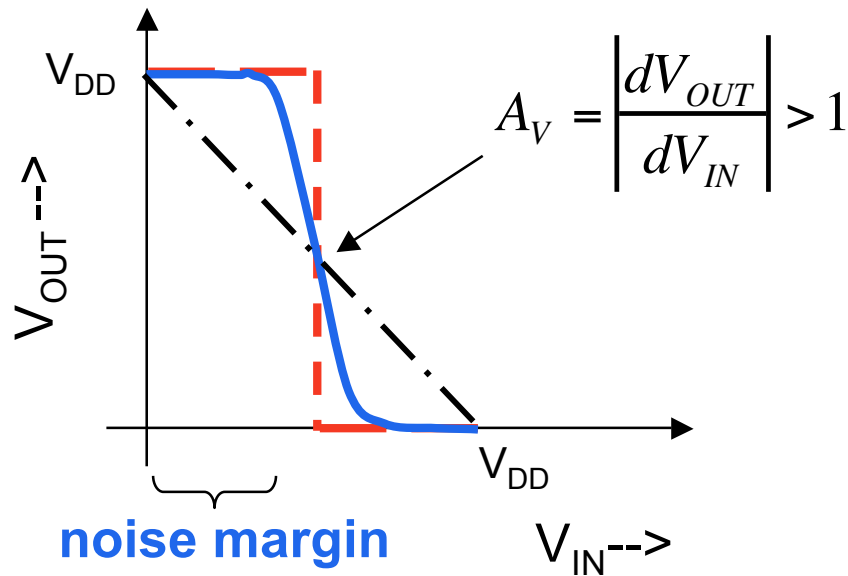
NAND		
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

2. CMOS Tutorial: [circuits](#)



2. CMOS Tutorial: gain

gain restores signal levels



$$V_{DD}|_{\min} = 2 \ln(2) (k_B T / q)$$

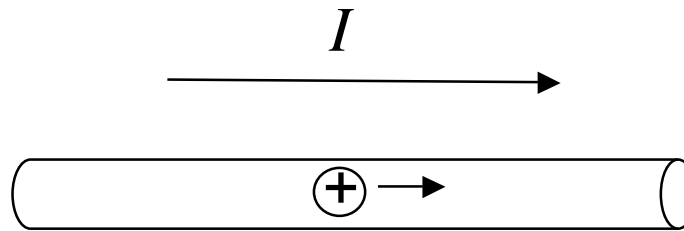
$$E_S = \frac{1}{2} C V_{DD}^2 = Q \frac{V_{DD}}{2}$$

$$E_S|_{\min} = k_B T \ln(2) \approx 3 \times 10^{-21} \text{ J}$$

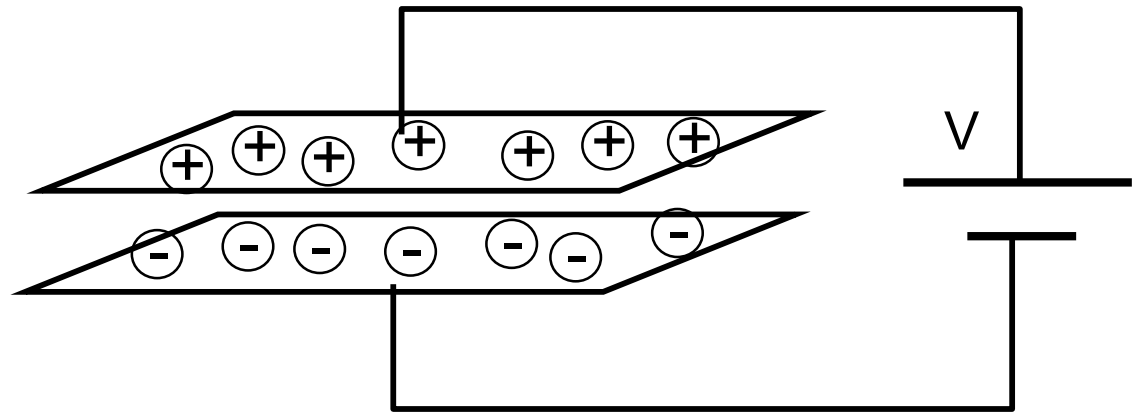
90 nm CMOS technology operates at $\sim 35,000 k_B T \ln(2)$

2. CMOS Technology: device speed

$$I = \frac{Q}{\tau}$$

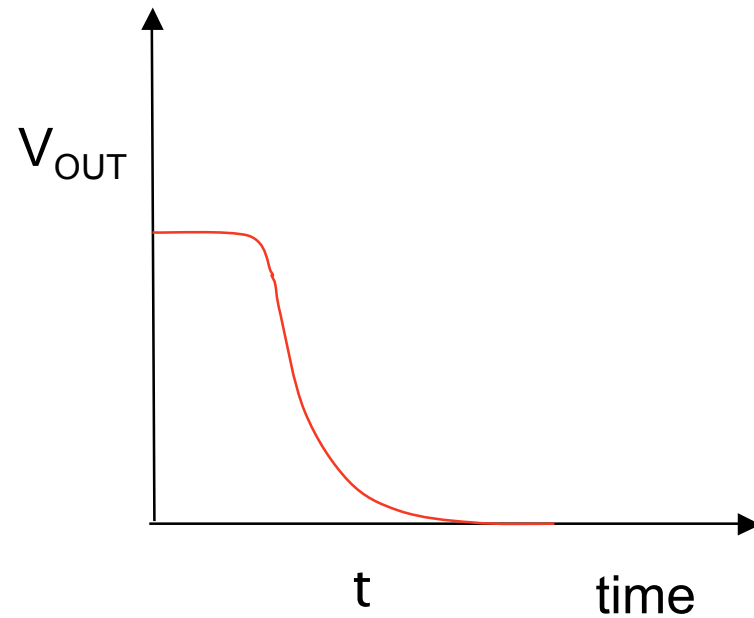
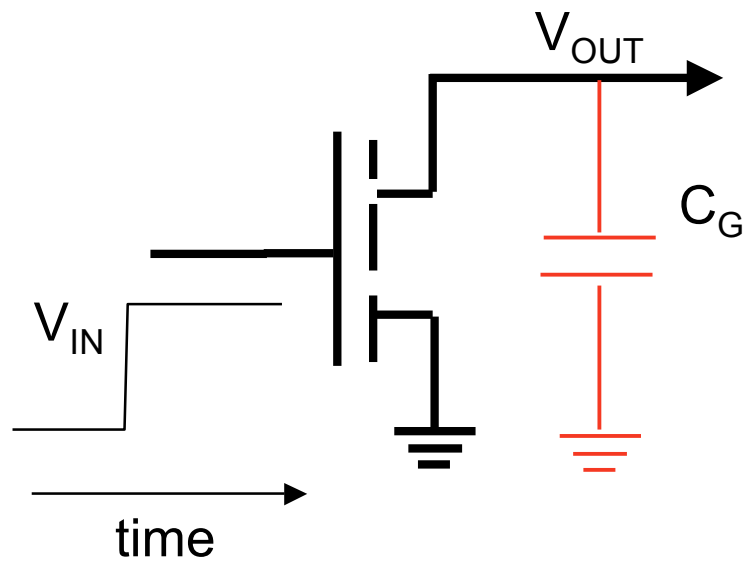


$$Q = CV$$



$$C = \frac{\epsilon A}{d} \text{ farads}$$

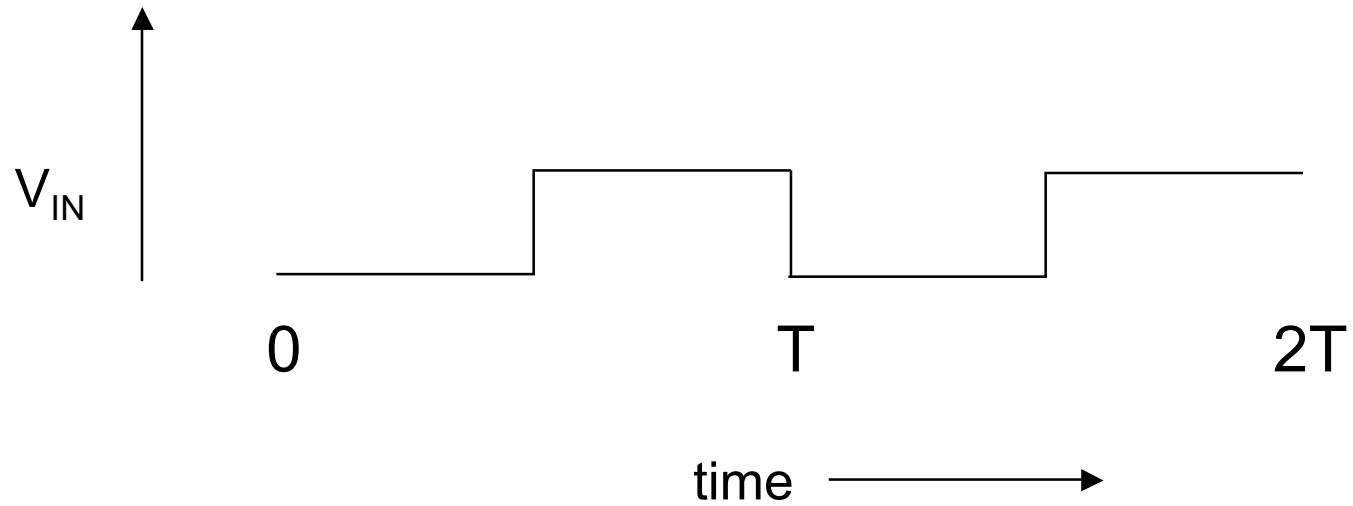
2. CMOS Technology: device speed



$$\tau = \frac{C_G V_{DD}}{I_D(on)} \approx \frac{L}{v} \approx 1 \text{ ps}$$

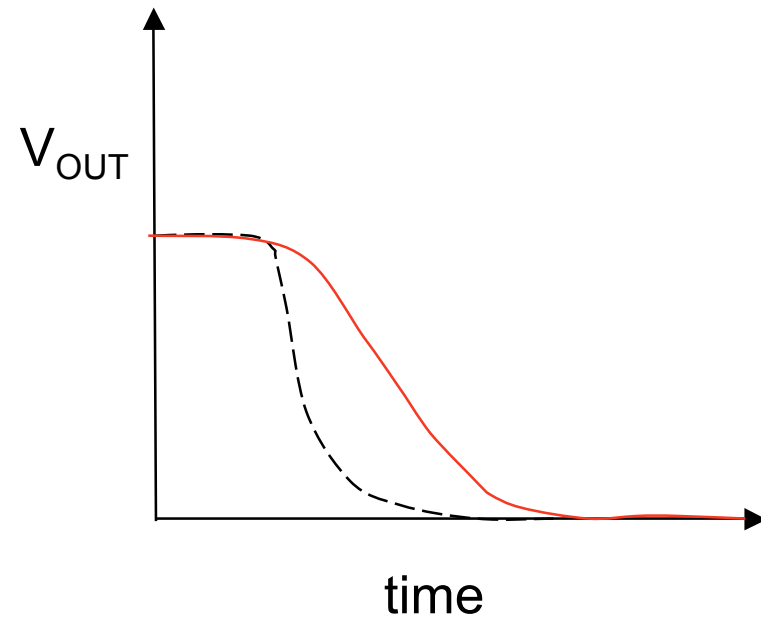
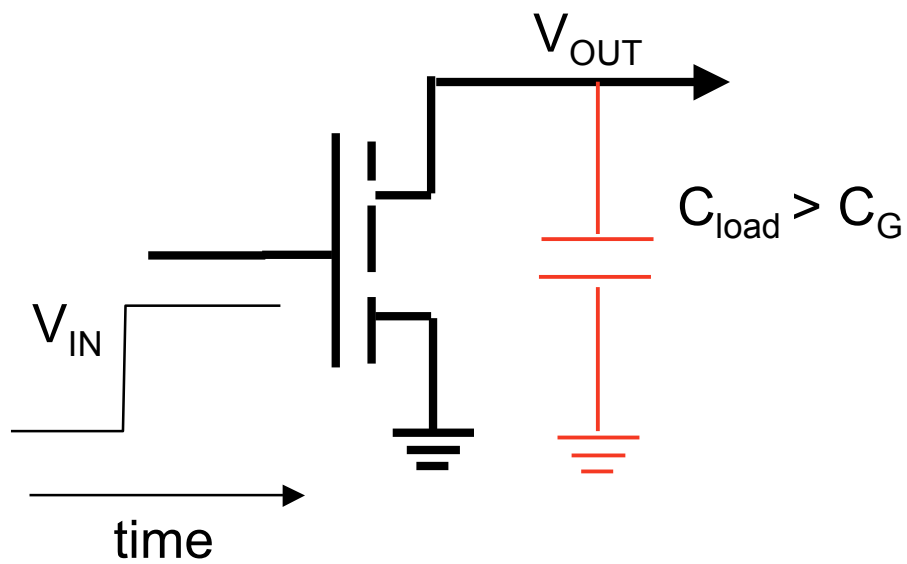
(90 nm technology node) 16

2. CMOS Technology: device speed



$$f = \frac{1}{T} \approx \frac{1}{2 \text{ ps}} = 500 \text{ GHz}$$

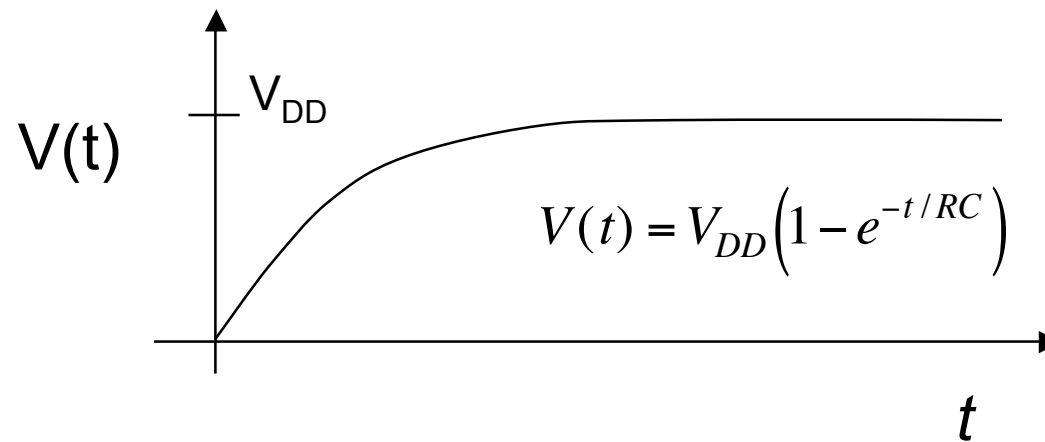
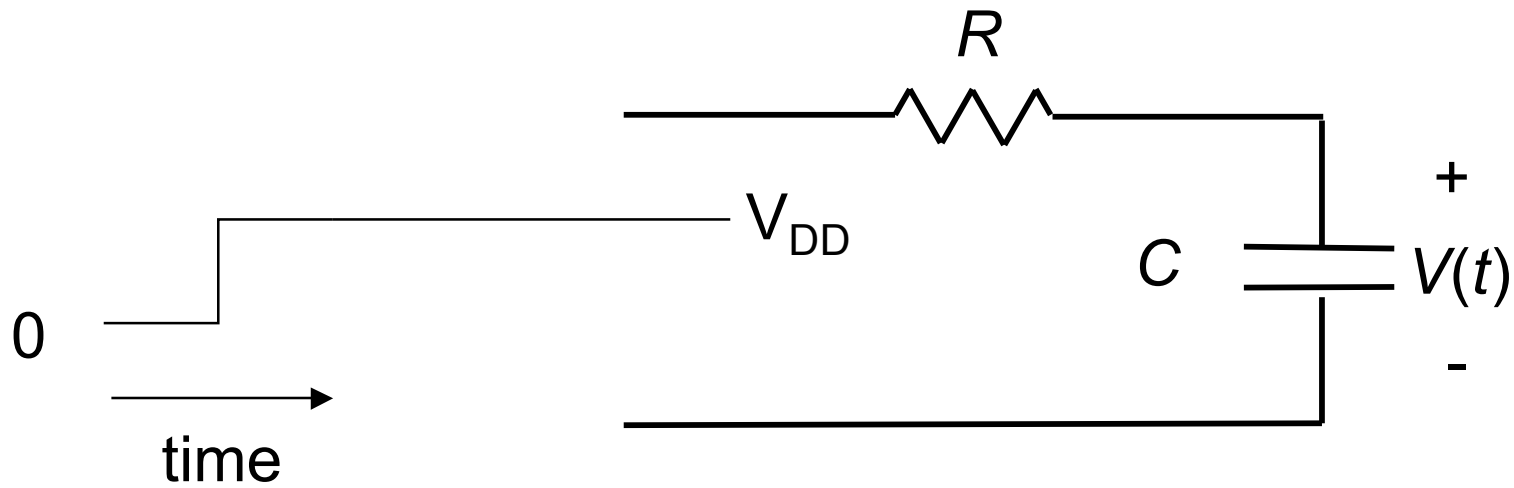
2. CMOS Tutorial: circuit speed



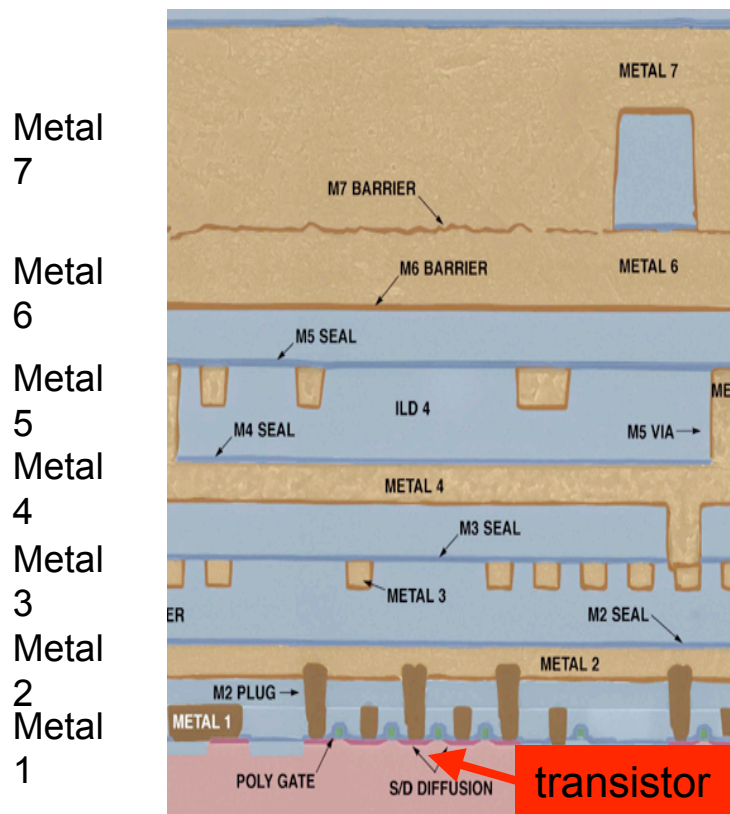
$$\tau = \frac{C_{Load} V_{DD}}{I_D(on)} \approx 10 \text{ ps}$$

(90 nm technology node) 18

2. CMOS Tutorial: [system speed](#)

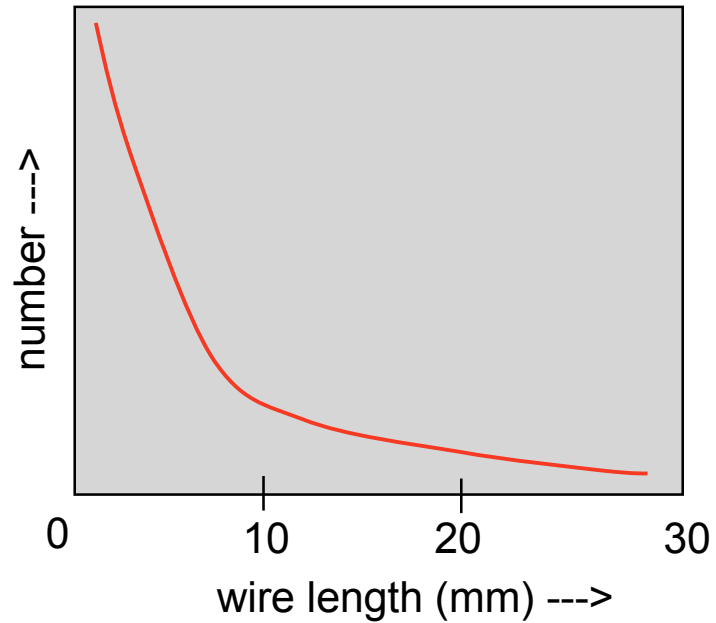


2. CMOS Tutorial: system speed



Silicon wafer

Rent's Rule



$$\tau_{global} \approx r_{int} c_{int} \sim l^2 \approx 100 \text{ ps}$$

(90 nm technology node)

2. CMOS Tutorial: [system speed](#)

until ~1990:

device delay > interconnect delay

Today (90nm technology):

device delay: ~ 1ps

1 mm interconnect delay: ~ 6 ps

2015 (22 nm technology):

device delay: ~0.1ps

1 mm interconnect: ~30ps

J. Meindl, "Beyond Moore's law: the interconnect era," *Computing in Science and Engineering*, 2003

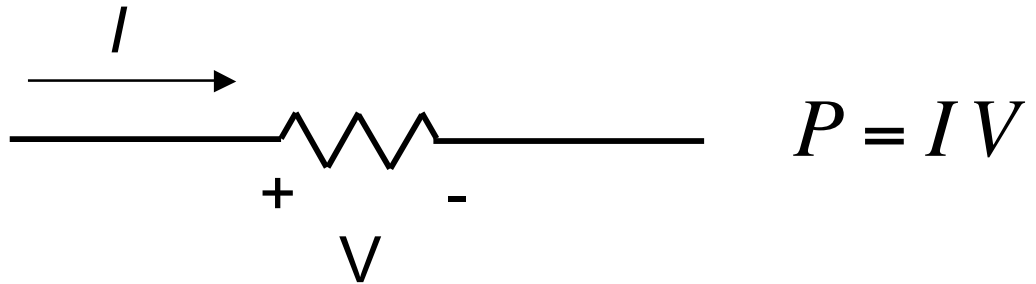
2. CMOS Tutorial: system speed

$$\tau = \frac{C_{Load} V_{DD}}{I_D(on)}$$

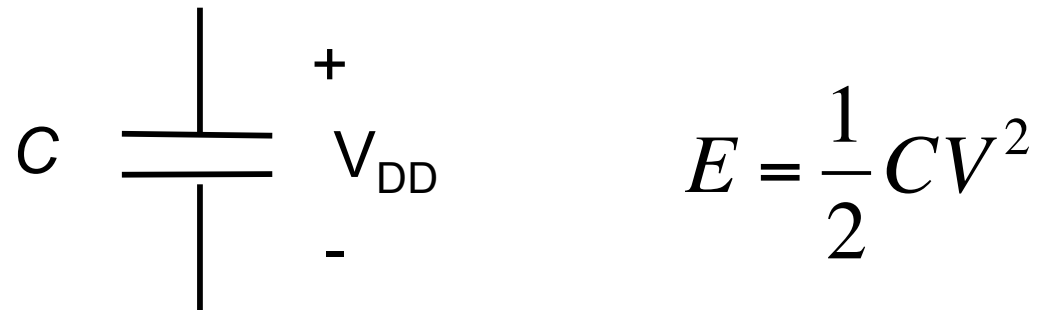
speed is controlled by the DC “on-current”

2. CMOS Tutorial: [system power](#)

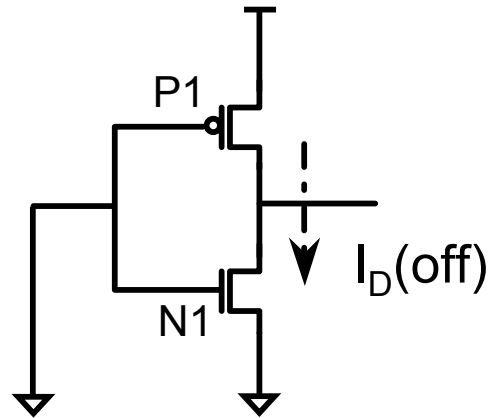
DC Power:



Energy:

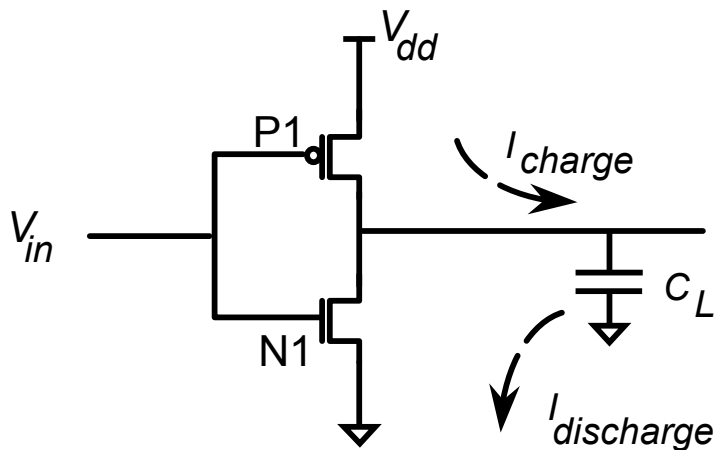


2. CMOS Tutorial: system power



1) standby power:

$$P_{off} = N_G I_D(off) V_{DD}$$

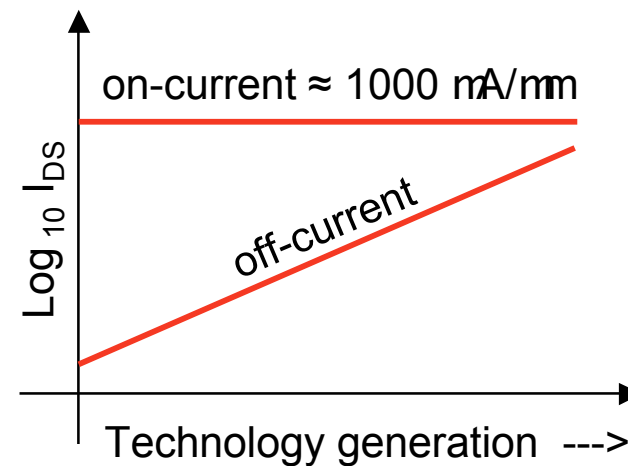
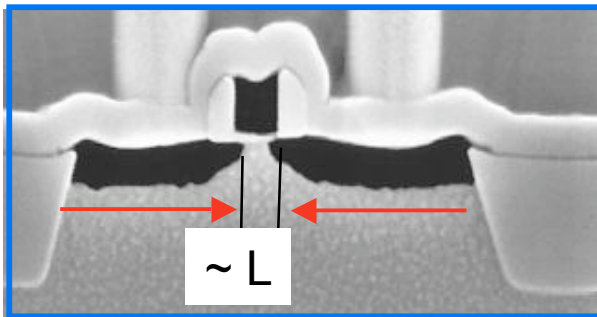


2) dynamic power:

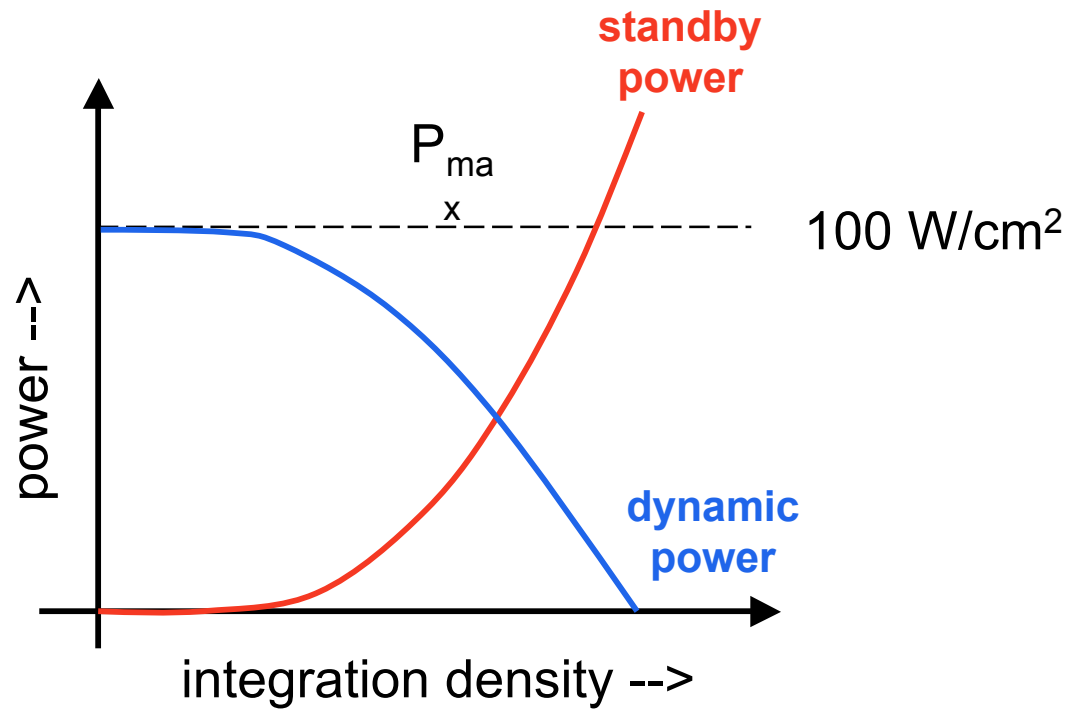
$$P_{on} = \alpha f C_{TOT} V_{DD}^2$$

2. CMOS Tutorial: [system power](#)

- 1) Lower V_{DD} means lower power
- 2) More leakage means more power
- 3) Higher on-current means higher speed
- 4) Faster operation means more power



2. CMOS Tutorial: system power



there is an optimum device size!

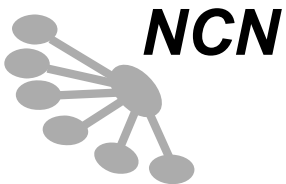
2. CMOS Tutorial: device requirements for digital systems

- high on-current
- low off-current
- gain
- acceptable power
- well-controlled parameters

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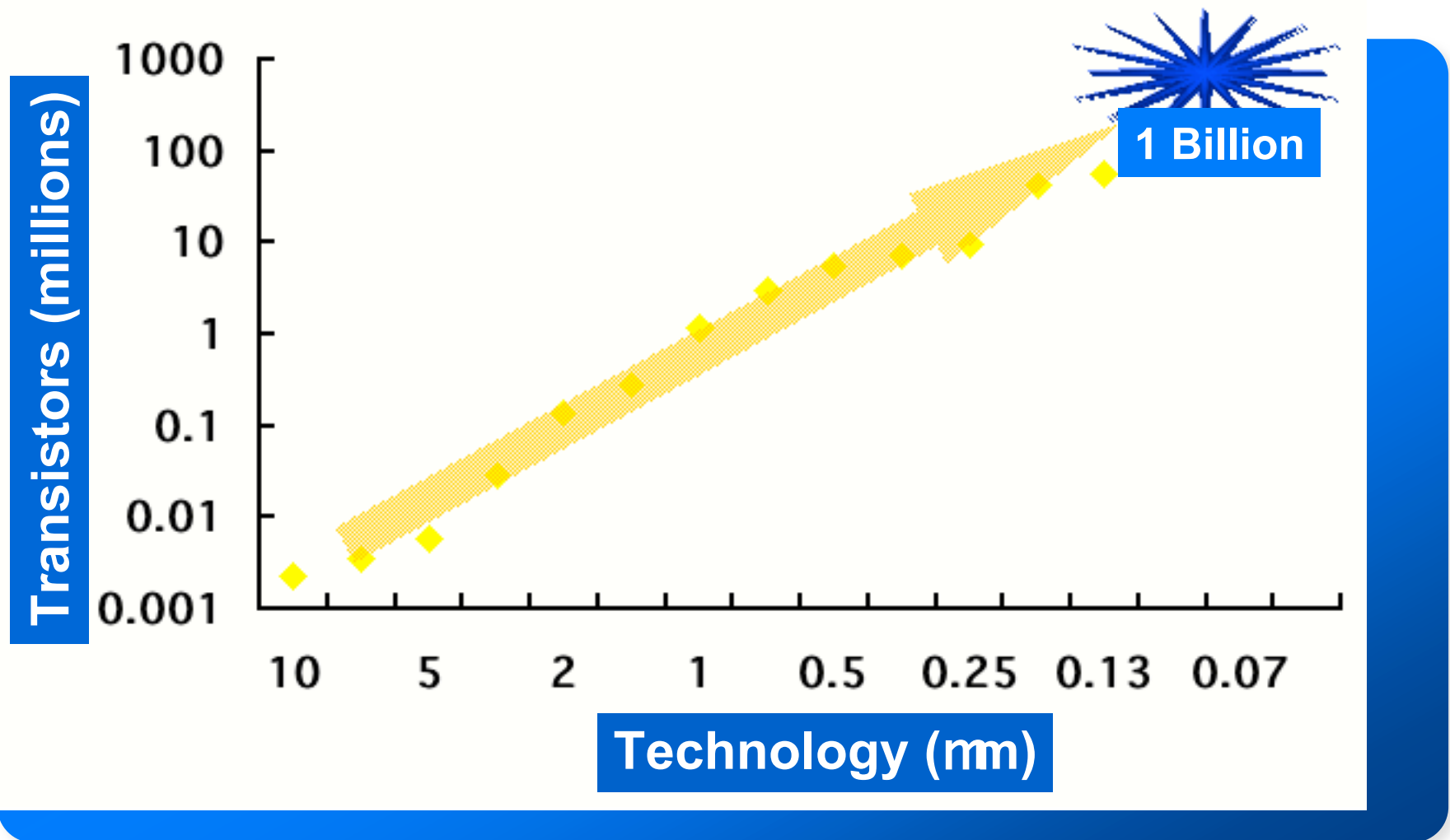


3. CMOS Today

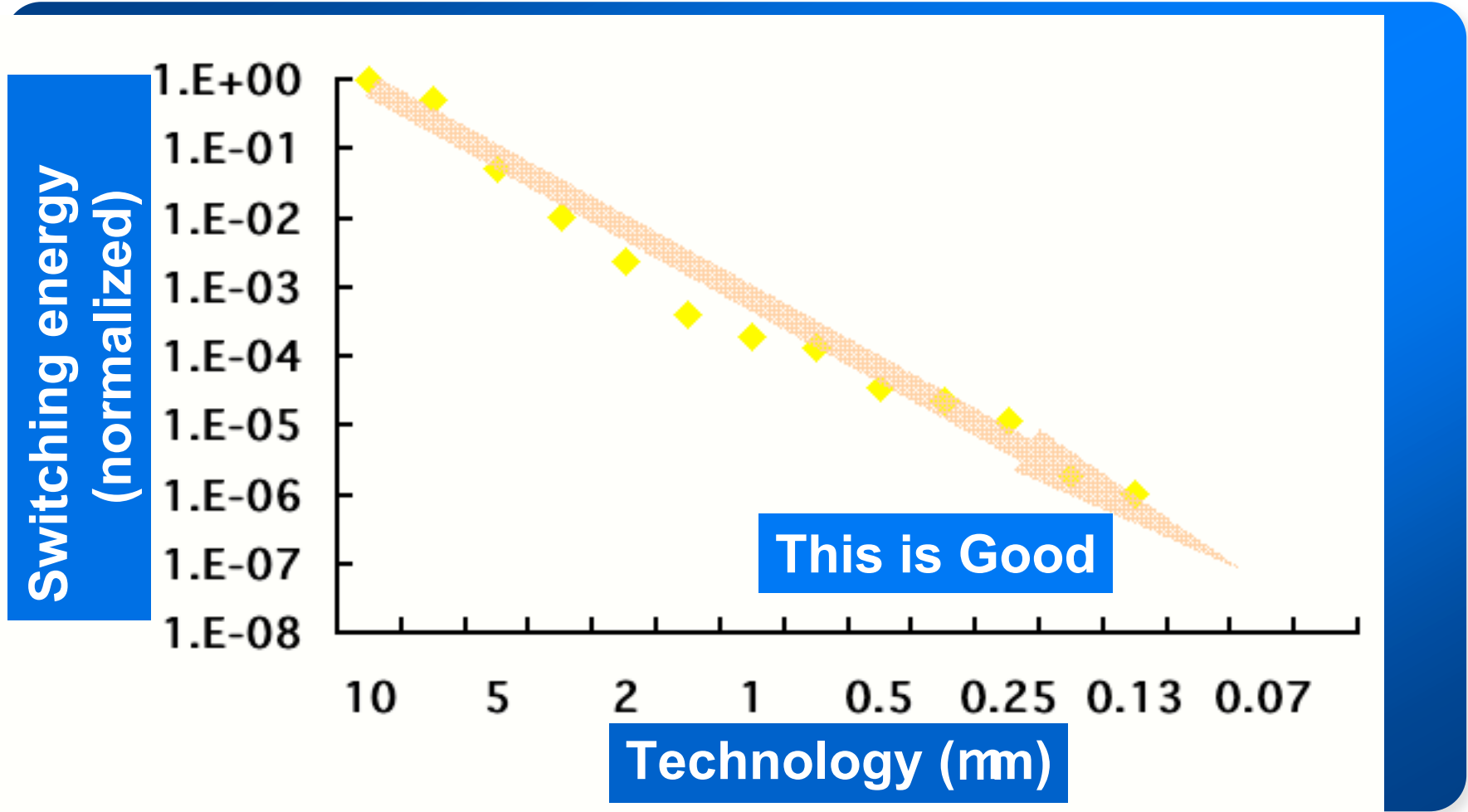
the following slides were provided courtesy of

Dr. Shekhar Borkar
Circuit Research, Intel Labs
Intel Corp.

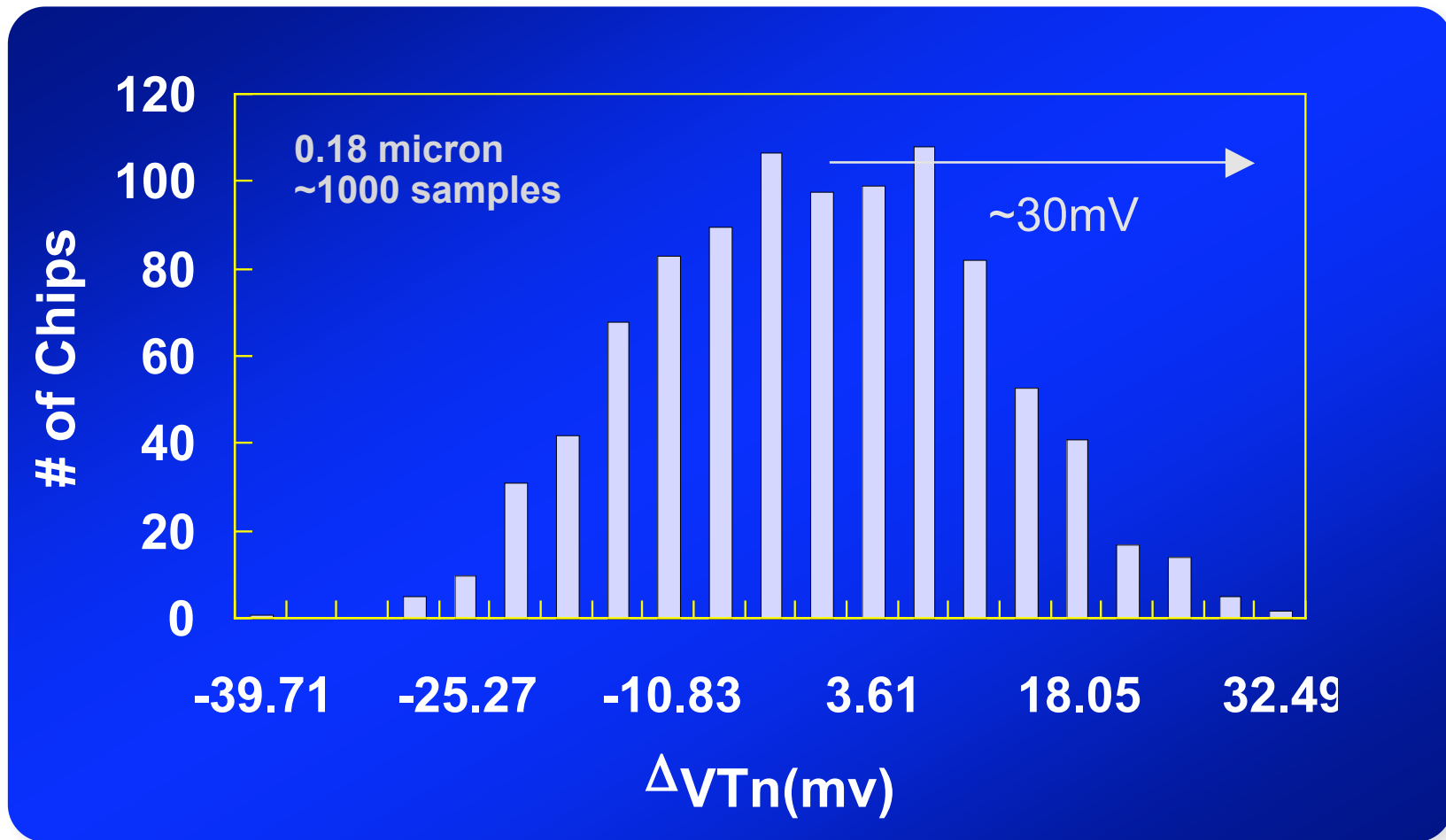
3. CMOS Today: [technology scaling](#)



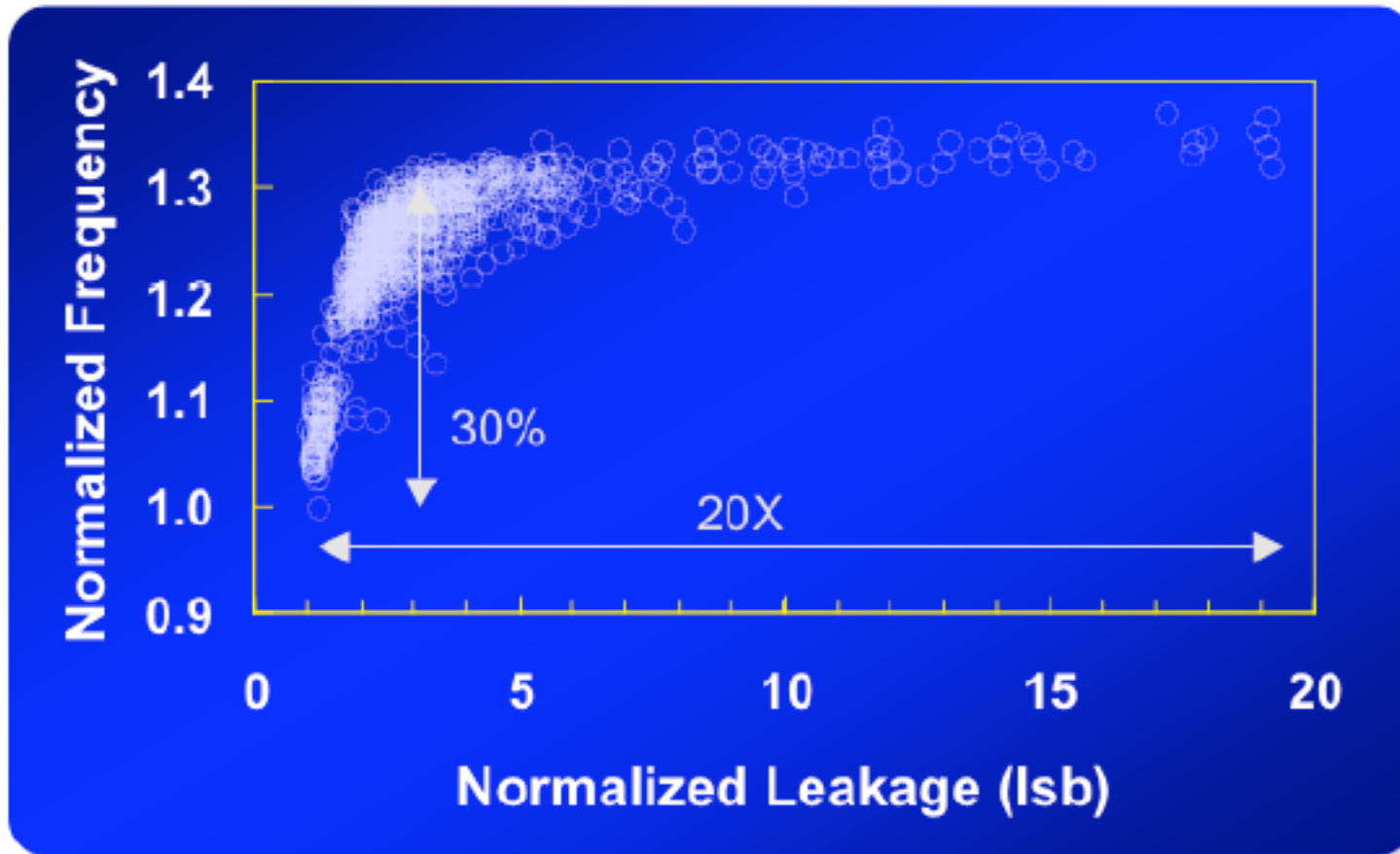
3. CMOS Today: [technology scaling](#)



3. CMOS Today: device variations

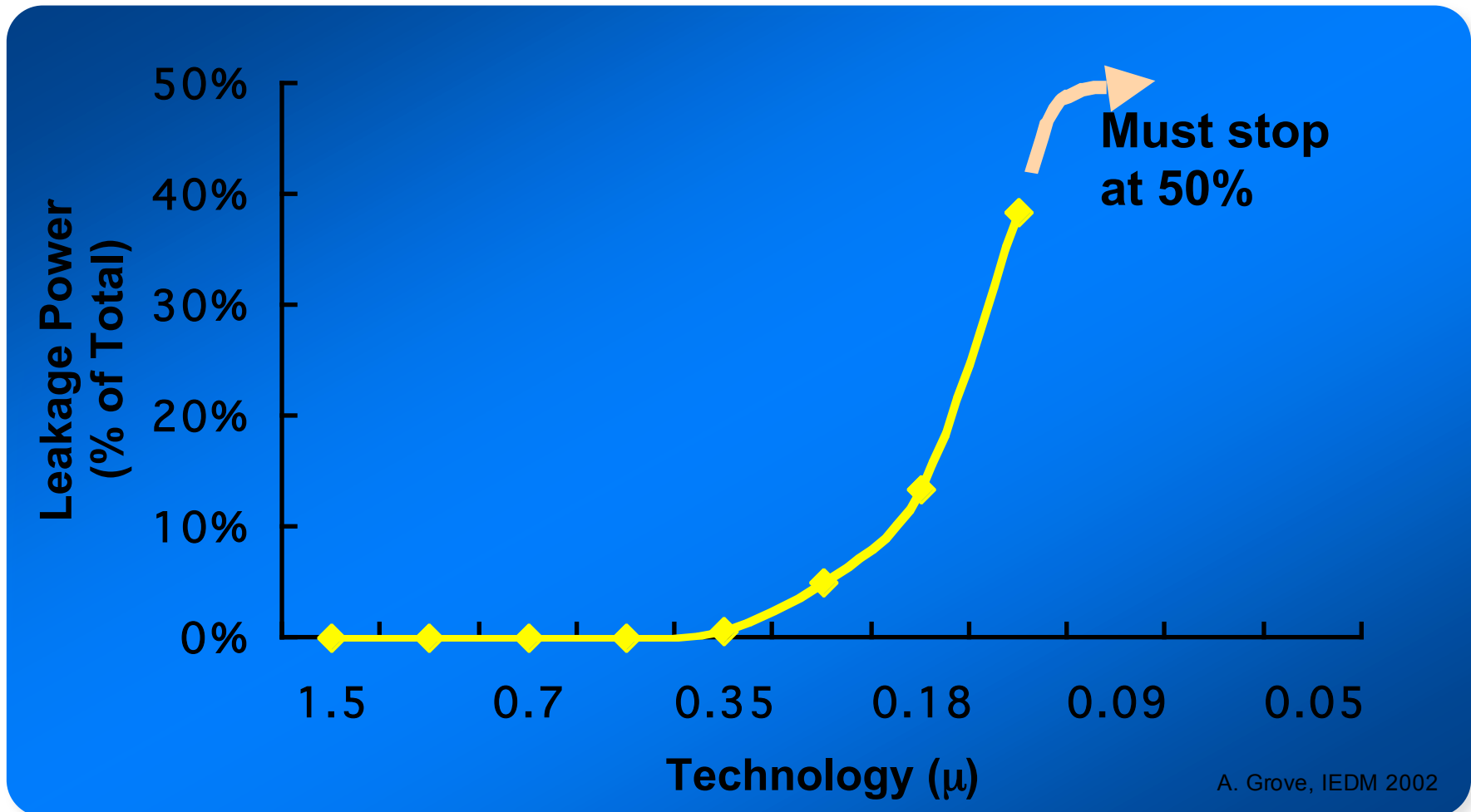


3. CMOS Today: device variations



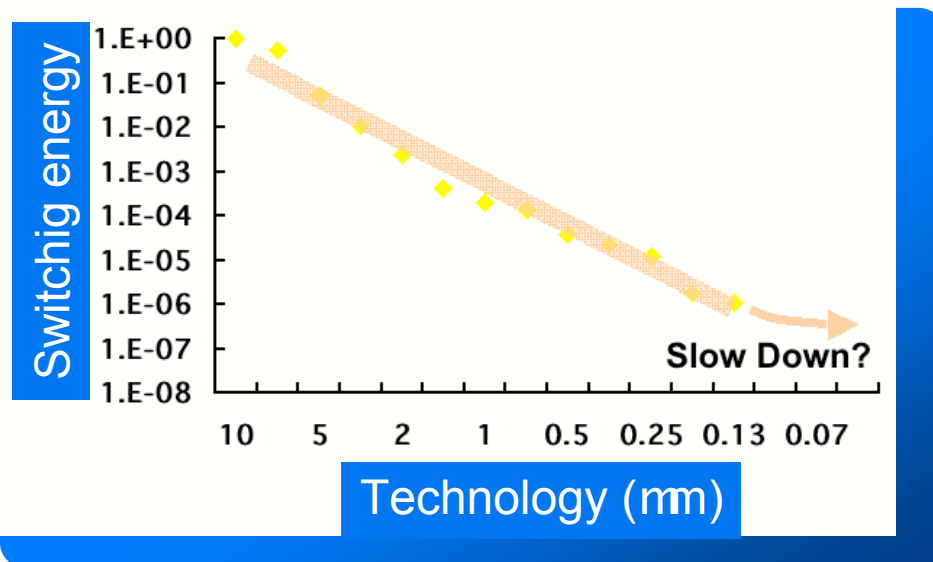
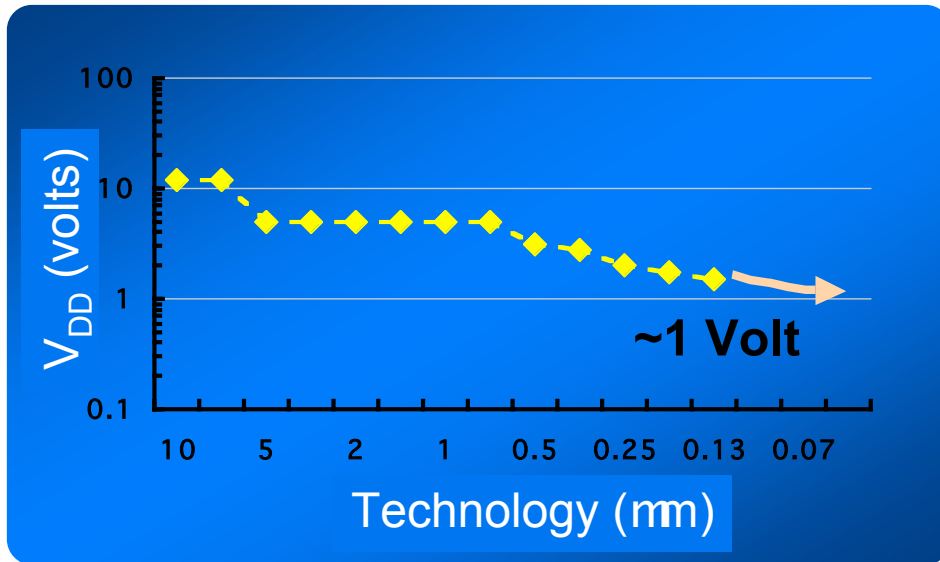
- ✎ 20X variation in SD leakage
- ✎ 30% variation in Frequency

3. CMOS Today: leakage power



Leakage power limits Vt scaling

3. CMOS Today: technology scaling



- T_{ox} scaling will slow down
- V_{DD} scaling will slow down
- V_T scaling will slow down
- Approaching constant V_{DD} scaling
- **Energy/logic op will not scale**

3. CMOS Today: technology scaling

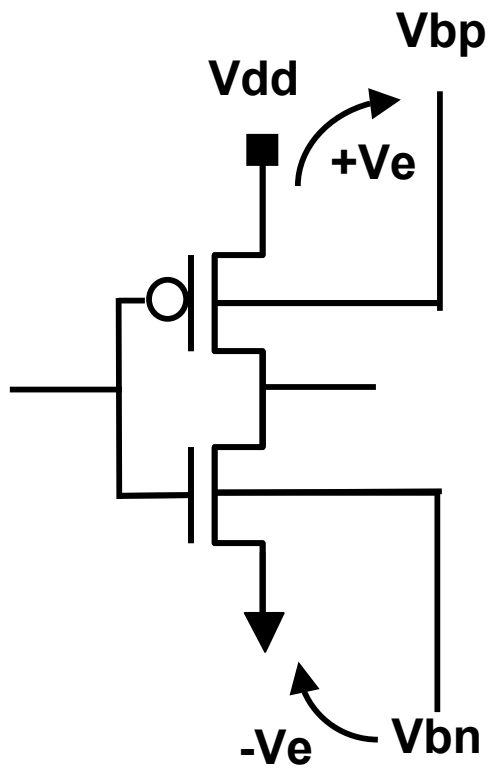
- >1B Transistor integration capacity will be available
- Could be unusable due to power
- Logic Transistor growth will slow down
- Transistor performance will be limited

Solutions:

- Low power design techniques
- Improve design efficiency
- Increased performance by even higher integration
(of slower transistors)

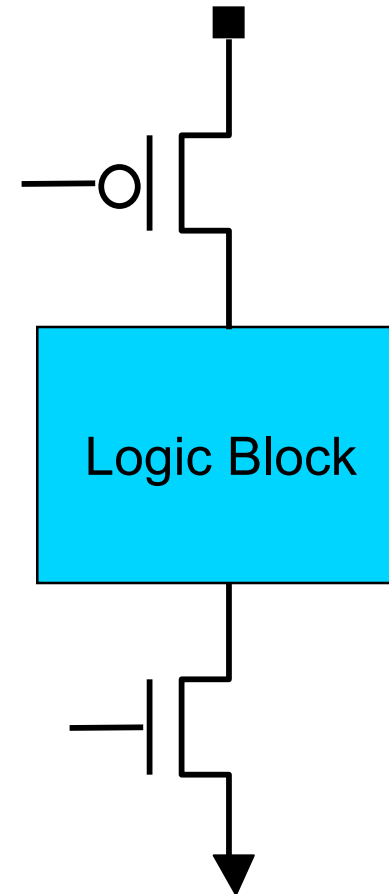
3. CMOS Today: solutions

Body Bias



2-10X reduction

Sleep Transistor

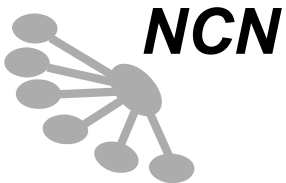


2-1000X reduction

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4. Summary

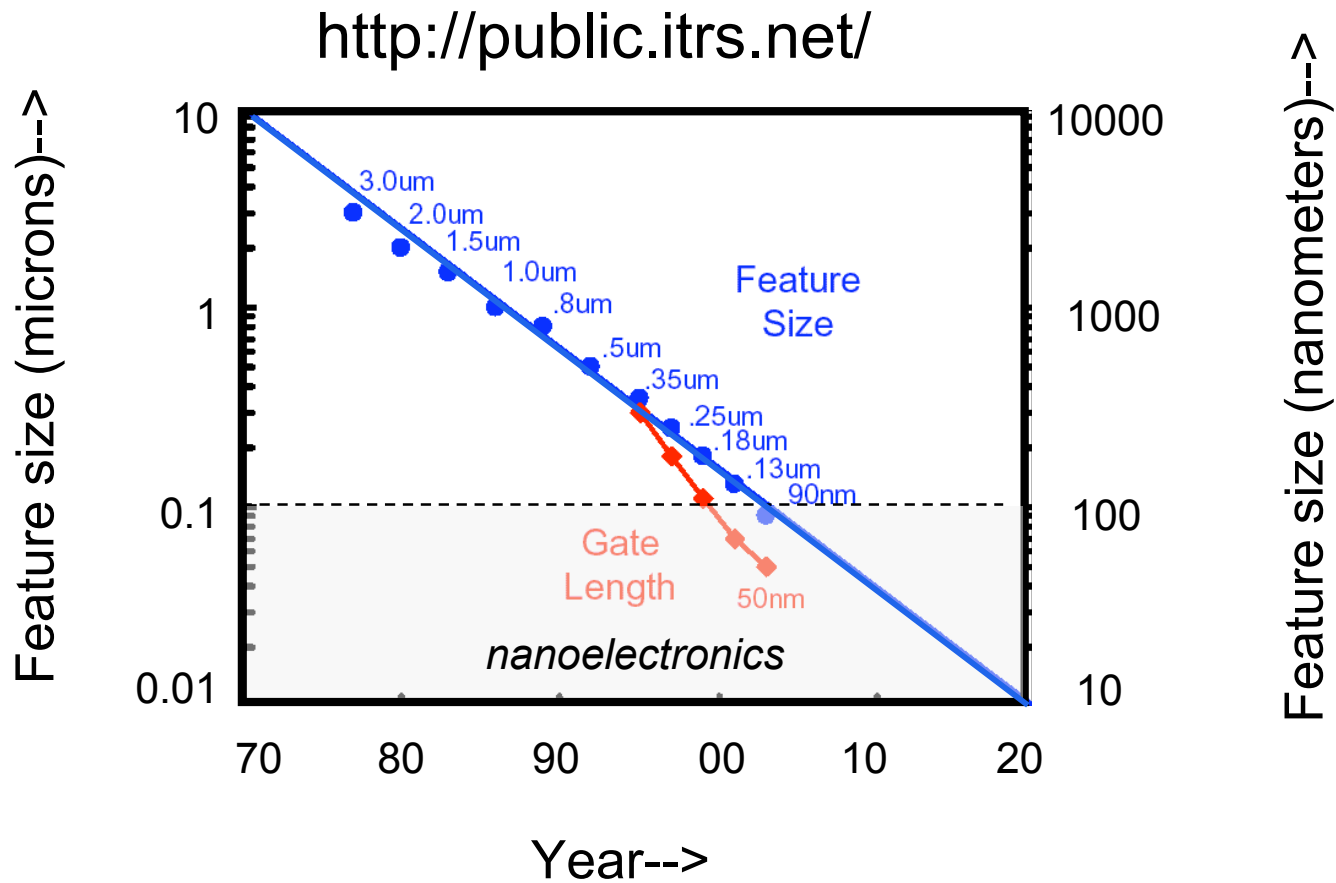
- 1) **CMOS devices face serious challenges**
leakage, variations, interconnects, ...
- 2) **Power dissipation limits device density**
not our ability to make devices small
- 3) **CMOS will operate near ultimate limits**
no transistor can be fundamentally better
- 4) **CMOS will provide more devices than can be used**
increasingly, design will drive progress

4. Summary

The promise of (bottom-up) nanoelectronics.....

- *understanding devices at the molecular scale*
- *new tools for metrology*
- *new materials*
- *unit processes for directed self-assembly*
- *new devices for new applications*
- *new architectures for ultra-dense systems*
- *terascale electronics*

4. Summary



(L = 6 nm (IBM, 2002)
L = 5 nm (NEC, 2003))