Section 32
Modern MOSFET

32.4 Mobility enhancement

Gerhard Klimeck
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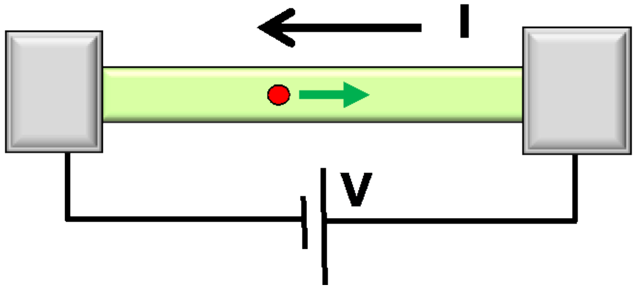
PURDUE UNIVERSITY®

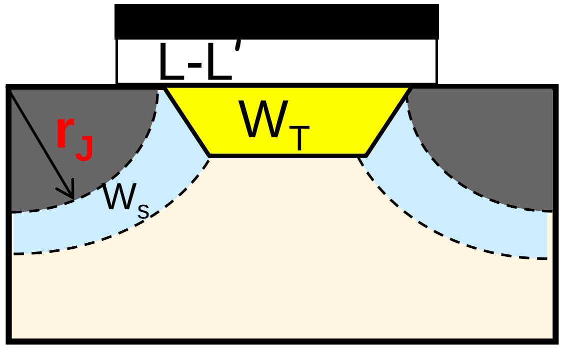
School of Electrical and
Computer Engineering

Section 32
Modern MOSFET



$$I = G \times V$$
$$= q \times n \times v \times A$$

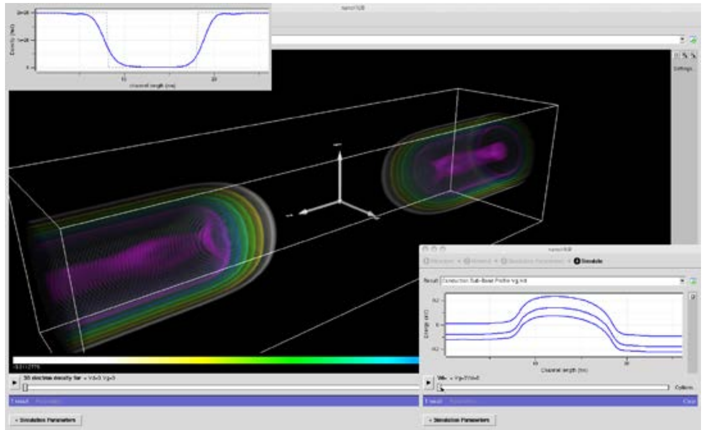
charge density velocity area

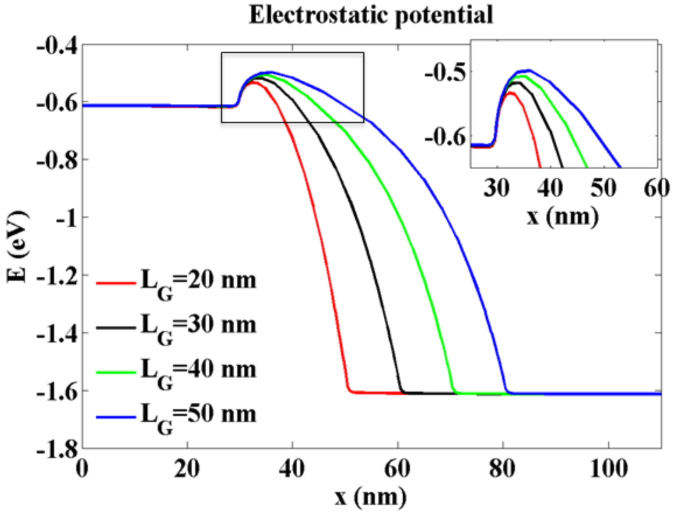


1 - 32.1 Some of Moore's Law Challenges
2 - 32.2 Short channel effect
3 - 32.3 Control of threshold voltage
4 - 32.4 Mobility enhancement

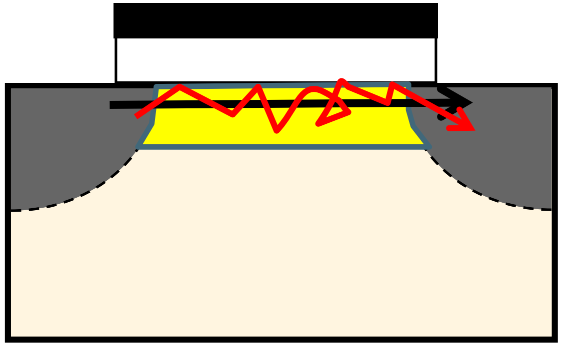
status

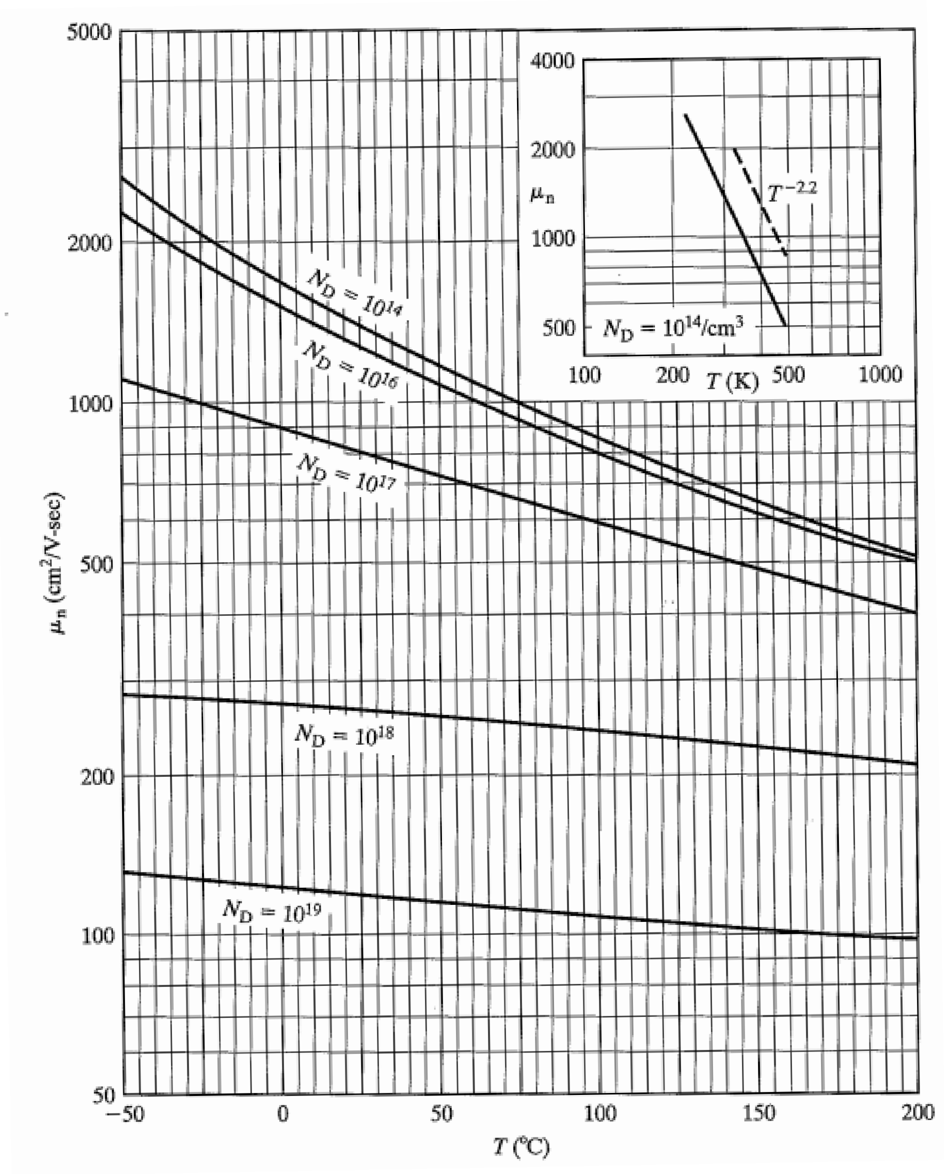
$$I_D = \frac{\mu C_{ox}}{L_{ch}}(V_G - V_{th}^*)^2$$





Mobility - Phonon and Doping Scattering



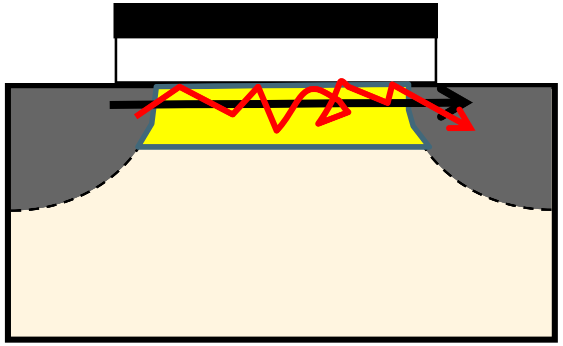


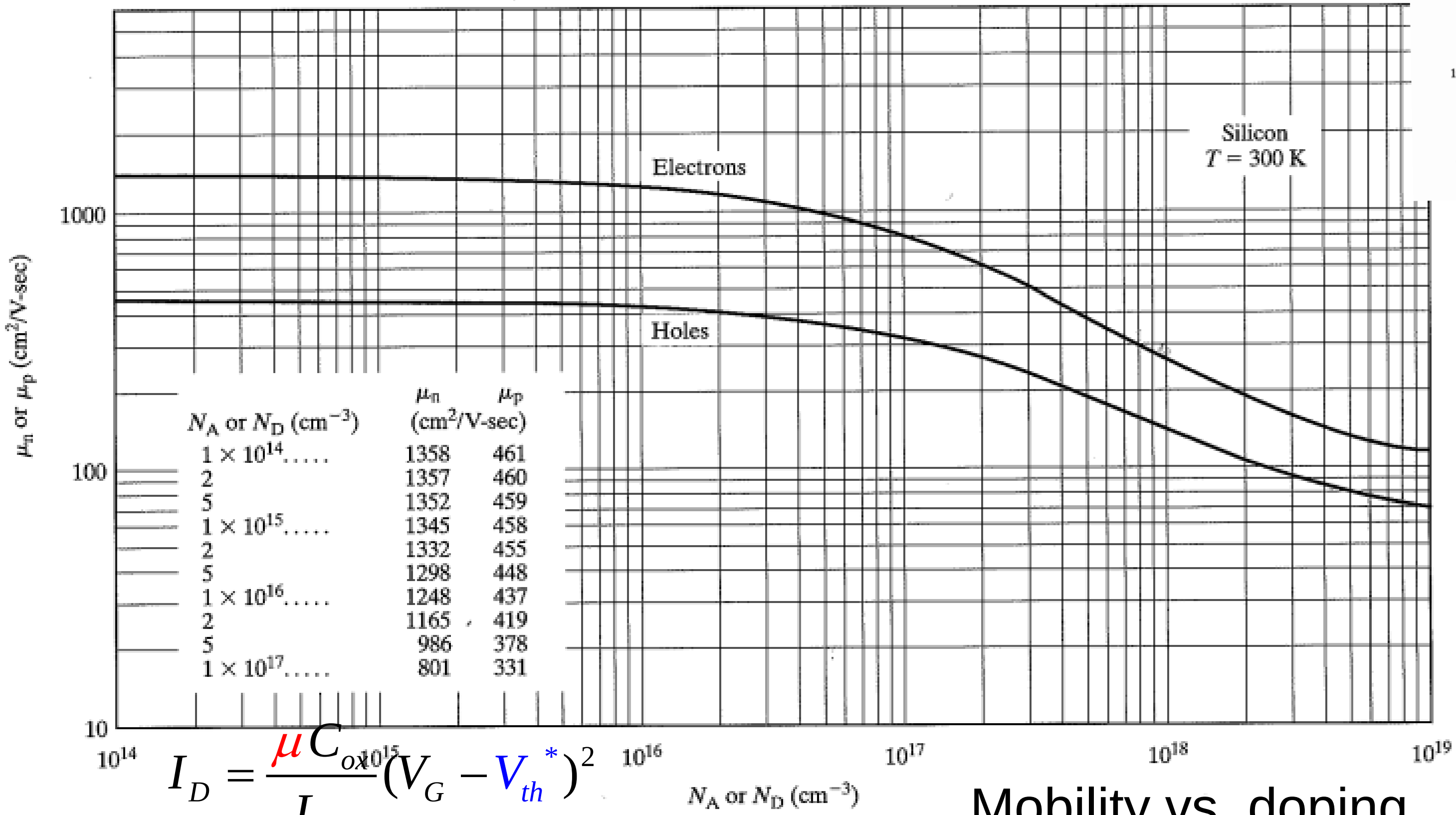
Mobility vs. temperature

Low bias mobility

$$I_D = \frac{\mu C_{ox}}{L_{ch}}(V_G - V_{th}^{*})^2$$

Few words about universal Mobility ….

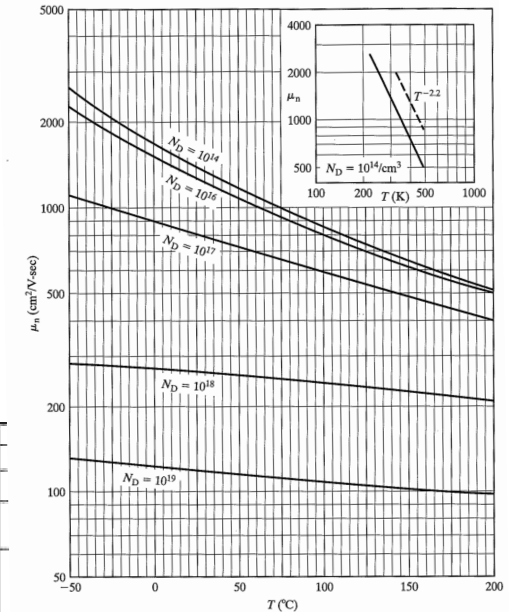




N_A or N_D (cm⁻³)	μ_n (cm²/V-sec)	μ_p (cm²/V-sec)
1 × 10^{14}.....	1358	461
2	1357	460
5	1352	459
1 × 10^{15}.....	1345	458
2	1332	455
5	1298	448
1 × 10^{16}.....	1248	437
2	1165	419
5	986	378
1 × 10^{17}.....	801	331

$$I_D = \frac{\mu C_{ox}}{L_{ch}}(V_G - V_{th}^{*})^2$$

Mobility vs. doping



Mobility vs. temperature

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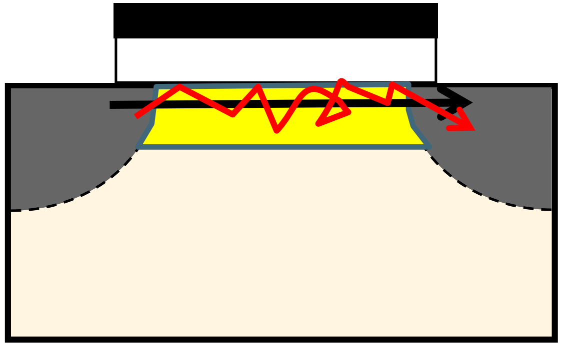
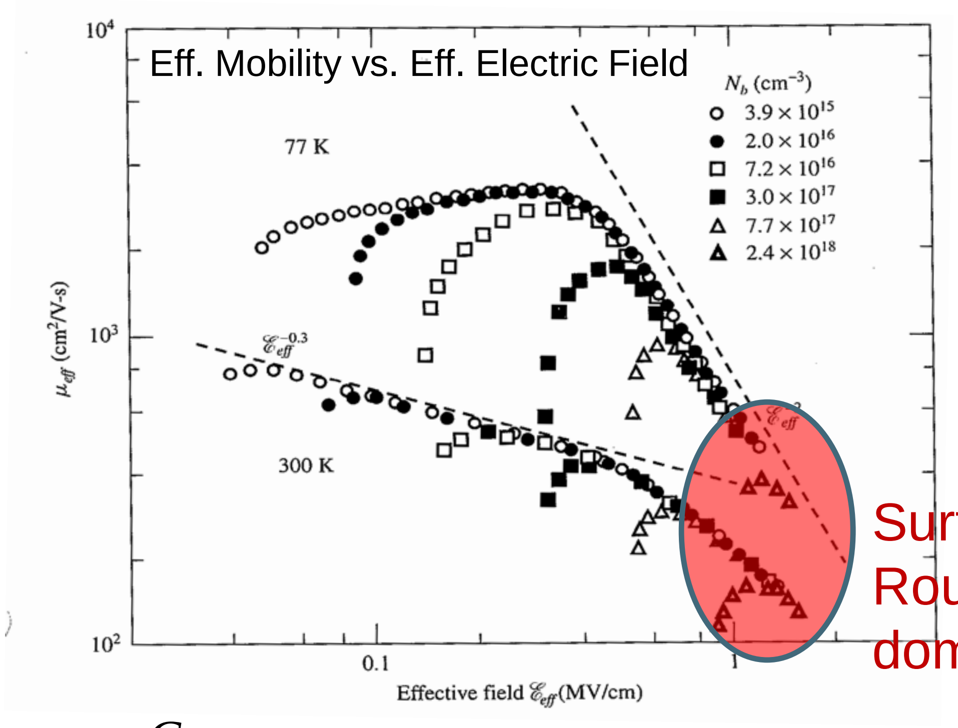


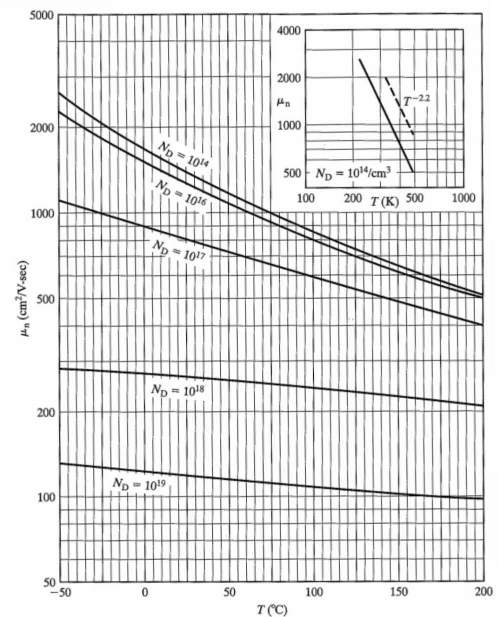
Gate E-field → electrons pulled to surface (surface scattering)

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_G - V_{th})}$$

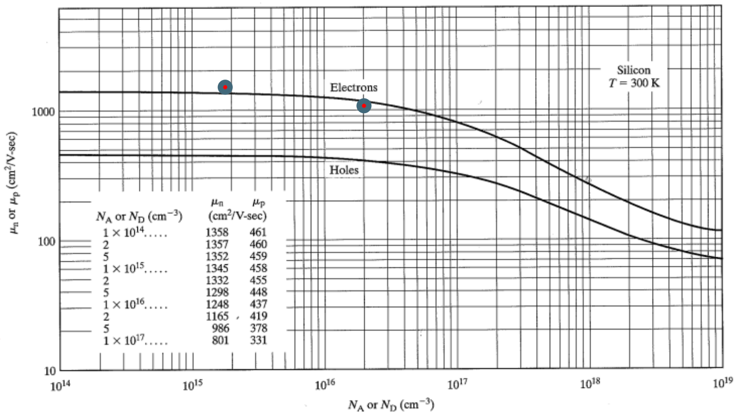


Surface Roughness dominates

$$I_D = \frac{\mu C_{ox}}{L_{ch}}(V_G - V_{th}^*)^2$$



Mobility vs. temperature



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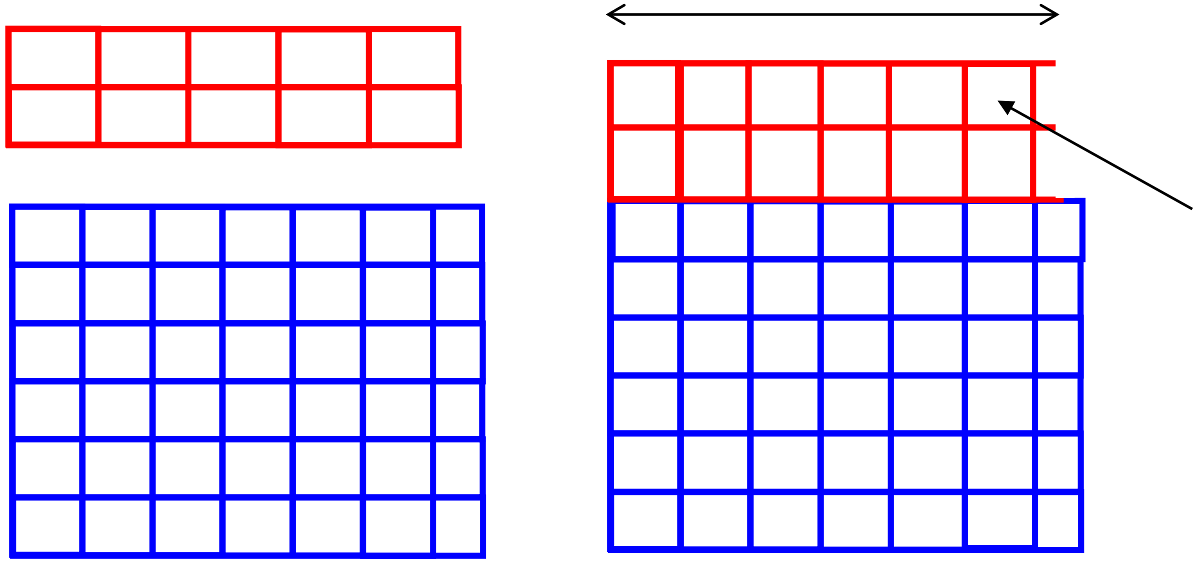
Mobility vs. doping

Low bias mobility

Basics of Strain ..



Larger lattice

Compressive
biaxial strain

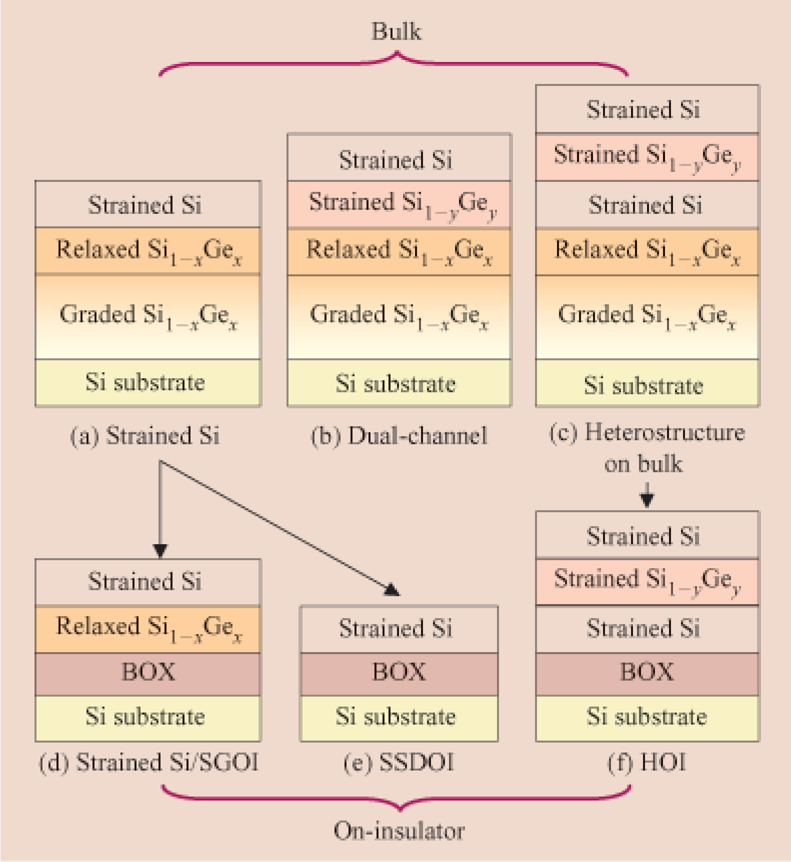
Use **strained** materials to enhance mobility
(strain can reduce effective mass)

Enhances mobility
in the channel …

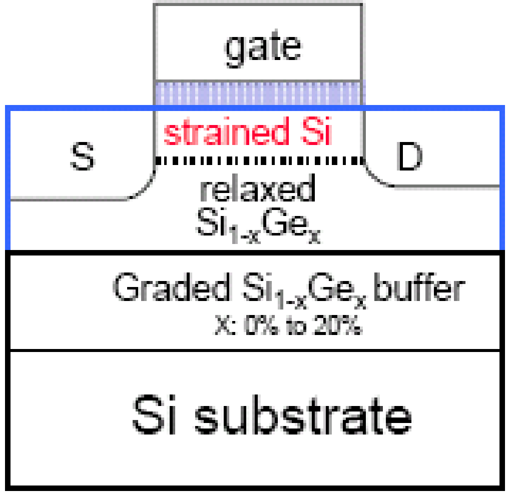
Smaller lattice

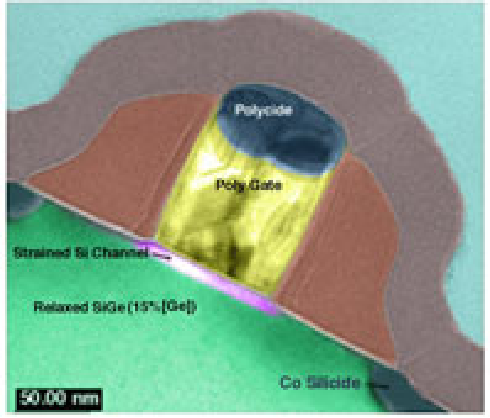
Biaxial Strain to Enhance Mobility

Examples of strained Si structures



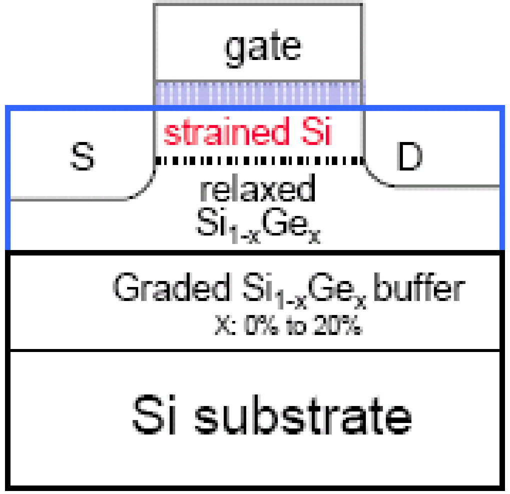
Experimental Device using strained Si

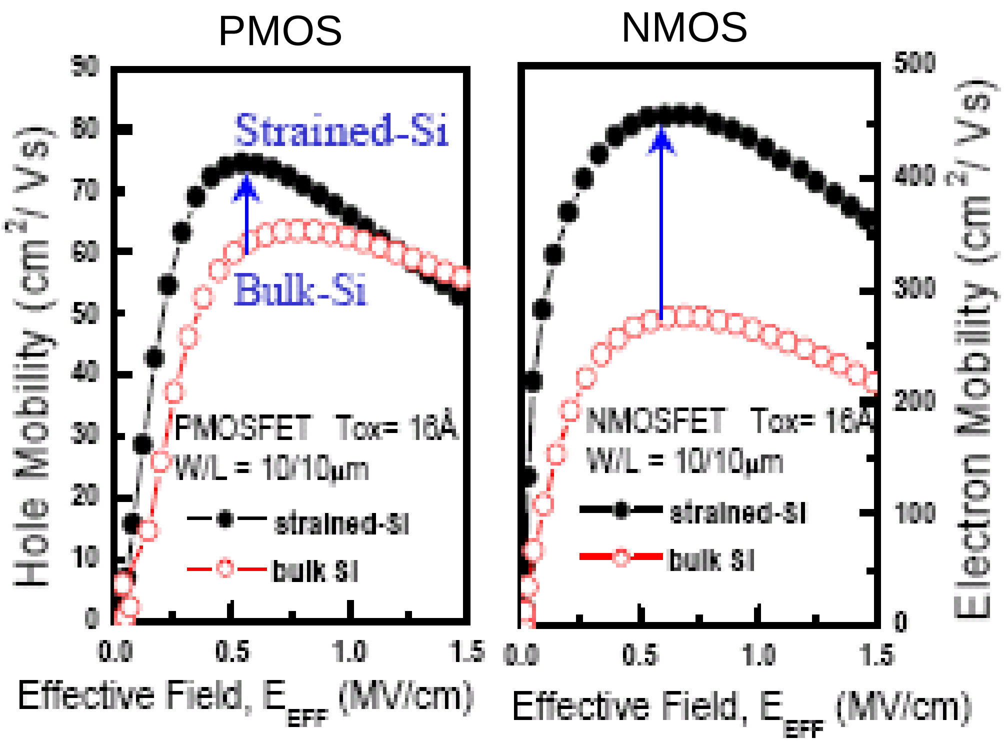




Biaxial Strain to Enhance Mobility

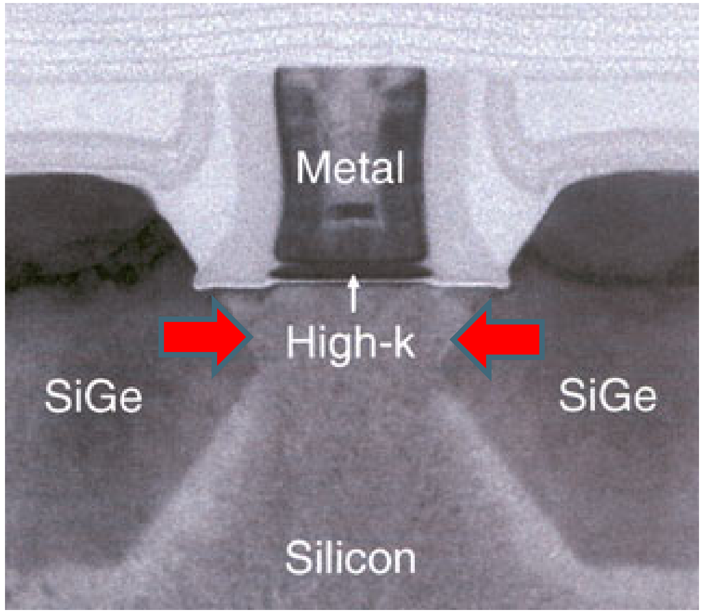
Experimental Device using strained Si





Adapted from Chang et. al, IEDM 2005.

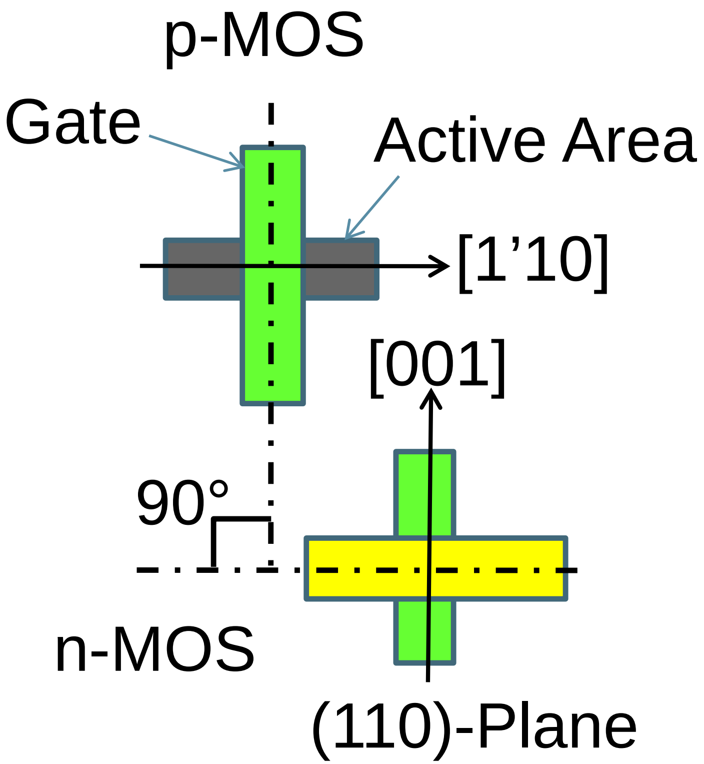
Uniaxial Compressive Strain to Enhance Mobility



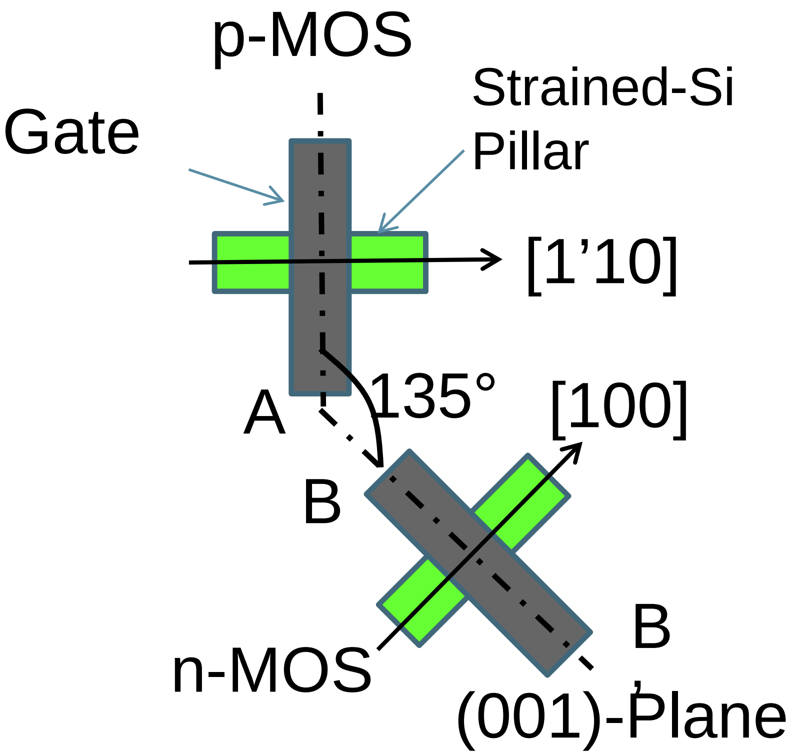
Uniaxial strain from source and drain

Orientation Dependent Mobility

Try different crystal directions to maximize mobility



Fin-FET



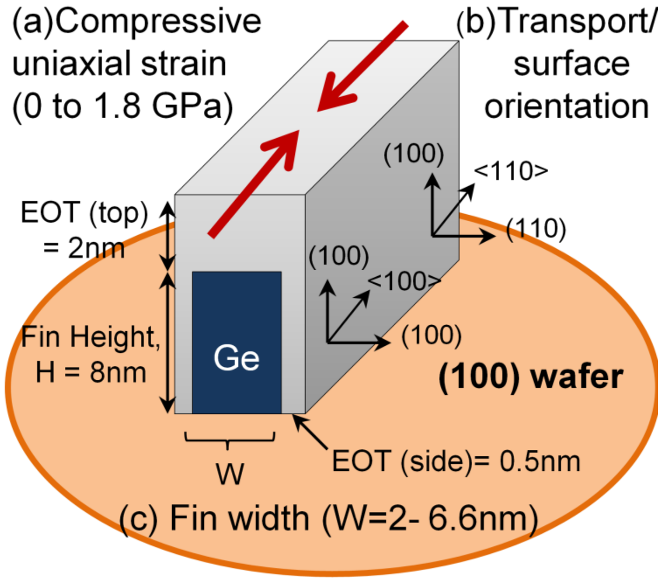
Takagi, TED 52, p.367, 2005

Implemented at TI in 90nm node, 2004, simulated with NEMO s/w By R.C. Bowen

Ge, Si and InGaAs FinFETs

Objective:

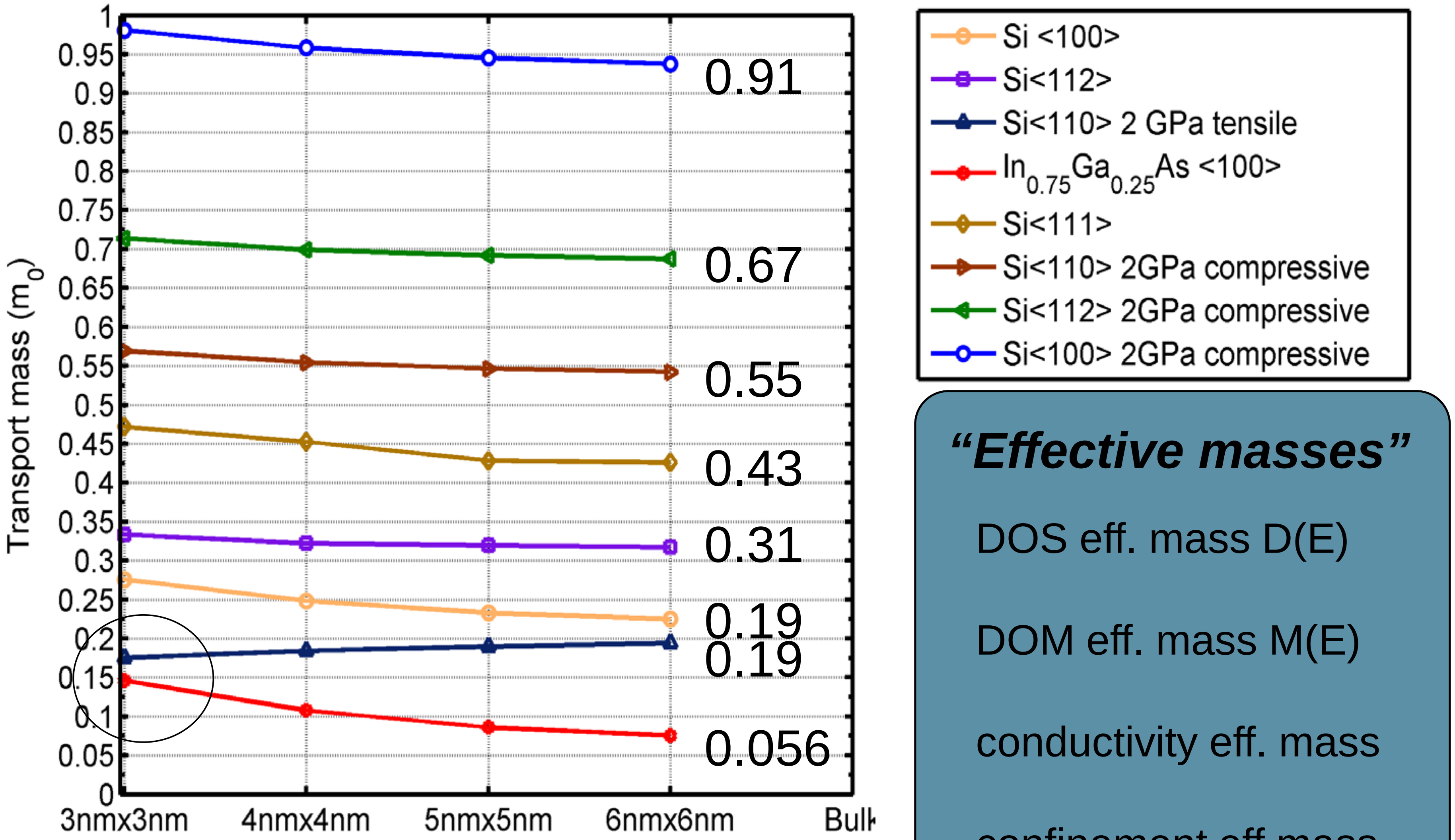
- Identifying performance boosters in Ge FinFETs for hole transport.



Approach

- Self-consistent Top of the barrier model used (NEMO5).
- Computed v_{inj} for different (a) Compressive strain, (b) Orientation and (c) Fin width scaling at a constant inversion charge (1e13/cm^2).

results: eff mass engineering



"Effective masses"

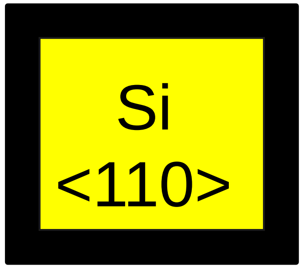
DOS eff. mass D(E)

DOM eff. mass M(E)

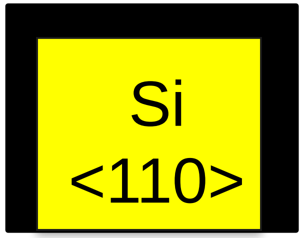
conductivity eff. mass

confinement eff mass

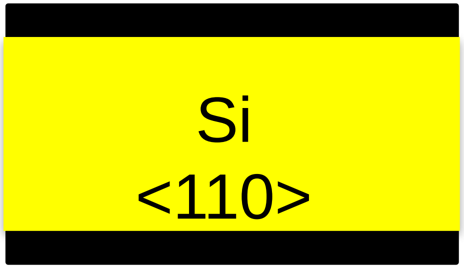
results: 5 nm MOSFETs



Gate all around



Tri-Gate



Double Gate

Si <110> 2GPa uniaxial tensile strain 3x3 nm^2

$m^* = 0.175\ m_0$ from TB bandstructure

EOT = 0.47 nm, $V_{DD} = 0.5$ V

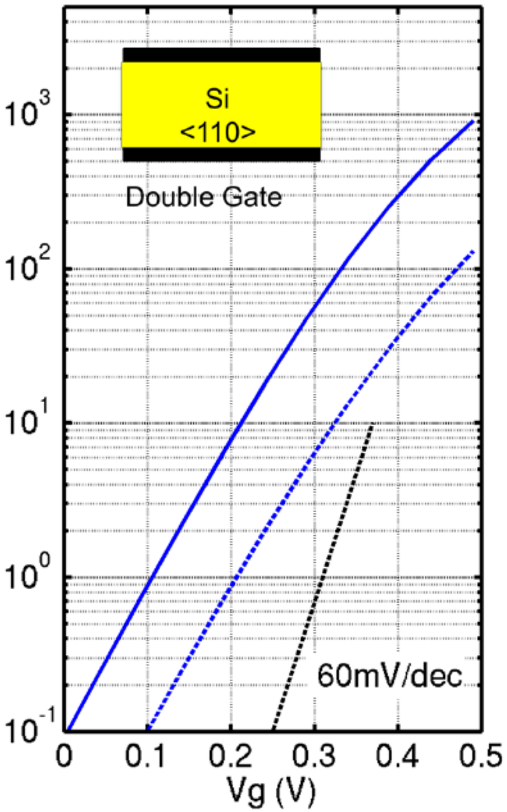
Simulations done by Klimeck group with NEMO5

results: 5 nm MOSFETs

Gate all around

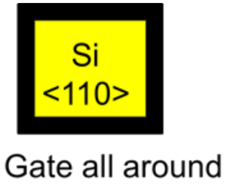
Tri-Gate

Double Gate



	I_{ON} (uA/um)	SS(mV/dec)	DIBL(mV/V)
Double Gate	~900	101.5	200
Tri-Gate	~2000 (norm. with height)	91.3	120
Gate-All-Around	~3000 (norm. with height)	84.1	90

results: 5 nm MOSFETs



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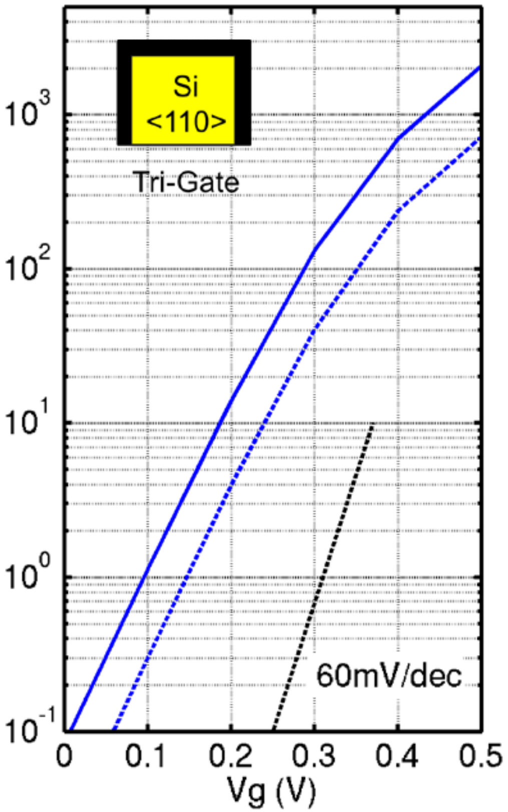
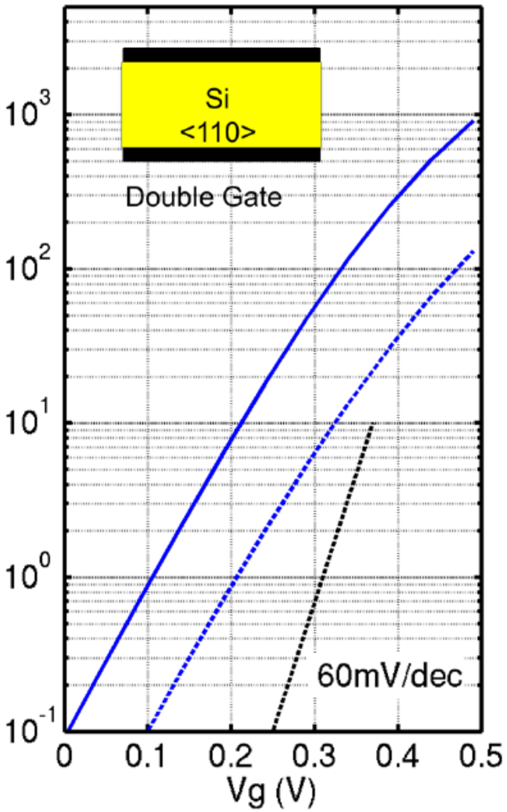


Double Gate



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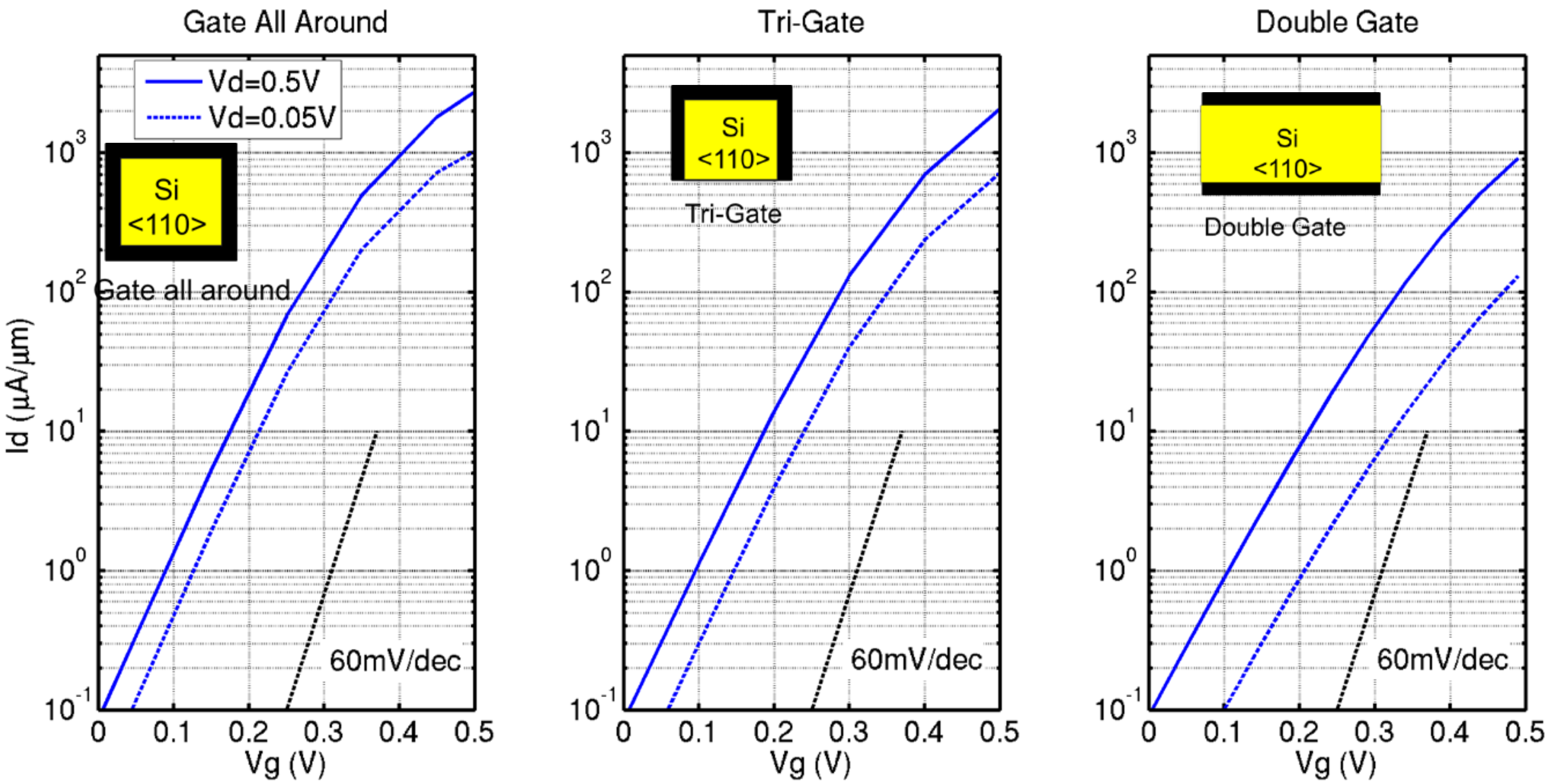

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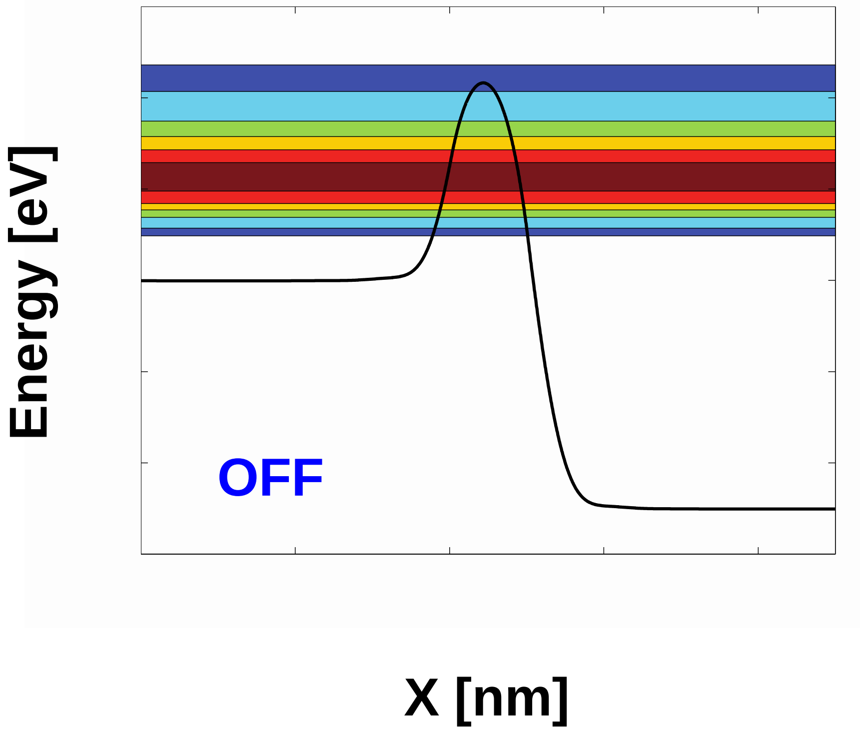
Double Gate	~900	101.5	200
Tri-Gate	~2000 (norm. with height)	91.3	120
Gate-All-Around	~3000 (norm. with height)	84.1	90

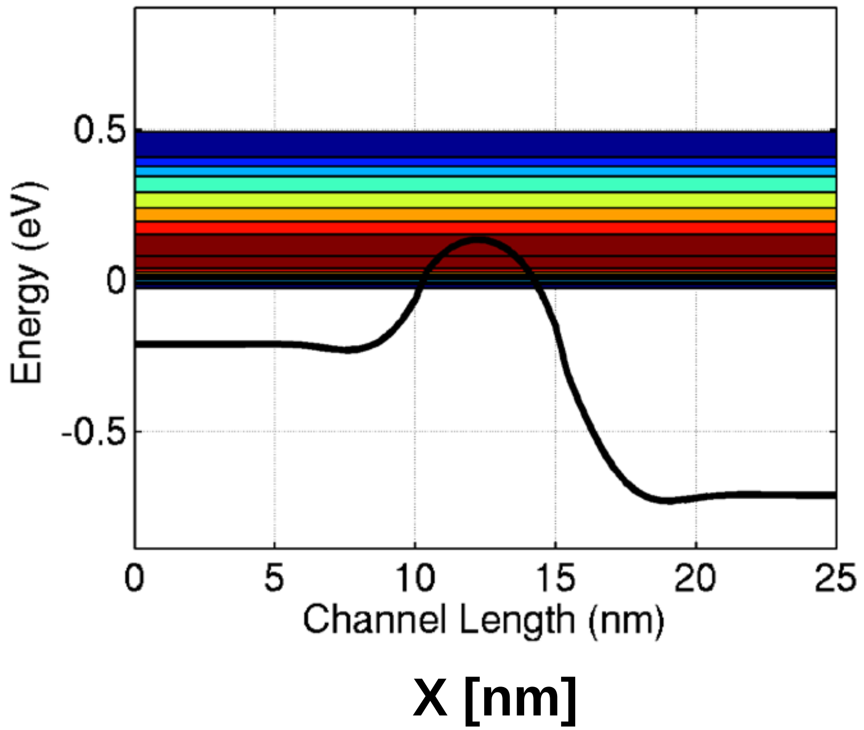
results: SD tunneling in 5 nm MOSFETs

Double Gate *L* = 5nm



Tunneling Current = 96%

GAA = 5nm

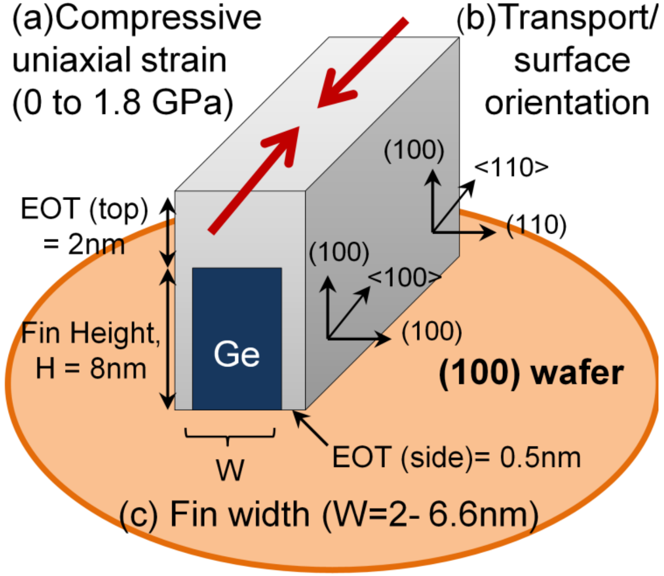


Tunneling Current = 45%

Ge, Si and InGaAs FinFETs

Objective:

- Identifying performance boosters in Ge FinFETs for hole transport.

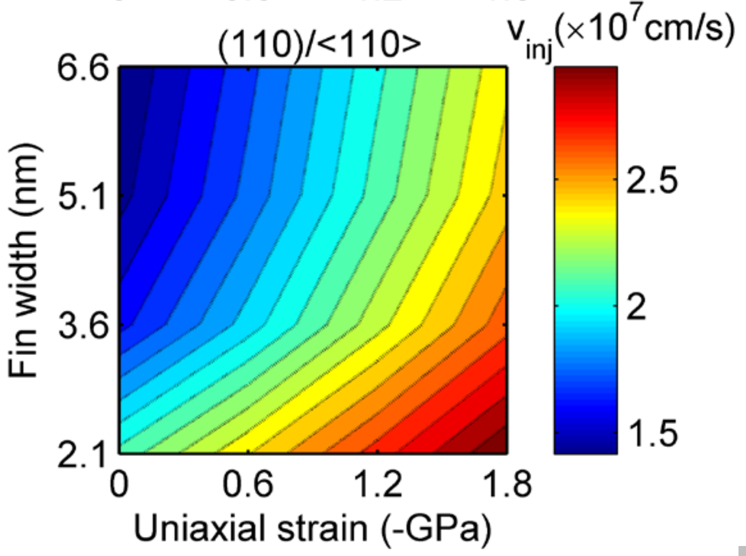


Approach

- Self-consistent Top of the barrier model used (NEMO5).
- Computed v_{inj} for different (a) Compressive strain, (b) Orientation and (c) Fin width scaling at a constant inversion charge (1e13/cm^2).

Results

- Similar enhancement in v_{inj} compared to mobility→ **v_{inj} a good metric for performance.**
- **(110)/<110> shows ~2.5X enhancement over (100)/<100>** for all strain/Fin width cases.
- **Fin width scaling** identified as a **performance booster** for (110)/<110> orientation that is additive to strain.



Summary

1) MOSFET scaling issues
    - Short channel effects
    - Discrete dopings
    - Interface roughness
    - Gate tunneling
    - Source tunneling
2) New materials – winner is not clear yet
3) High Mobility may not be the most important => source-drain tunneling
4) Contacts will become more important and dominate device performance
5) Effective masses and bandgaps can be engineered!

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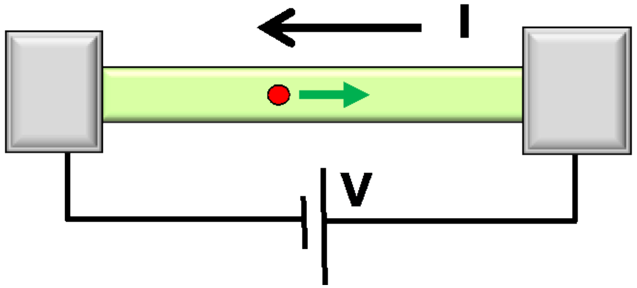

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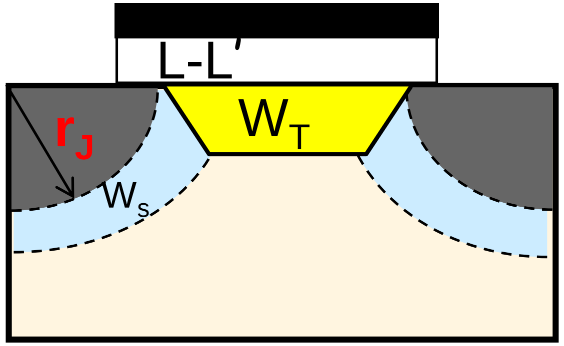

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- 32.2 Short channel effect
- 32.3 Control of threshold voltage
- 32.4 Mobility enhancement

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