Section 32
Modern MOSFET

32.3 Control of threshold voltage

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School of Electrical and
Computer Engineering

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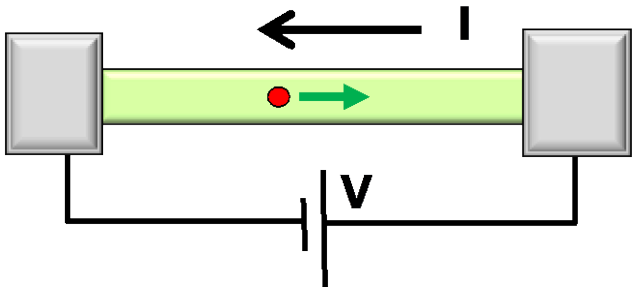
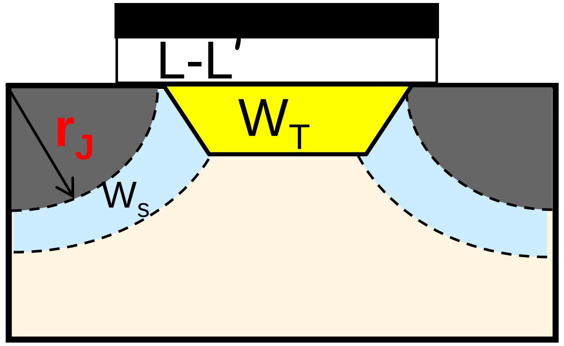
Modern MOSFET

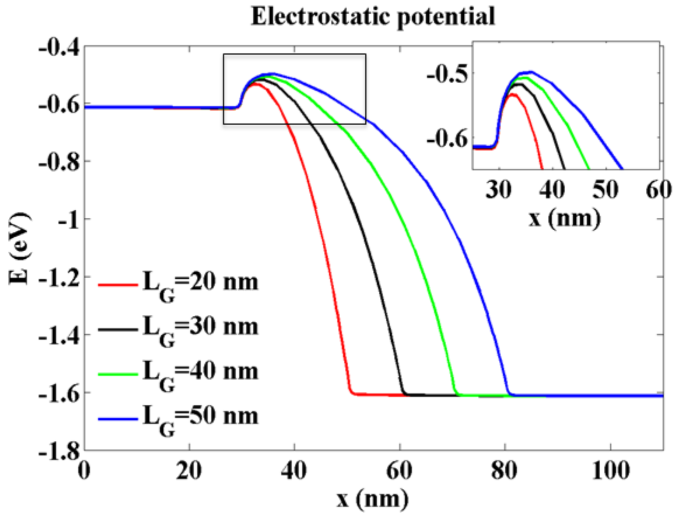


$$I = G \times V$$
$$= q \times n \times v \times A$$

charge density velocity area

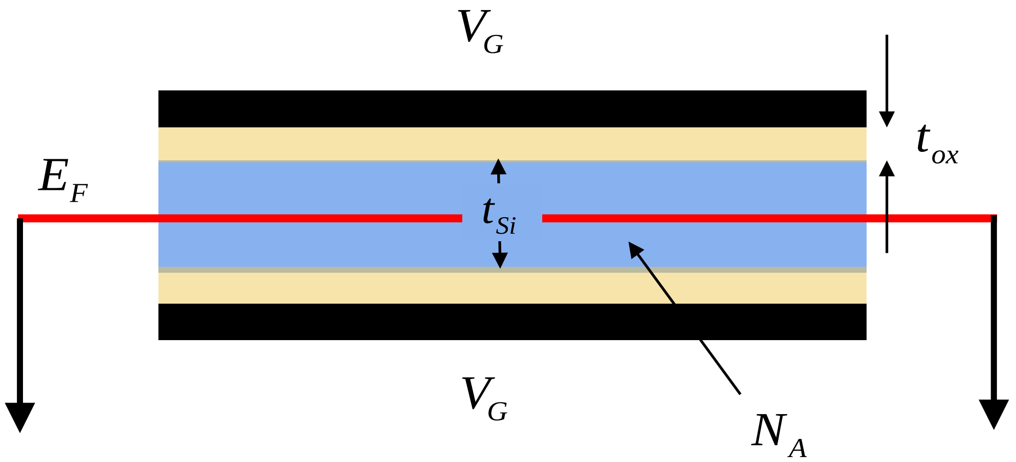


- 32.1 Some of Moore's Law Challenges
- 32.2 Short channel effect
- 32.3 Control of threshold voltage ← status
- 32.4 Mobility enhancement

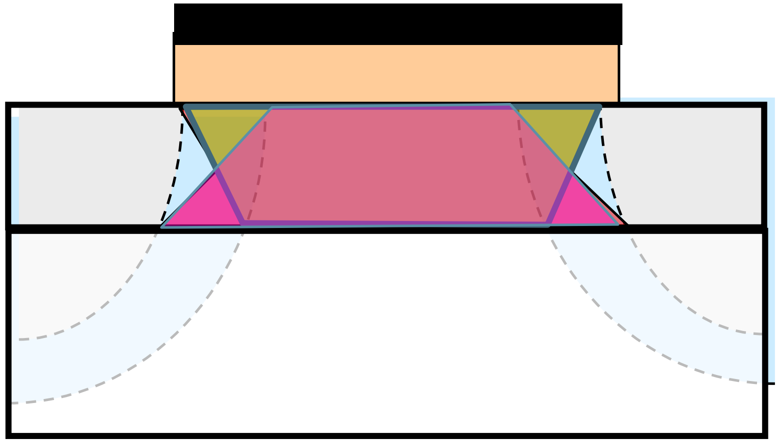


Solution: Ultra-thin Body SOI

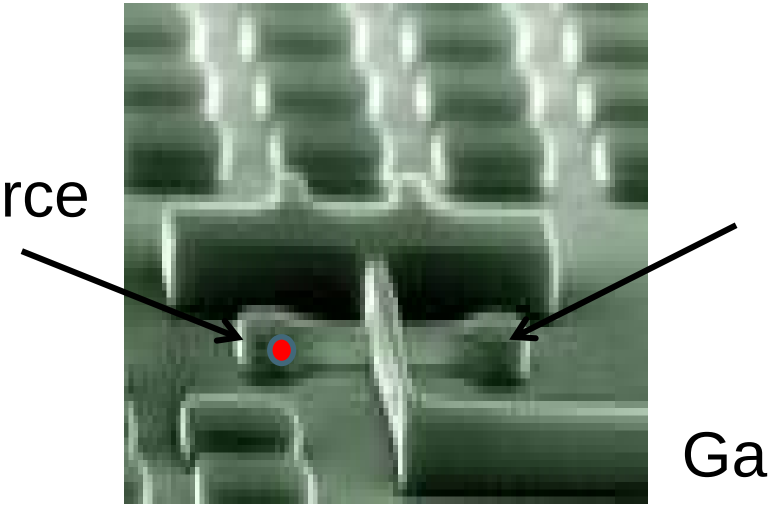
Two Gates → better channel control



SOI: Silicon On Insulator



Example: FINFET, OmegaFET, X-FET

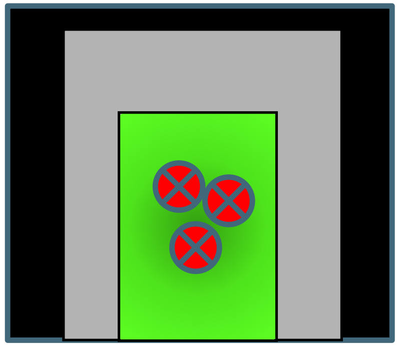


Source

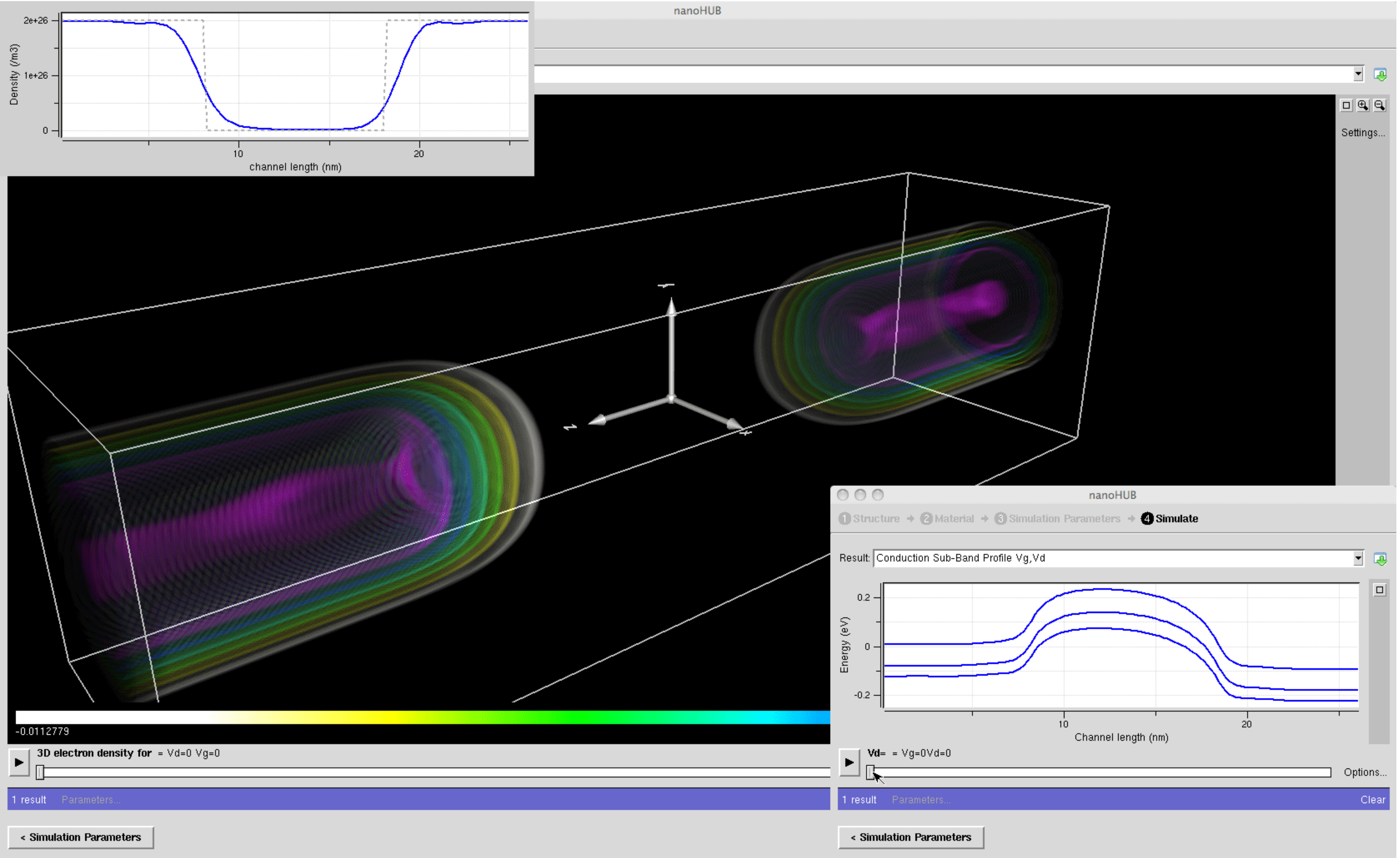
Drain

Gate

Cross-section



Electro-Static Control in a GAA Nanowire nanowire tool on nanoHUB.org



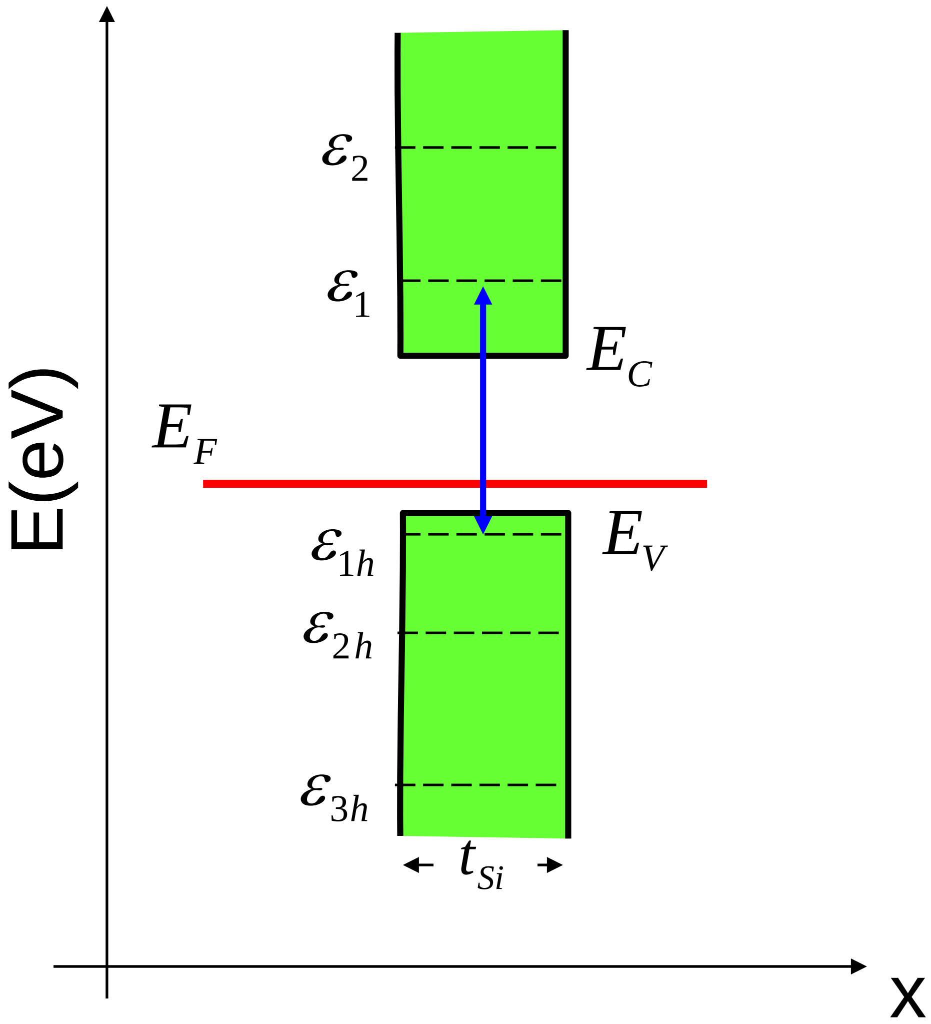
3D electron density for = Vd=0 Vg=0

Result: Conduction Sub-Band Profile Vg,Vd

Vd= = Vg=0Vd=0

- **https://nanohub.org/tools/omenwire**

Quantization and Control of Fin-width

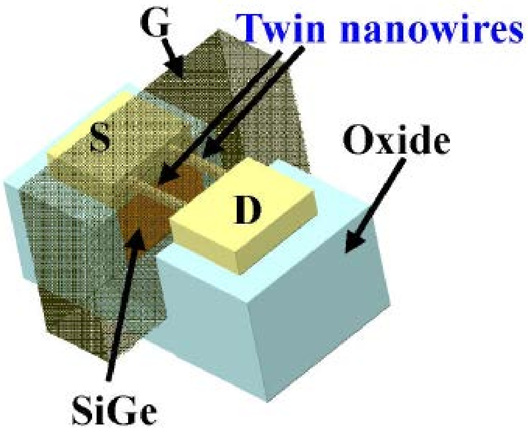


$$\varepsilon_n = \frac{\hbar^2 n^2 \pi^2}{2m^* t_{Si}^2}$$

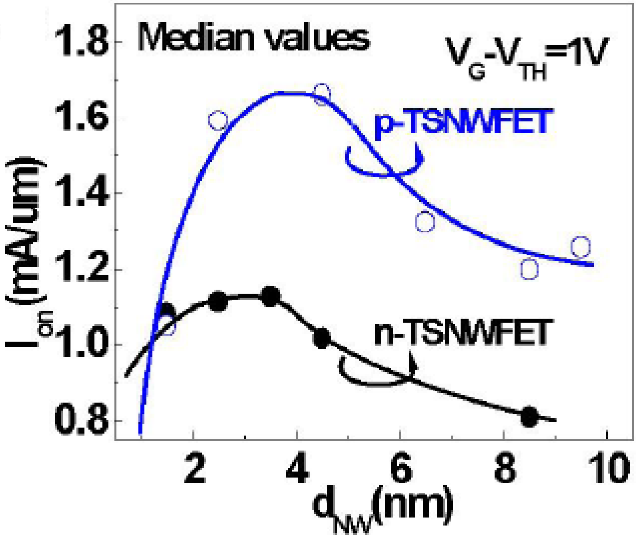
$$E_G' = E_G + \varepsilon_1 + \varepsilon_{1h}$$

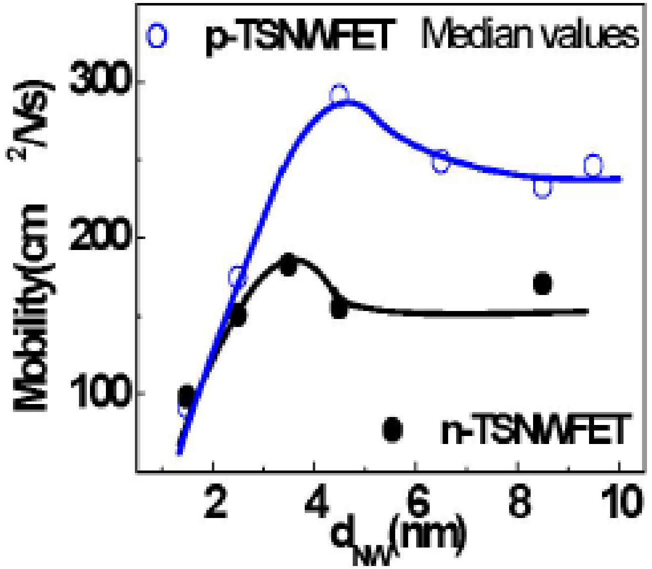
Band-gap widening
Fluctuation in thickness

Motivation



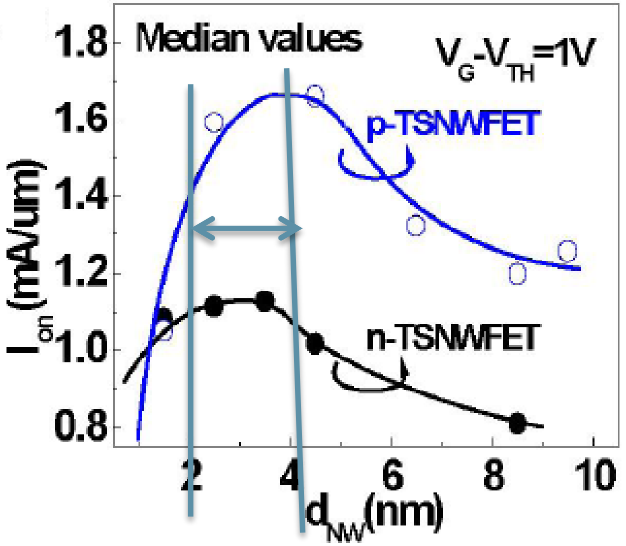
[1] S. D. Suk, IEDM, 2007





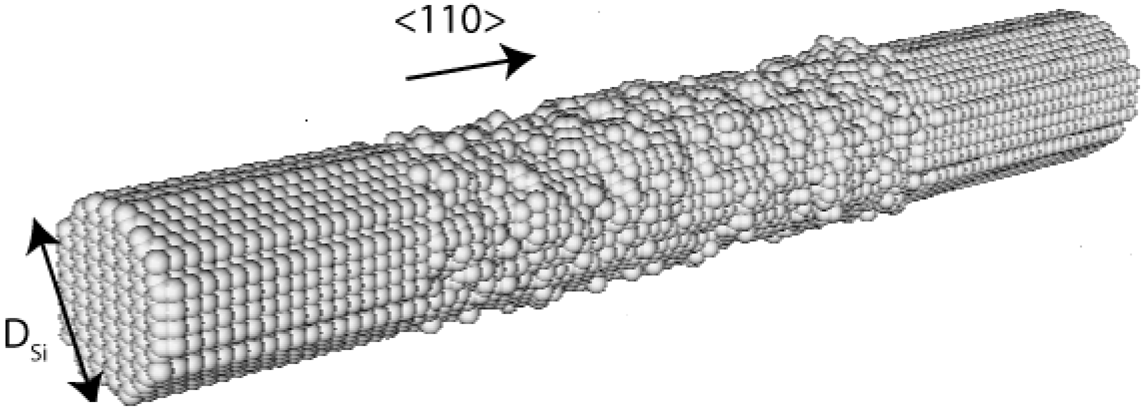
- Significant reduction of ON-current/mobility in NW with diameter less than 3 nm.
- What causes this?

Interface roughness scattering



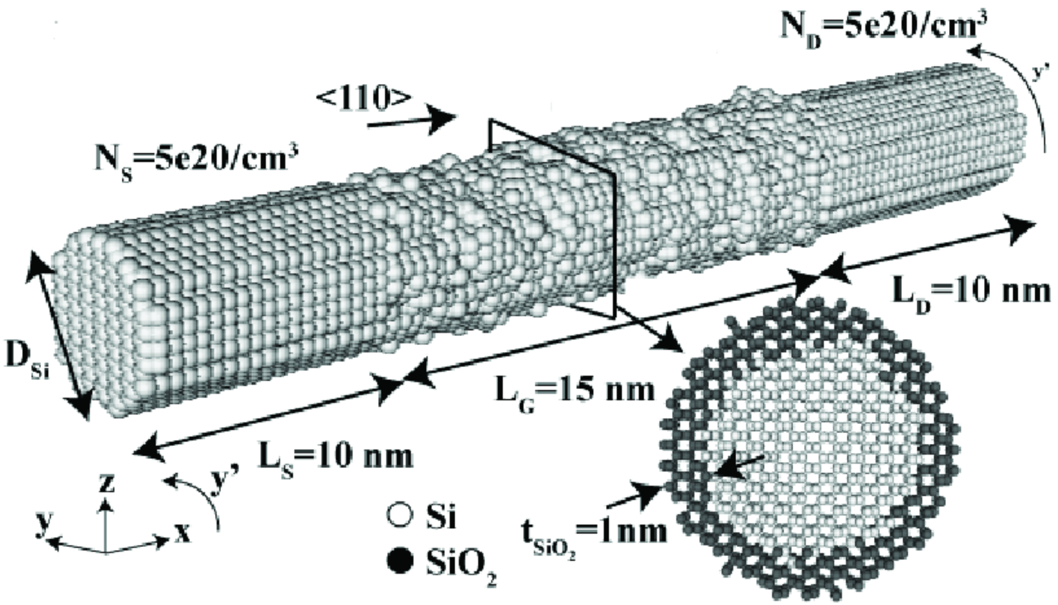
- Bandstructure: tight-binding/full-band
- 3D-atomistic interface roughness
- SiO_2 included in transport
- Low/High-drain bias

Comparison with experiments



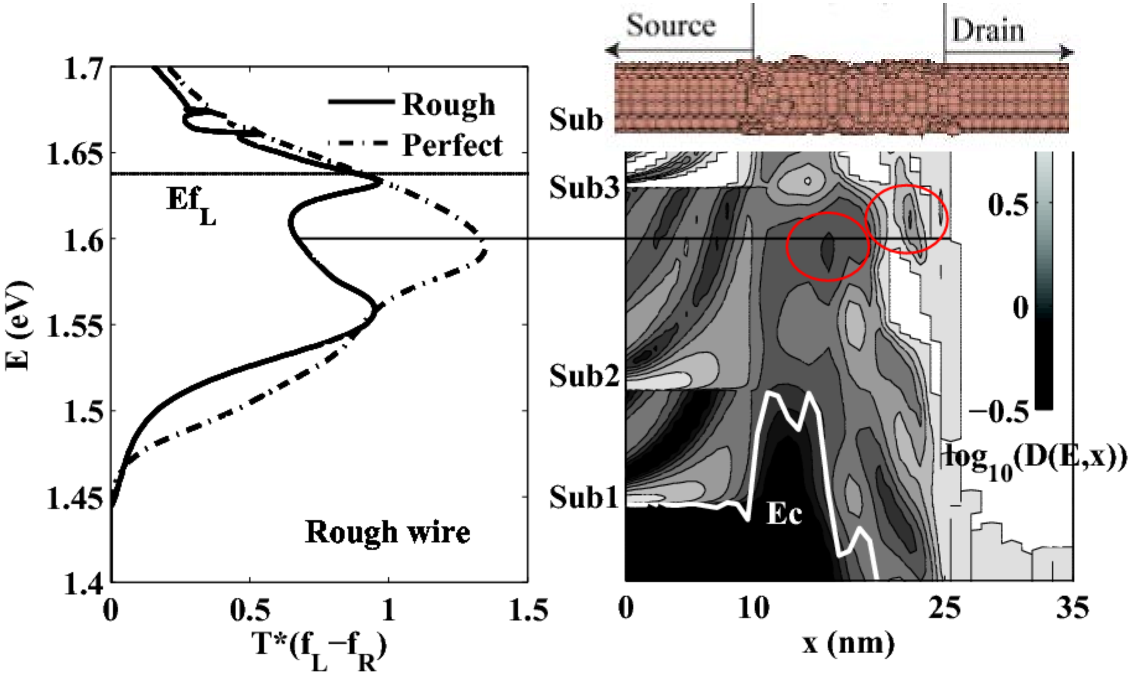
Difficulties: Interface roughness scattering

- Realistic/atomistic rough interface between Si/SiO_2
  - Adapt experimentally generated statistical function: How do we know the generated interface roughness is correct?
  - Many statistical samples needed: computational cost high
  - Electrons may penetrate into the SiO_2 region. How do we count it?
  - Computational cost increases as we take into account SiO_2 in tight-binding approximation.



Difficulties: Full band Tight-binding simulation

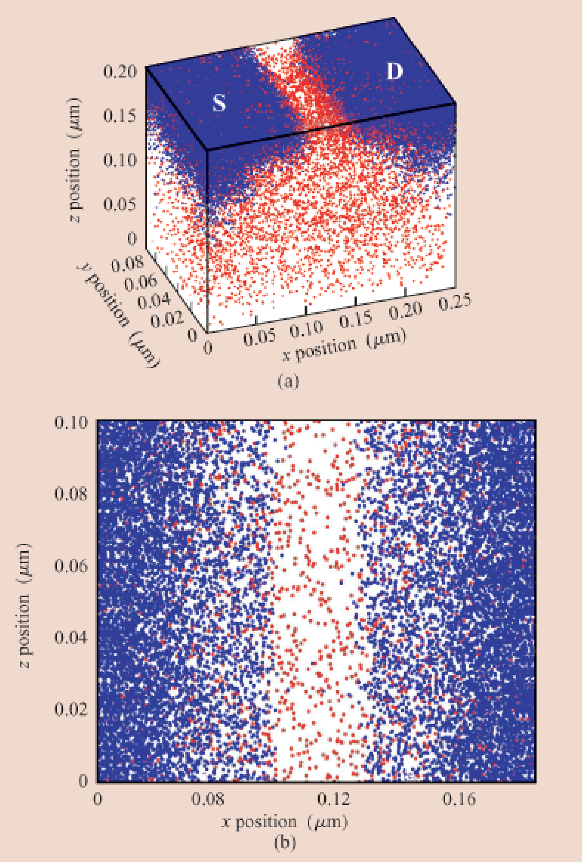
- To correctly include scattering mechanisms (interface roughness/phonon scattering) <110> NW
  - » Beyond the effective mass approximation, full band tight-binding simulation is needed: computational cost is higher
    - ✓ Effective mass cannot understand non-parabolicity/anisotropy in the bandstructure of <110> oriented NW
    - ✓ At high drain/gate bias drain side of the channel, higher subbands are mixing and influence the scattering



Variability in Vth at Low Doping

$$V_{th} = 2\phi_F - \frac{Q_B}{C_{ox}} = 2\phi_F - \frac{qN_DW_T}{C_{ox}}$$

$$\sigma_{V_T} = 3.19 \times 10^{-8}\left(\frac{t_{ox}N_A^{0.4}}{\sqrt{L_{eff}W_{eff}}}[V]\right),$$



Variation of V_T in short channel devices

Stronger effect of dopant number fluctuations on V_T

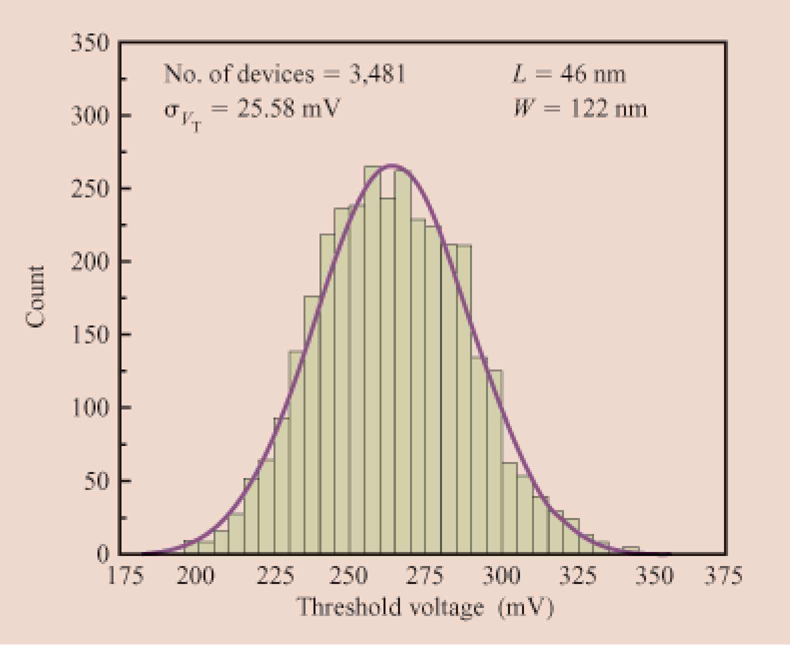


Figure 2

Threshold voltage histogram for FETs in the 90-nm-technology node.

IBM Journal of Res. And Tech. 2003.

Variability in Threshold Voltage

$$V_{th} = 2\phi_F - \frac{Q_B}{C_{ox}} = 2\phi_F - \frac{qN_A W_T}{C_{ox}}$$

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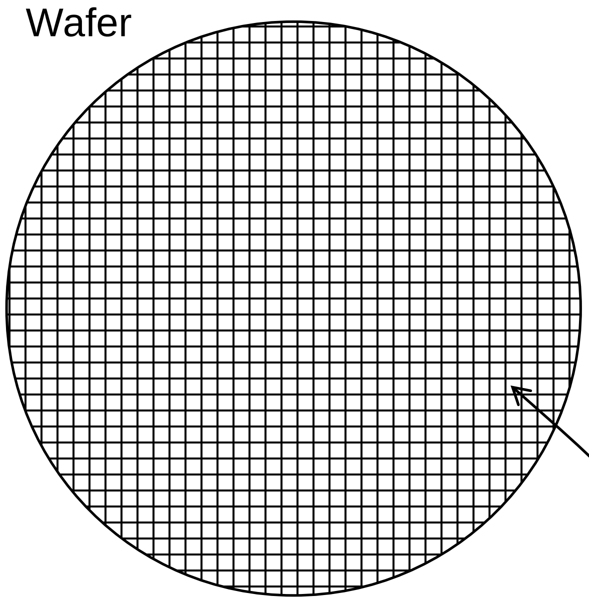
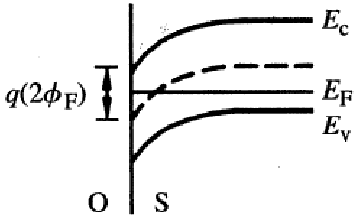


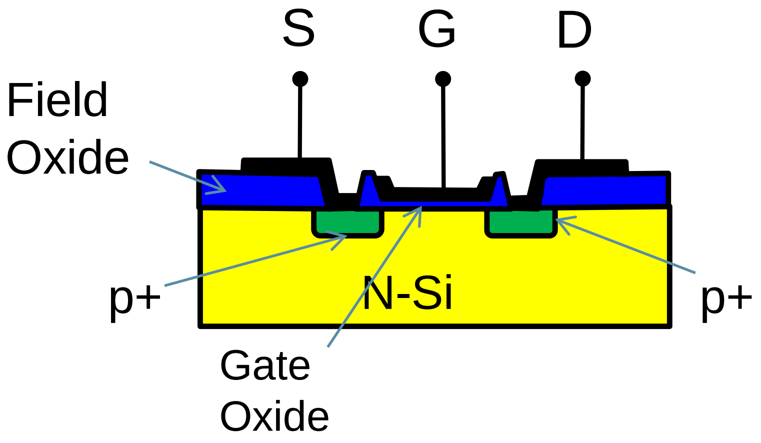
$$I_D = \frac{\mu C_{ox}}{L_{ch}} (V_G - V_{th}^{*})^2$$

If every transistor has different V_{th} and therefore different current, circuit design becomes difficult

V_{th} control by Substrate Bias

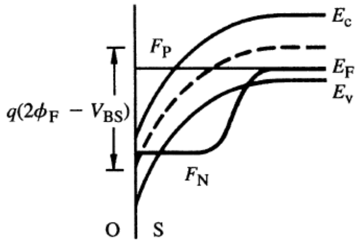
$$V_{th} = \psi_s - \frac{Q_B}{C_{ox}} = \psi_s + B\sqrt{\psi_s}$$

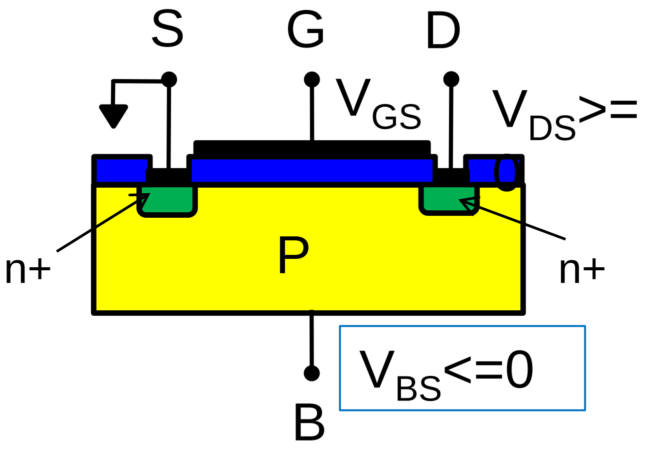




$$\psi_s = 2\phi_F$$

Control channel inversion voltage through back gate bias



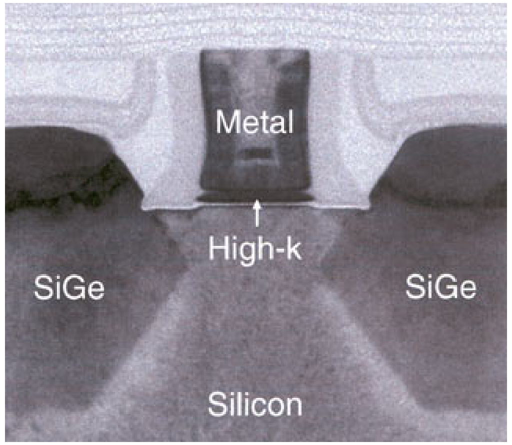


$$\psi_s = 2\phi_F - V_{BS}$$

Tune V_T through back gate bias V_{BS}

V_{th} control by Metal Work-function

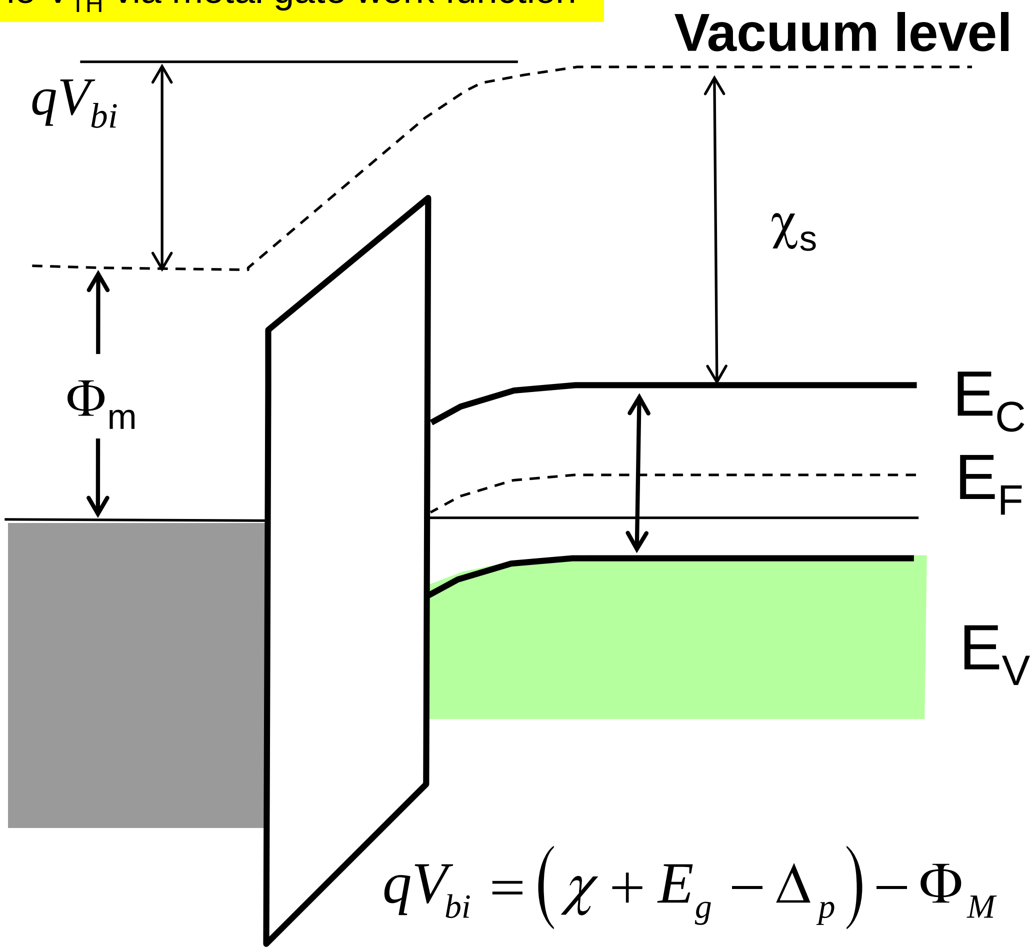
High-k/metal gate MOSFET



$$Q_i = C_{ox}(V_G - V_{th})$$

$$V_{th} = -V_{FB} + \psi_s - \frac{Q_B}{C_{ox}}$$

Tune V_{TH} via metal gate work function



$$qV_{bi} = \left(\chi + E_g - \Delta_p\right) - \Phi_M$$

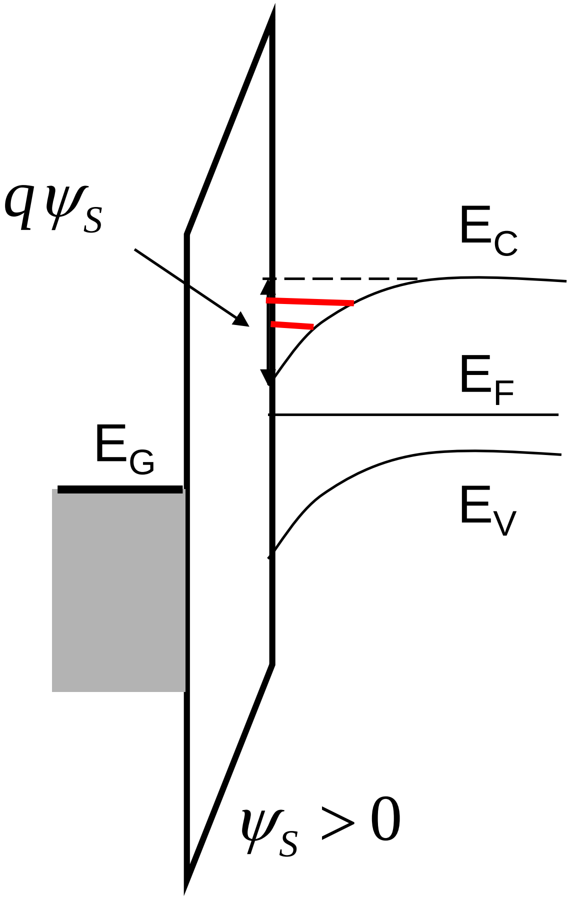
$$= qV_{FB}$$

Quantization in Inversion
“Exact” solution is not really exact ...

$$\left.\frac{d^2\psi}{dx^2}\right| = \frac{-q}{\varepsilon}\left[p(x) - n(x)\left|\psi(x)\right|^2 + N_D^+ - N_A^-\right]$$

$\downarrow$

wavefunction, not potential !



Wave function should be accounted for

Bandgap widening near the interface must also should be accounted for.

Assumption of nondegeneracy may not always be valid

“Exact” solution is not really exact … really

R. Bowen, Chenjing Fernando, Gerhard Klimeck, Amitava Chatterjee, Daniel Blanks, Roger Lake, J. Hu, Joseph Davis, M. Kularni, Sunil Hattangady, I.C. Chen,
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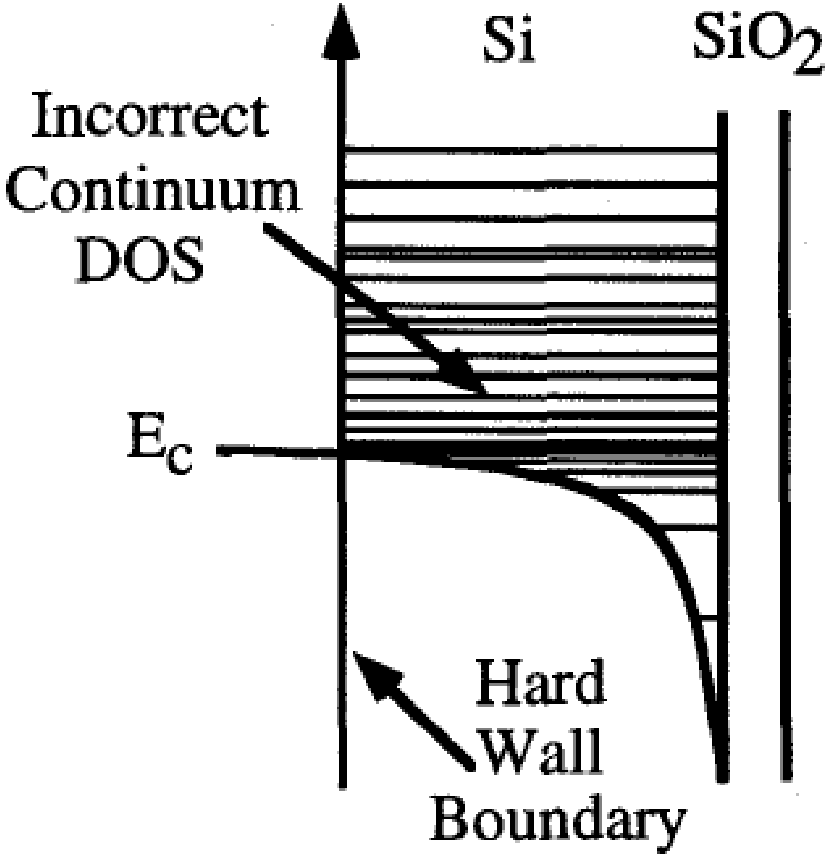
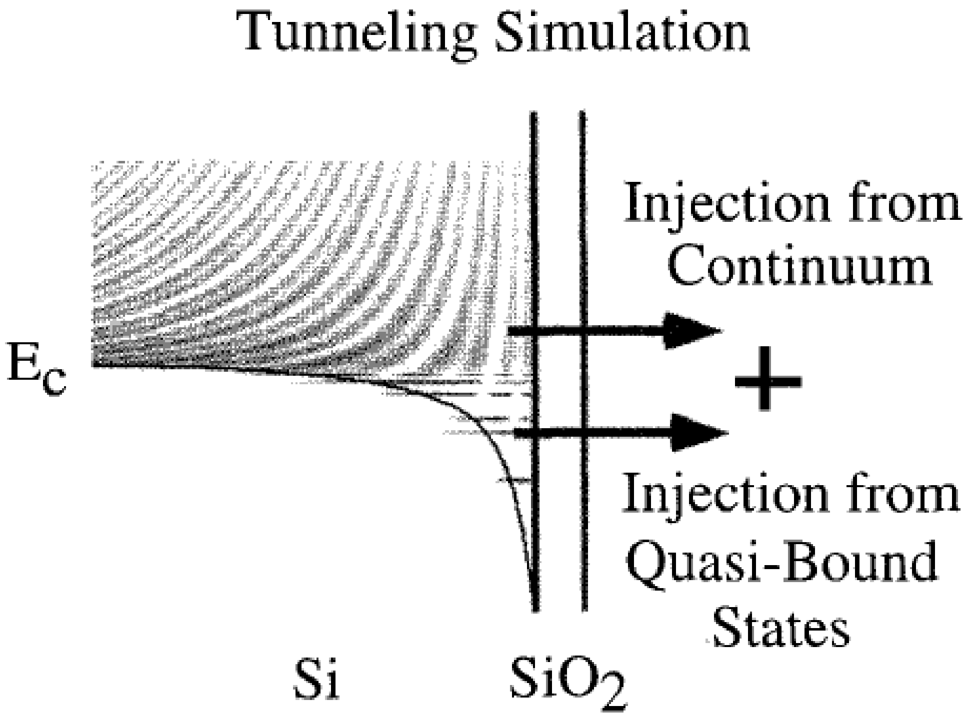
Proceedings of IEDM 1997, IEEE, 869 (1997);doi : 10.1109/IEDM.1997.650518, Cited by 42





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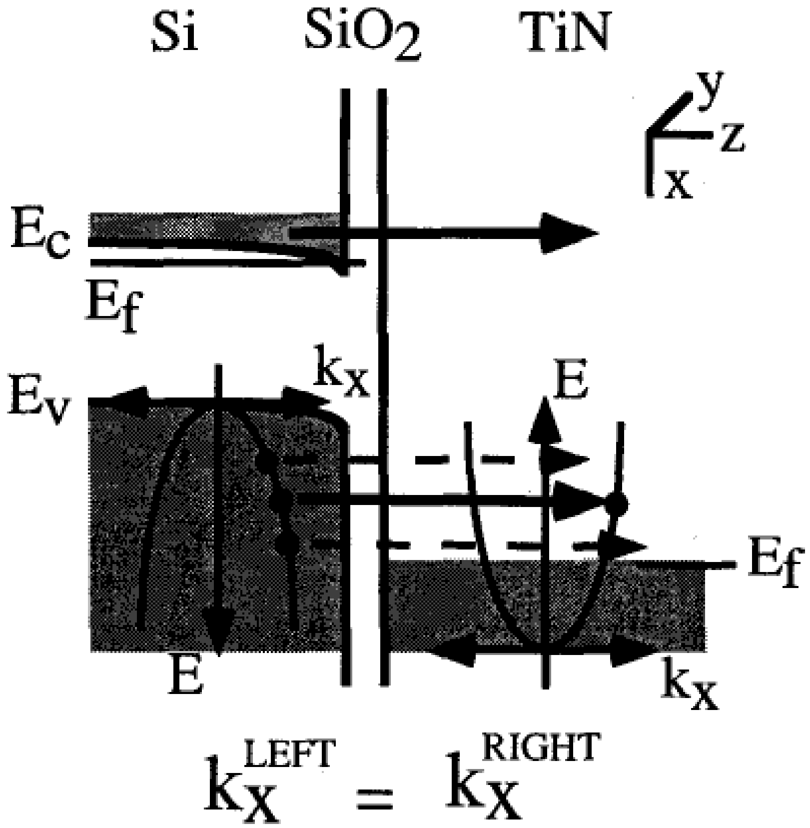

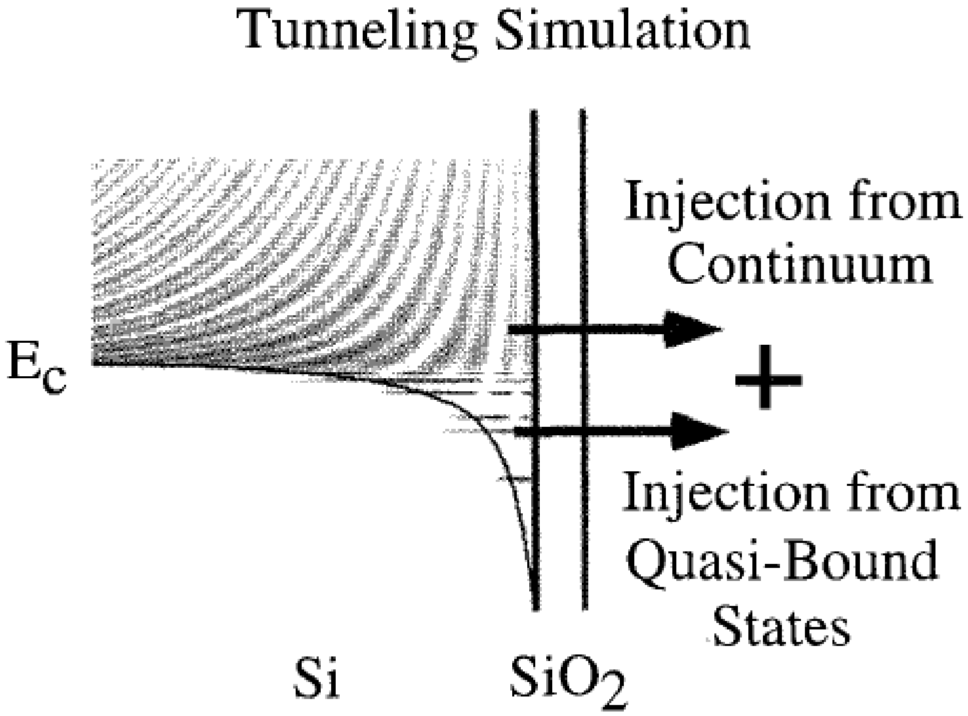

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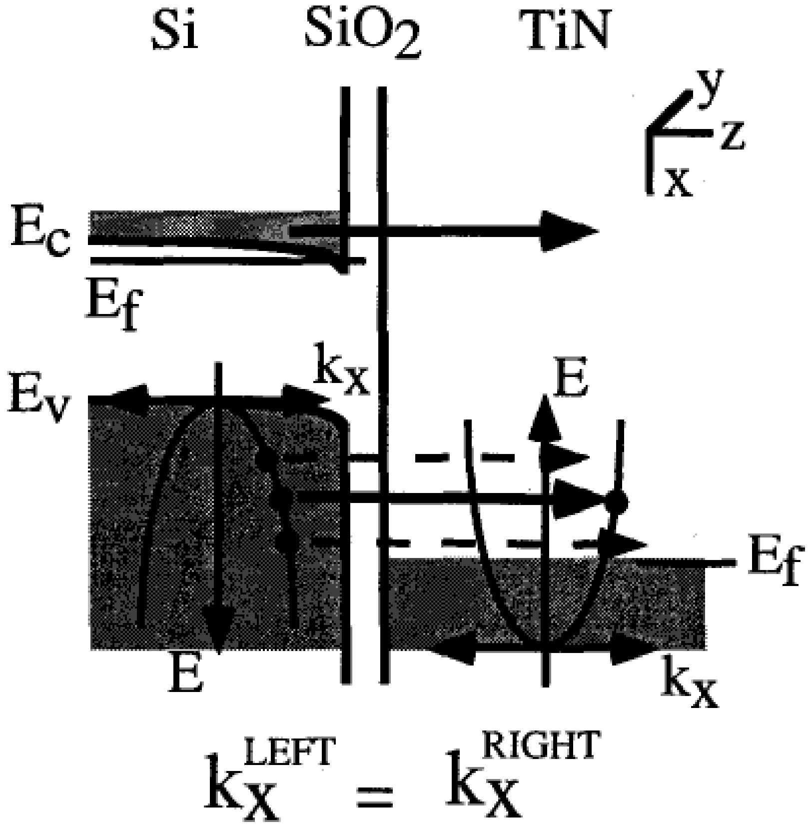
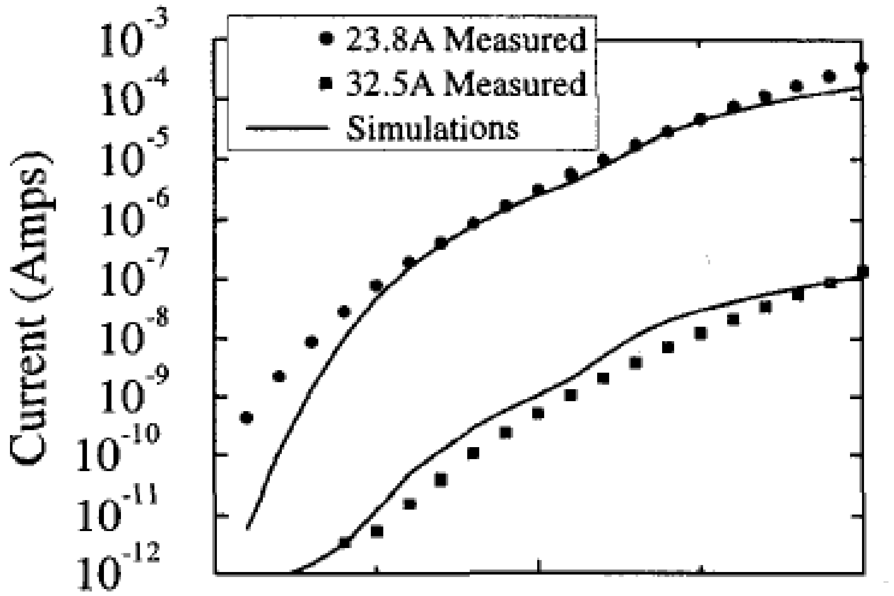
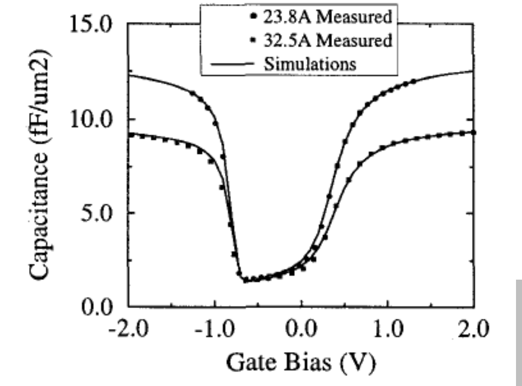


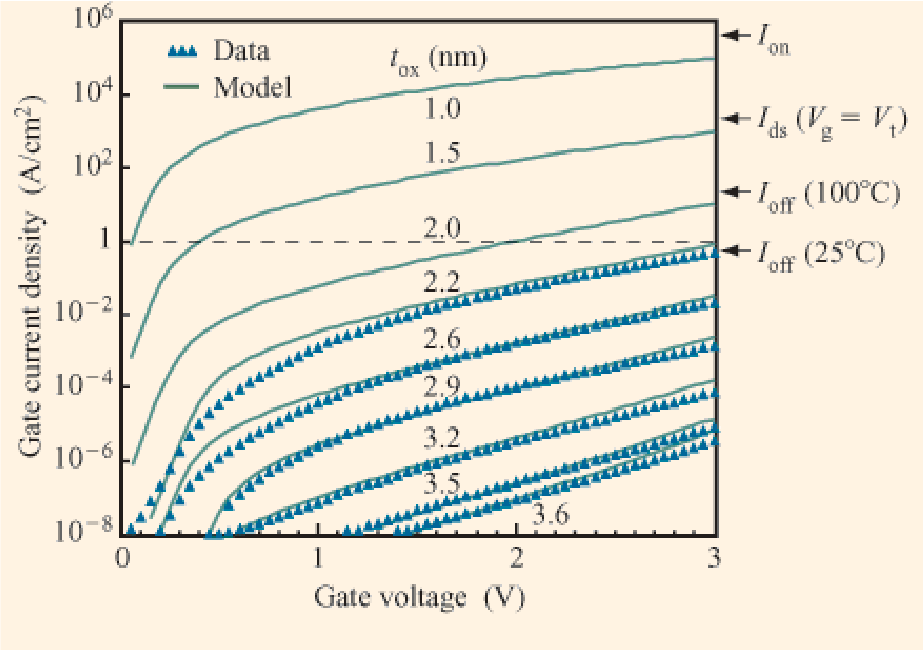


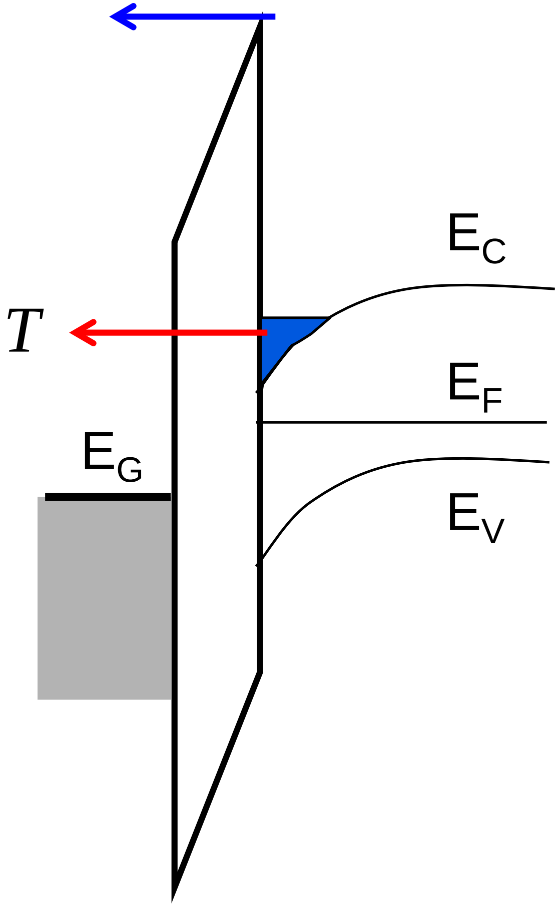


Tunneling Current

Don’t make oxides too thin → tunneling!

$$J_T = \left[Q_i(V_G) - \frac{n_i^2}{N_A} e^{-qV_G \beta} \right] \upsilon_{th} \langle T(E) \rangle$$



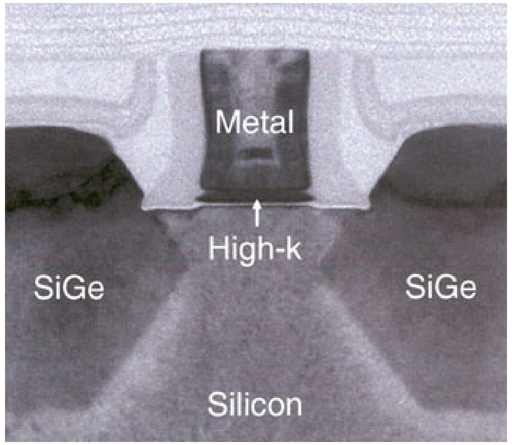


How to make Vth Roll-off small …

$$L_{\min} = \frac{qN_A W_T}{\dfrac{\kappa_{ox}\varepsilon_0}{x_0}} \frac{r_J}{\alpha}\left(\sqrt{1+\frac{2W_T}{r_J}}-1\right)$$

High k oxides allow for smaller L_{min} but lot of defects

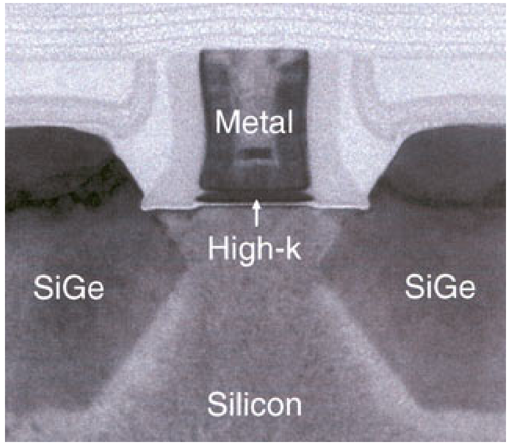
High-k/metal gate MOSFET

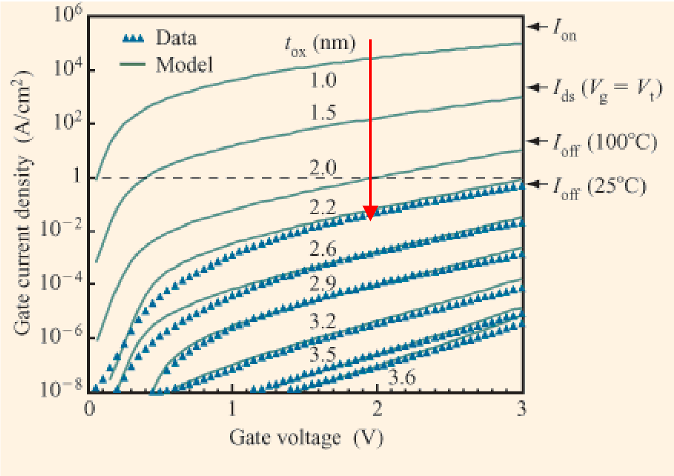


- Shallow junction and geometry of transistors
  laser annealing of junctions, FINFET
- Substrate doping NA
  consider WT and junction breakdown
- Thinner gate oxides
  consider tunneling current
- Higher gate dielectric
  consider bulk traps

Advantages of High-k Dielectric ...

High-k/metal gate MOSFET





$$L_c = \frac{qN_A W_T}{\dfrac{\kappa_{ox}\varepsilon_0}{x_0}} \frac{r_J}{\alpha}\left(\sqrt{1+\frac{2W_T}{r_J}}-1\right)$$

$$I_D = \frac{\mu C_{ox}}{L_{ch}}(V_G - V_{th}^{*})^2$$

Thicker oxide (x_0) for same capacitance …

… ensures the drive-current is not reduced
, but tunneling current is suppressed.

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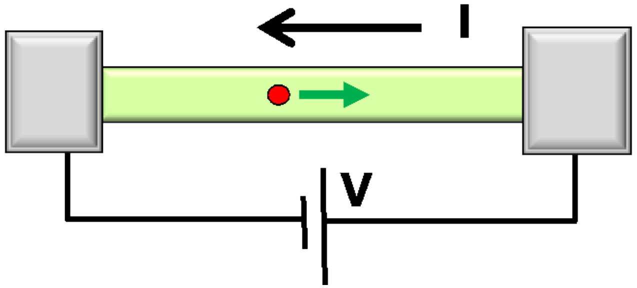

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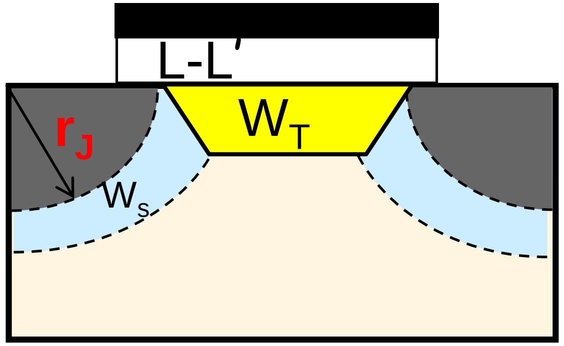

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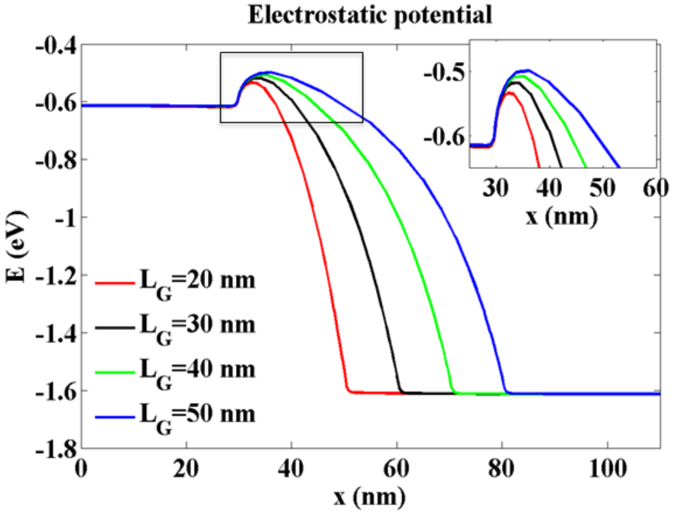

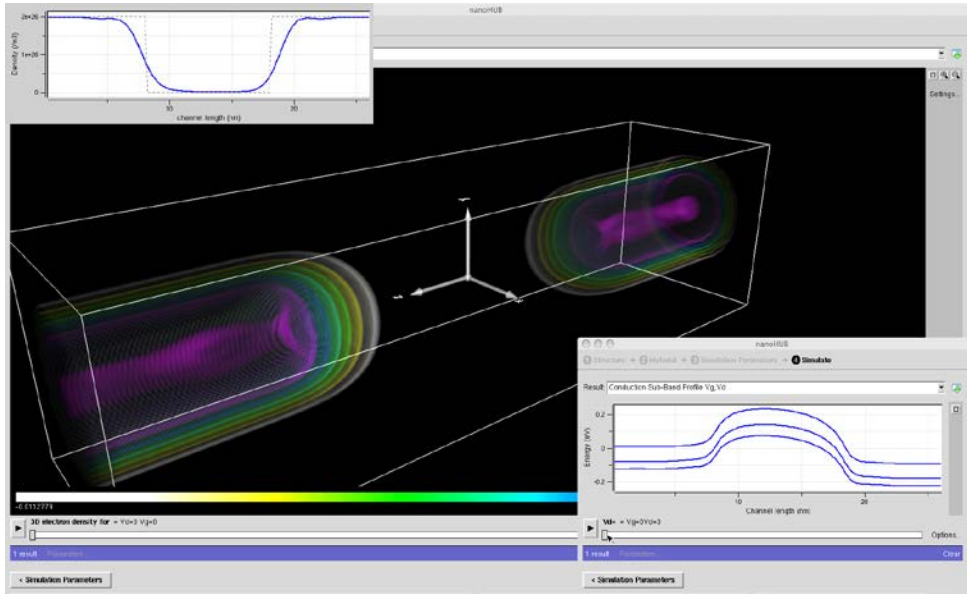

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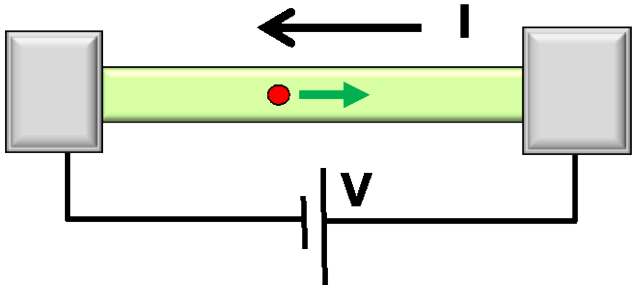

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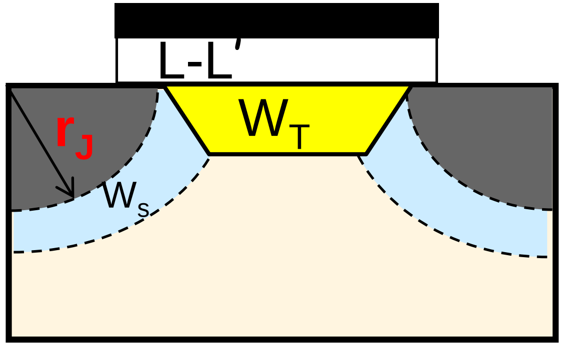

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3
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status