Section 32
Modern MOSFET

32.2 Short channel effect

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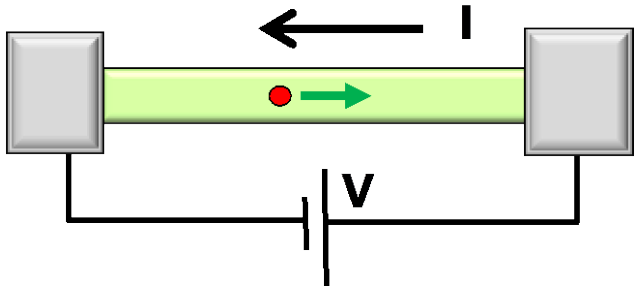
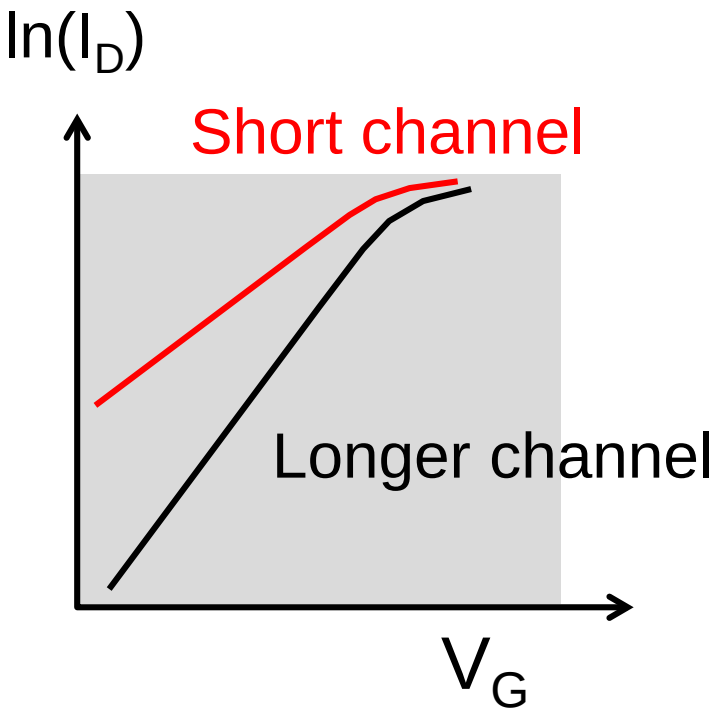
Modern MOSFET



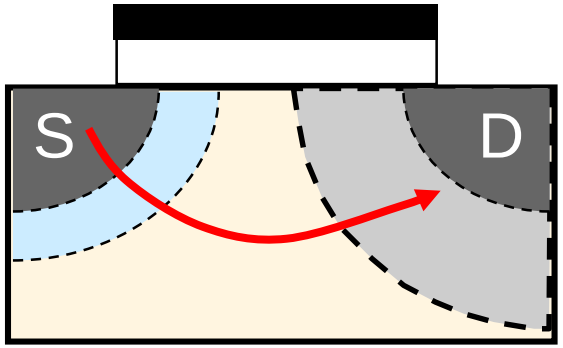
$$I = G \times V$$
$$= q \times n \times v \times A$$

charge density velocity area

status

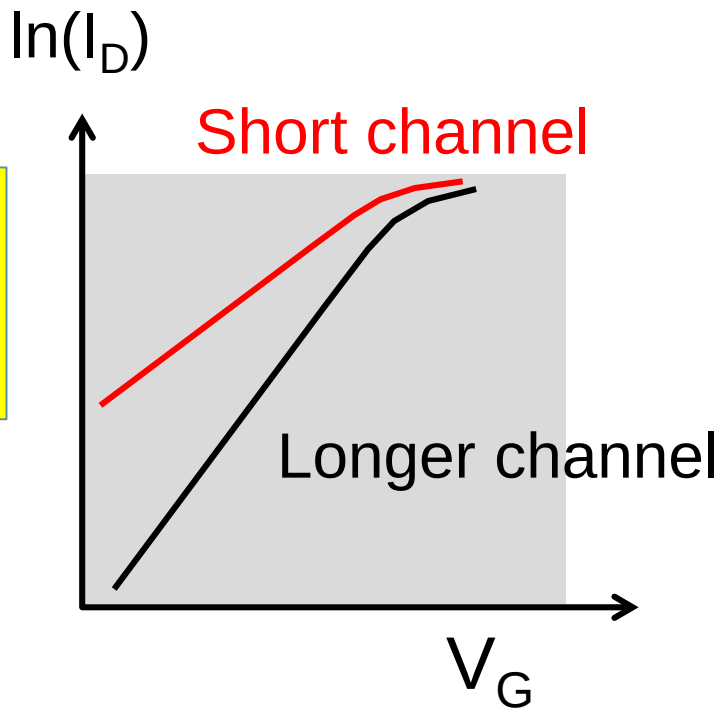


Short Channel Effect: Punch-through



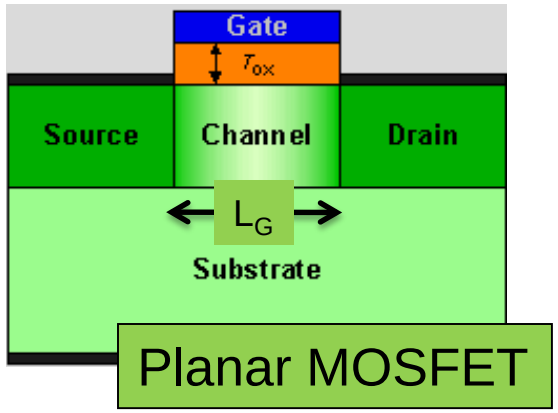
Large Drain bias can lead to “punch-through”

Gate control is weaker for short channel devices
→ slope less steep

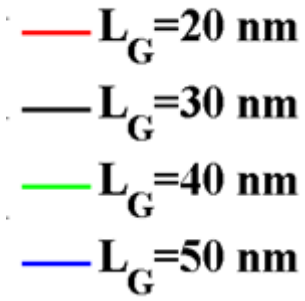


Recall similar problem with bipolar transistor

Why is the traditional MOSFET reaching its limit?

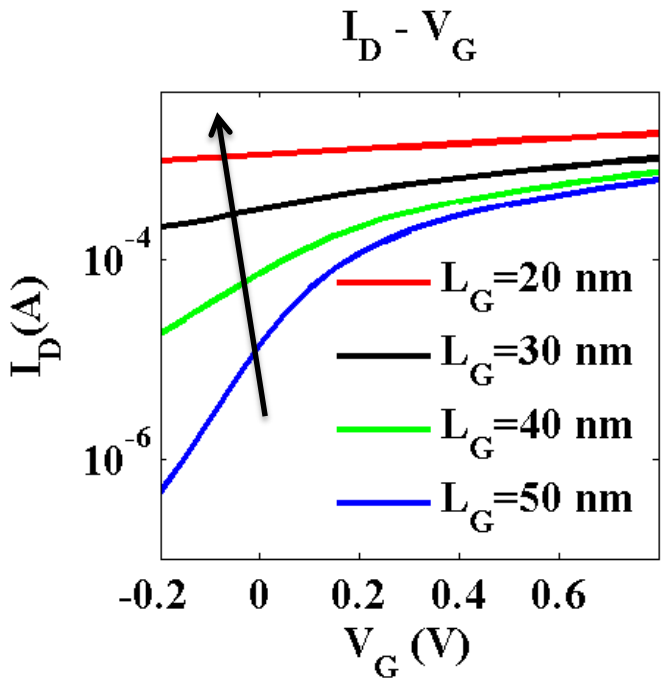


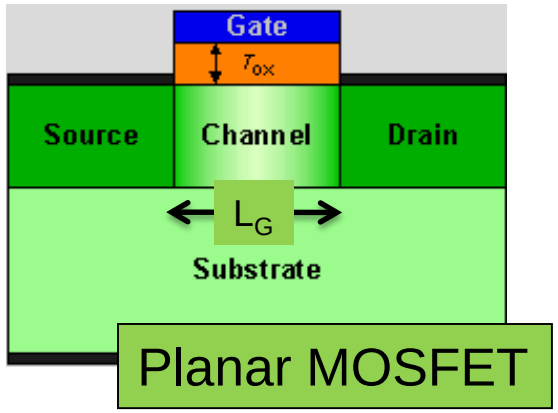
Planar MOSFET



- **https://nanohub.org/tools/mosfet**

Why is the traditional MOSFET reaching its limit?





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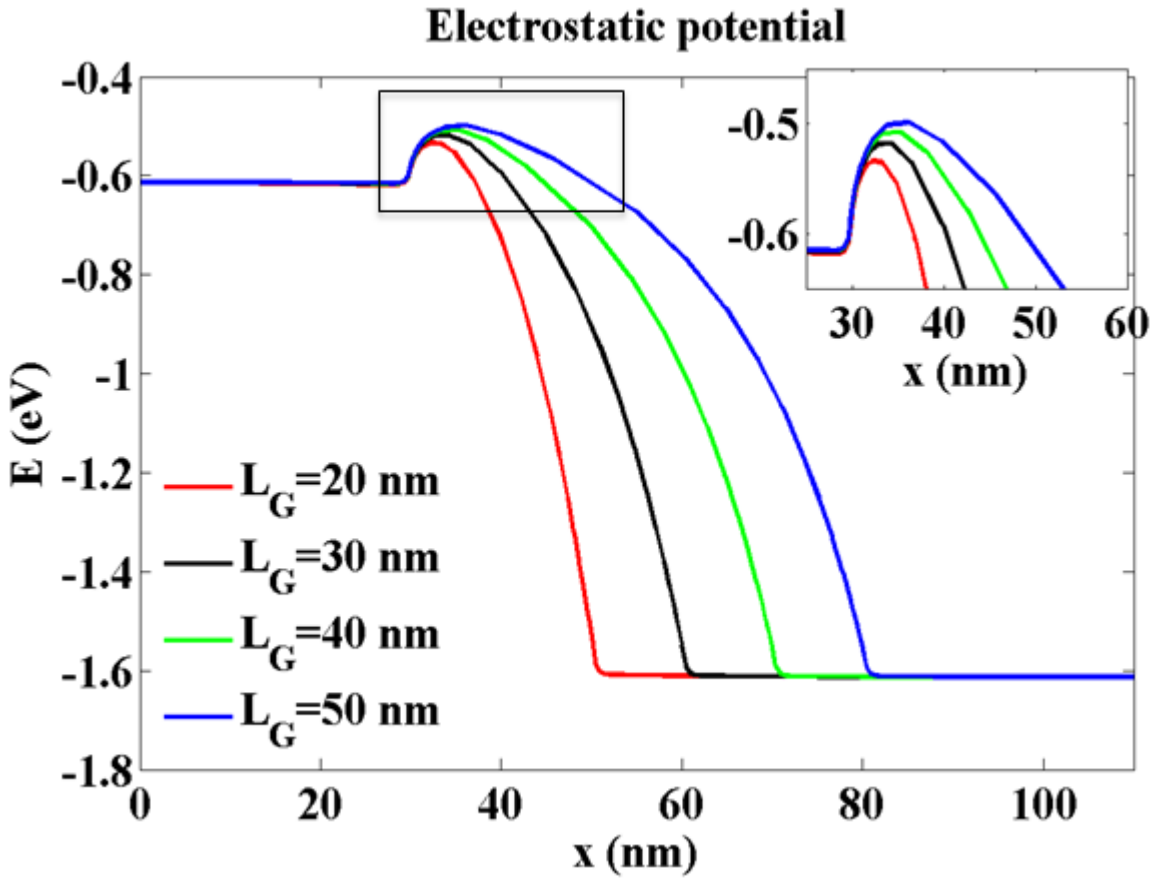

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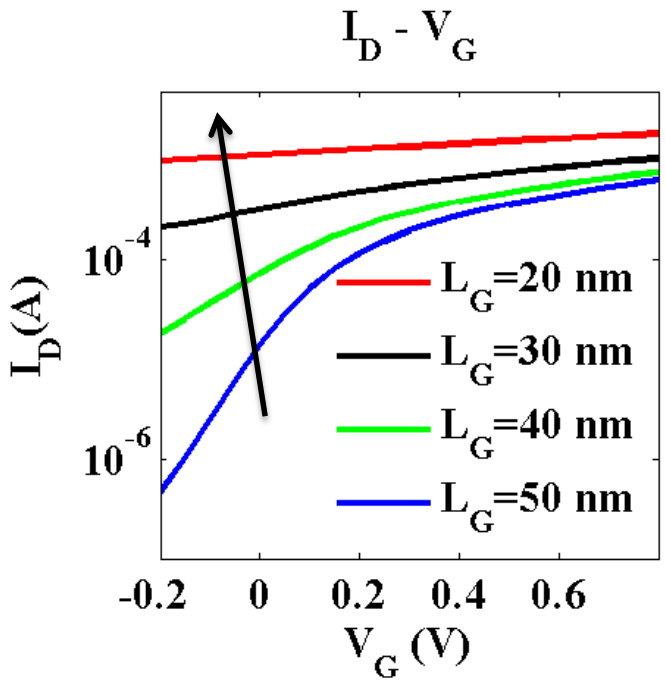
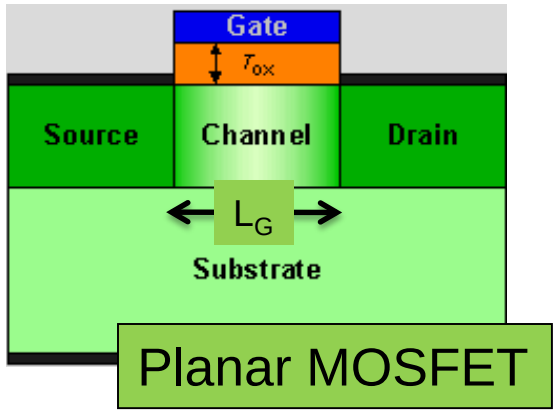
Why is the traditional MOSFET reaching its limit?





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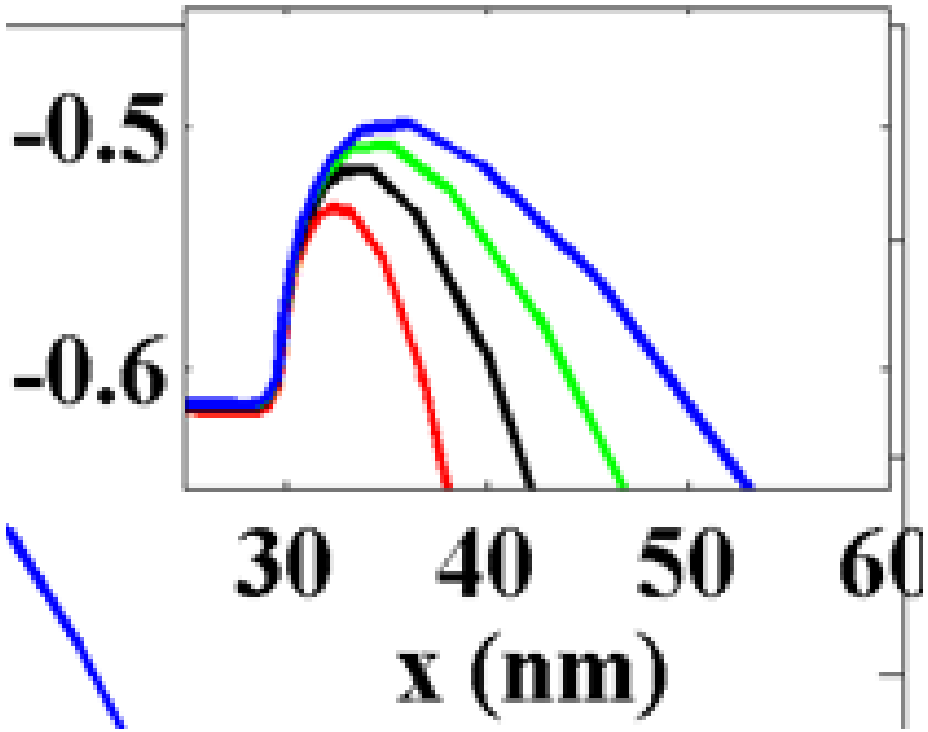
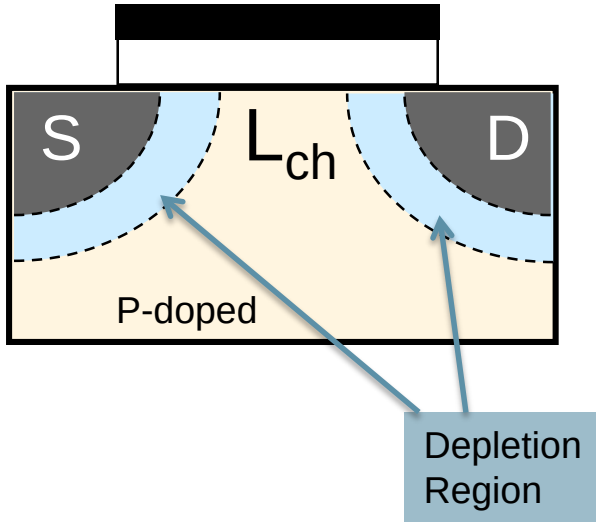


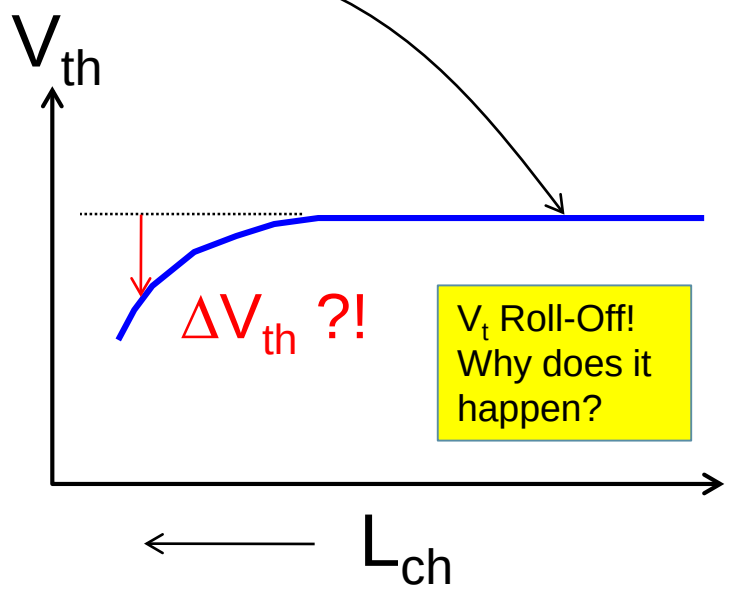
- Short channel effects:
  drain induced barrier lowering DIBL

- **https://nanohub.org/tools/mosfet**

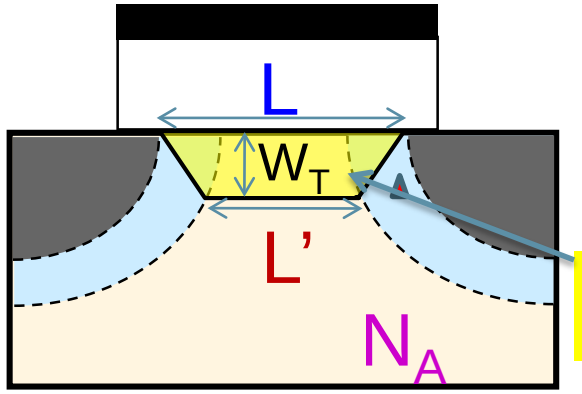
Short Channel Effect: V_{th} Roll-off

$$V_{th} = 2\phi_F - \frac{Q_B}{C_{ox}} = 2\phi_F + \frac{qN_A W_T}{C_{ox}}$$

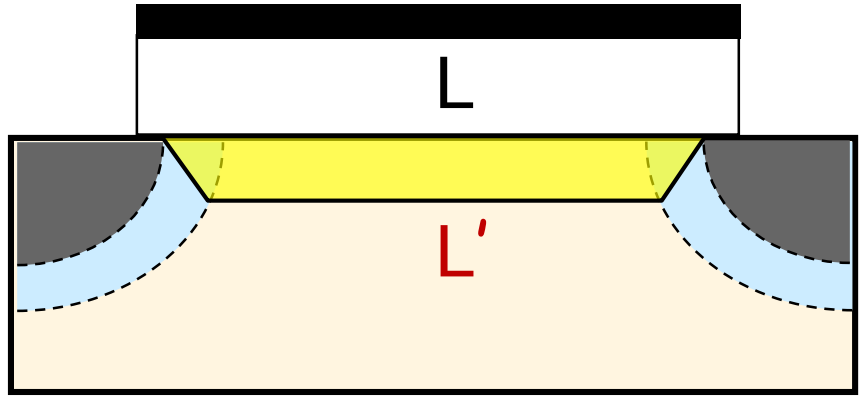




Physics of Short Channel Effect



Gate control region



$$V_{th,Short} = 2\phi_F - \frac{Q_{B,Short}}{C_{ox}}$$

$$V_{th,L} = 2\phi_F - \frac{Q_{B,Long}}{C_{ox}}$$

$$Q_{B,Short} = \frac{-qN_A \times Z \times W_T \left(\frac{L + L'}{2}\right)}{Z \times L}$$

Area of gate control region

$$= -qN_A W_T \left(\frac{L + L'}{2L}\right)$$

$$Q_{B,long} \rightarrow -qN_A W_T \quad (L \cong L')$$

For long channel

$$\Delta V_{th} = -\frac{Q_{B,Long}}{C_{ox}} + \frac{Q_{B,short}}{C_{ox}}$$

$$\Delta V_{th} = \frac{-qN_A W_T}{C_{ox}}\left[1 - \frac{L' + L}{2L}\right] \qquad \Delta V_{th} = \frac{-qN_A W_T}{C_{ox}}\frac{L - L'}{2L}$$

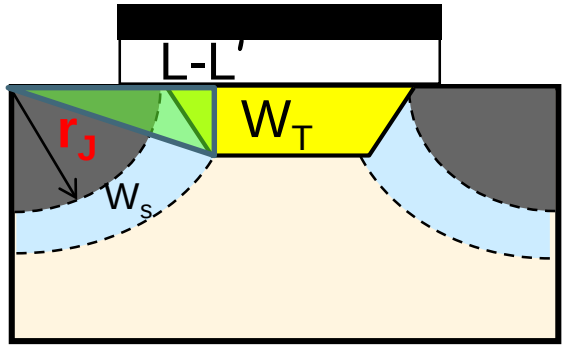
Minimize ΔV_th => Minimize L-L'

Short Channel Effect

Calculate L' (geometry exercise)

$$(r_J + W_S)^2 = W_T^2 + \left(r_J + \frac{L - L'}{2}\right)^2$$

$$\mathrm{L} - L' = 2r_J\left(\sqrt{1 + \frac{2W_T}{r_J}} - 1\right)$$



r_j junction curvature

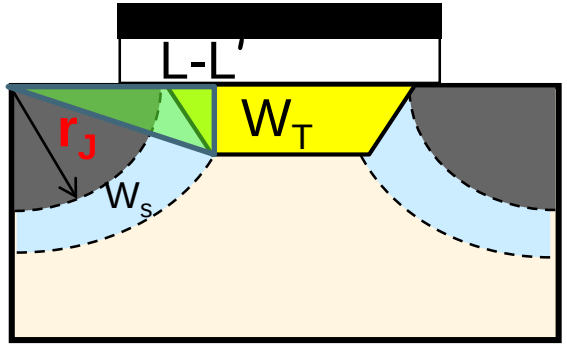
$$\Delta V_{th} = \frac{-qN_A W_T}{C_{ox}} \frac{L - L'}{2L}$$

$$\Delta V_{th} = \frac{-qN_A W_T}{C_{ox}} \frac{r_J}{L}\left(\sqrt{1 + \frac{2W_T}{r_J}} - 1\right) = \alpha_0$$ Minimum acceptable …

Minimize ΔV_th => Minimize L-L' => Minimize r_j

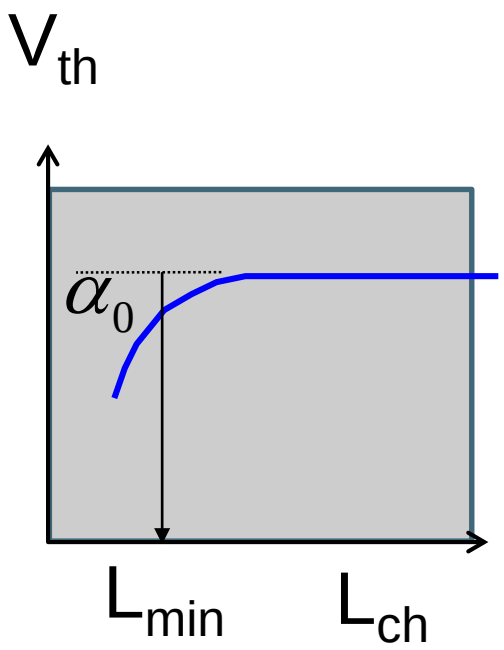
How to reduce V_{th} roll-off …

Shallow junction/geometry of transistors
laser annealing of junctions, FINFETs



Reduced substrate doping N_A
consider W_T and junction breakdown

$$\Delta V_{th} = \frac{-qN_A W_T}{C_{ox}} \frac{r_J}{L} \left(\sqrt{1 + \frac{2W_T}{r_J}} - 1 \right)$$



Thinner gate oxides
Consider tunneling current
Higher gate dielectric
Consider bulk traps

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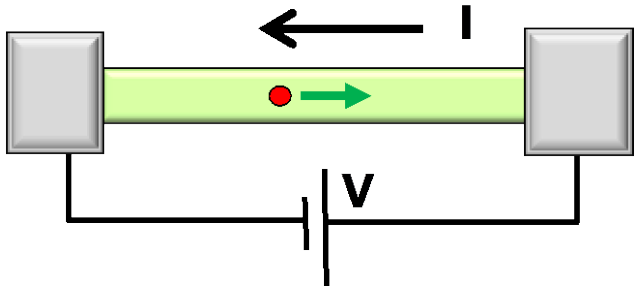

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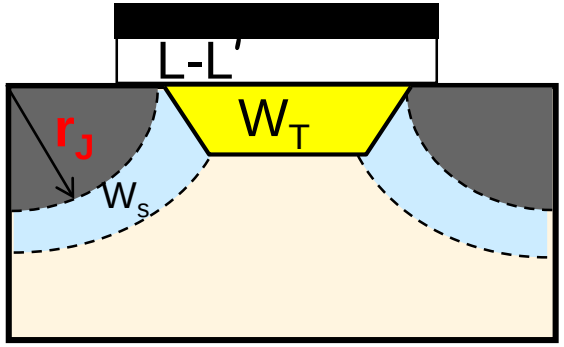
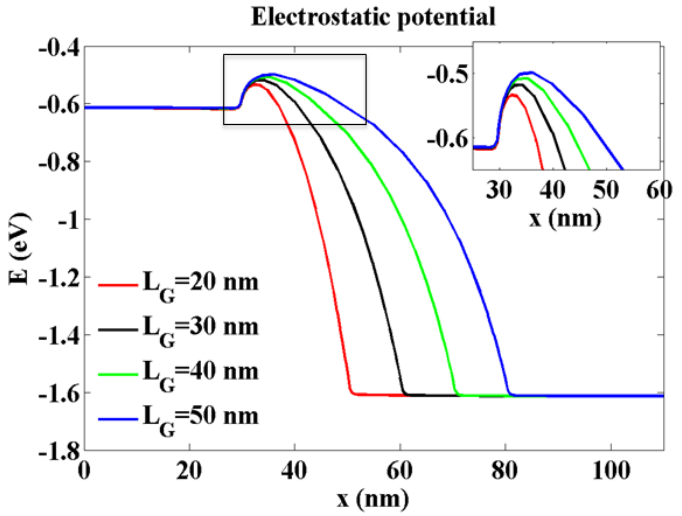


1. • 32.1 Some of Moore's Law Challenges
2. • 32.2 Short channel effect
3. • 32.3 Control of threshold voltage
4. • 32.4 Mobility enhancement

status



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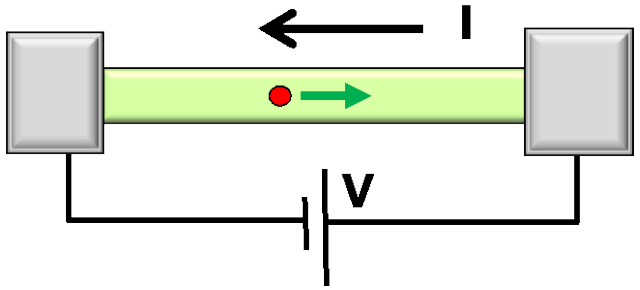

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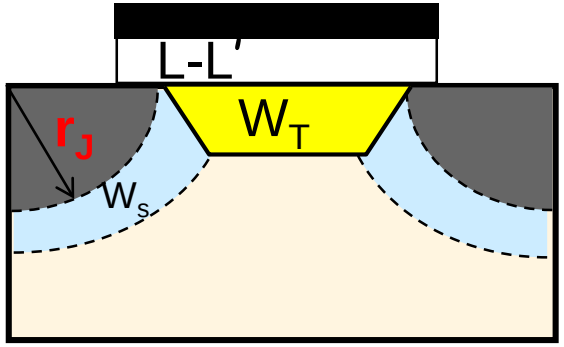

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