



Solid State Devices

Section 32

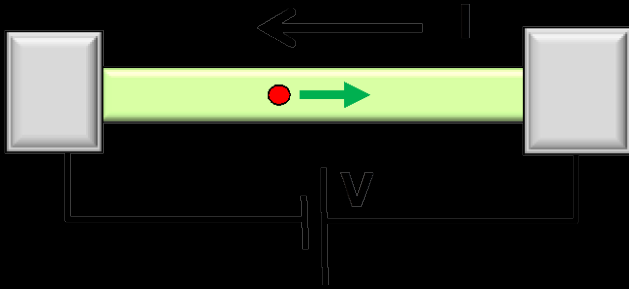
Modern MOSFET

Gerhard Klimeck
Purdue University
School of Electrical and Computer Engineering

gekco@purdue.edu



Section 32 Modern MOSFET



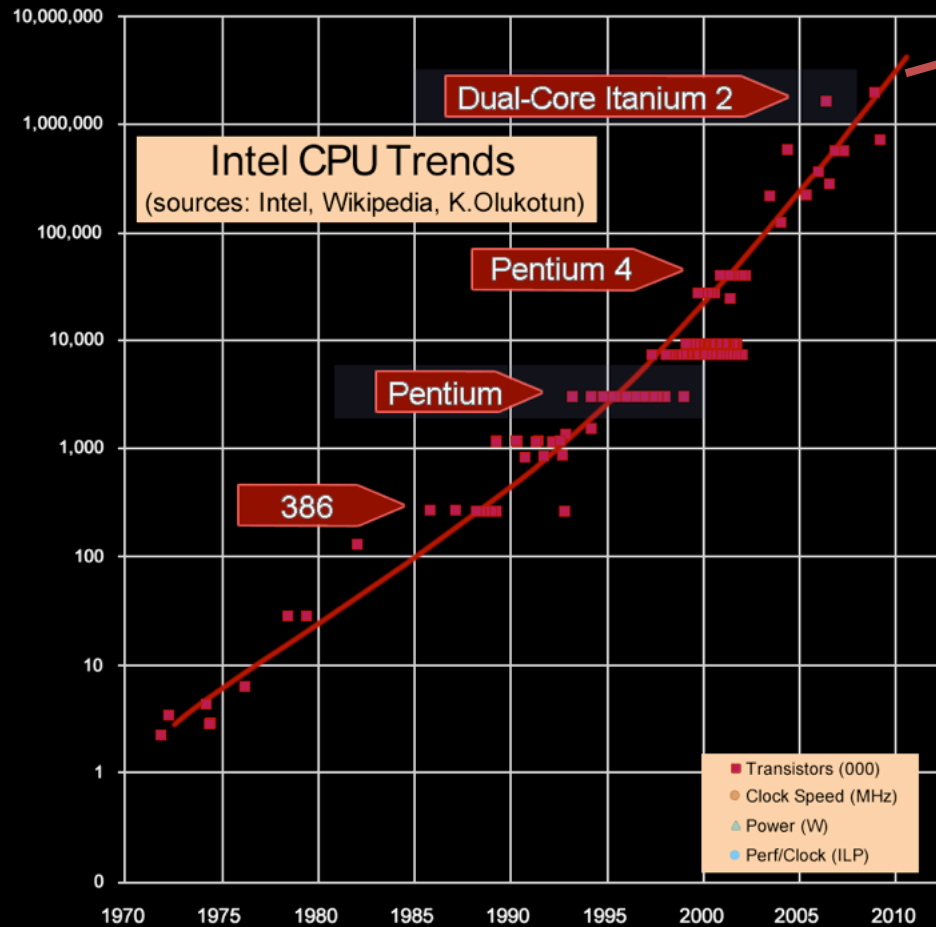
$$I = G \times V$$
$$= q \times n \times v \times A$$

charge density velocity area

- 1 • 32.1 Some of Moore's Law Challenges
- 2 • 32.2 Short channel effect
- 3 • 32.3 Control of threshold voltage
- 4 • 32.4 Mobility enhancement



Moore's Law Forever?

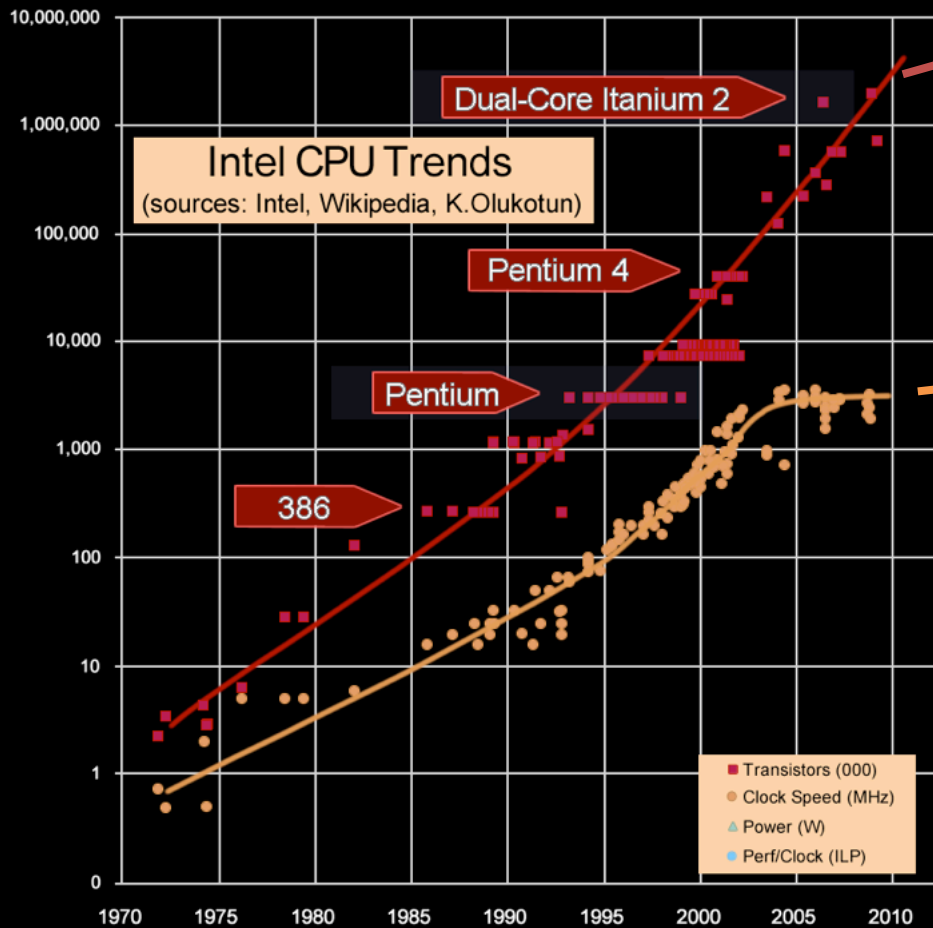


Number of transistors:
Moore's law is continuing

<http://jai-on-asp.blogspot.com>

2005: free lunch is over, updated 2009

CPU's are not getting faster!



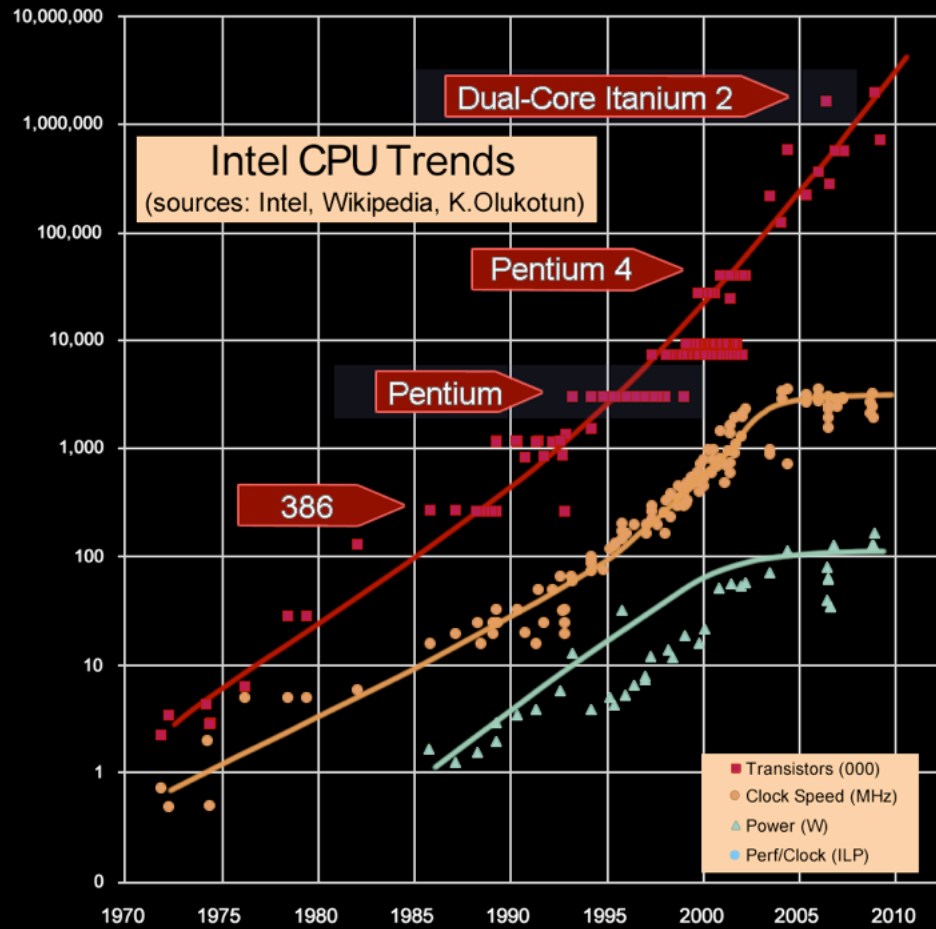
Number of transistors:
Moore's law is continuing

Clock speed:
no longer scaling

<http://jai-on-asp.blogspot.com>

© Gerhard Klimeck 2005: free lunch is over, updated 2009

Power is the Limit!



Number of transistors:
Moore's law is continuing

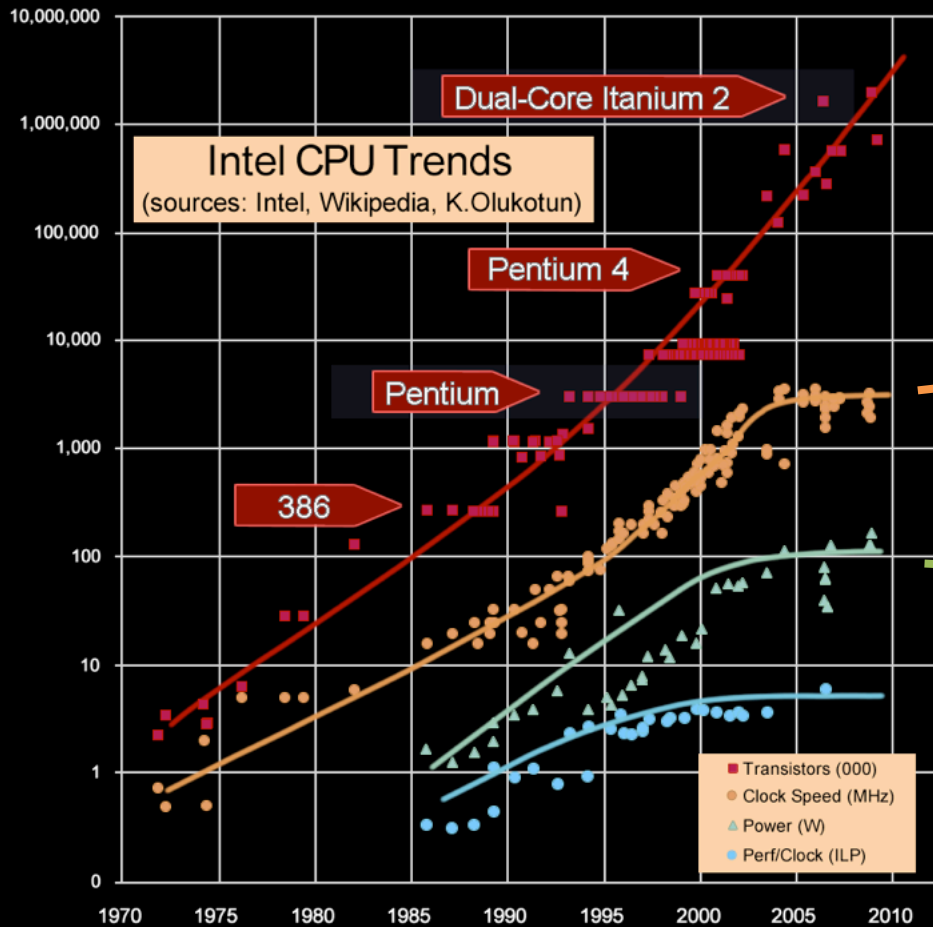
Clock speed:
no longer scaling

Power:
today's limitation
~100W

<http://jai-on-asp.blogspot.com>

2005: free lunch is over, updated 2009

Limited Performance Improvements



Number of transistors:
Moore's law is continuing

Clock speed:
no longer scaling

Power:
today's limitation
~100W

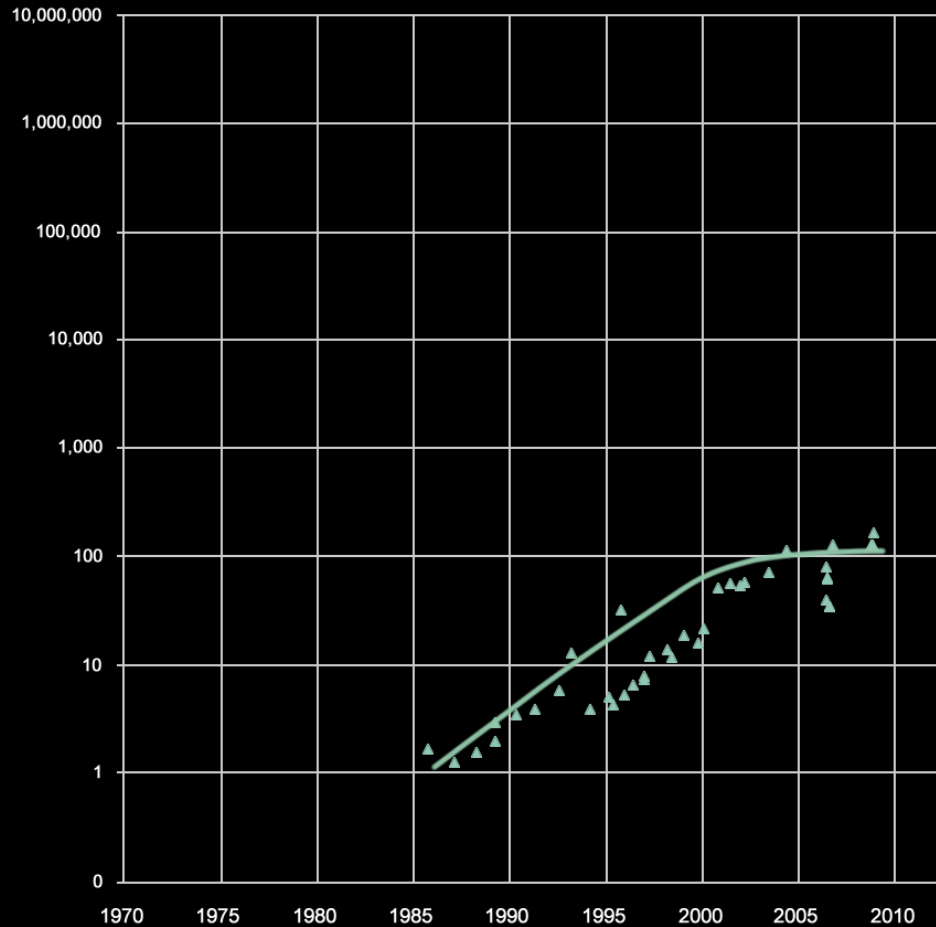
Performance Gain:
limited

Supply voltage (V_{dd}) stopped
scaling at around 2003

<http://jai-on-asp.blogspot.com>

2005: free lunch is over, updated 2009

What is Special about 100W ?



Power:
today's limitation
~100W

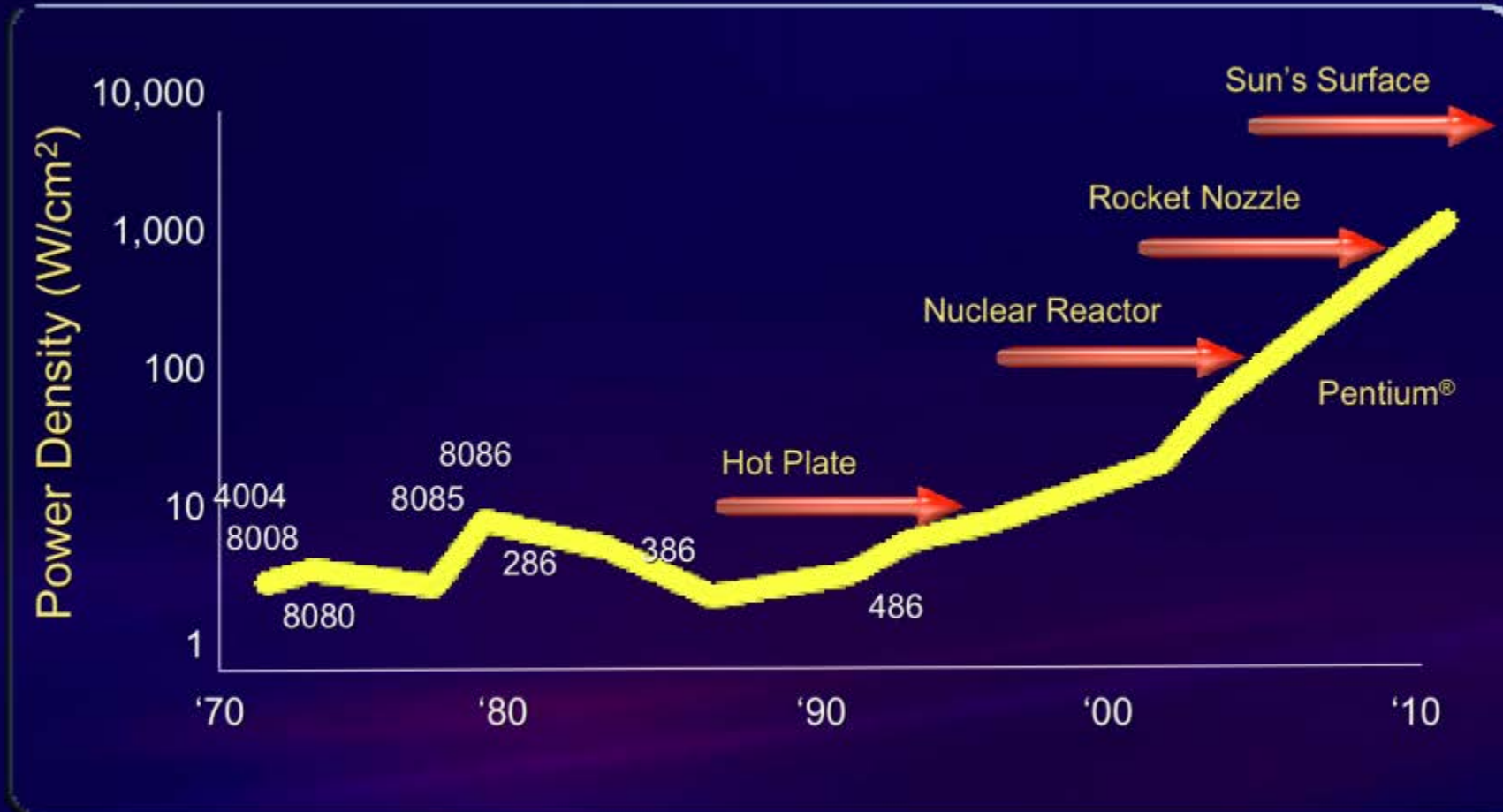
<http://jai-on-asp.blogspot.com>

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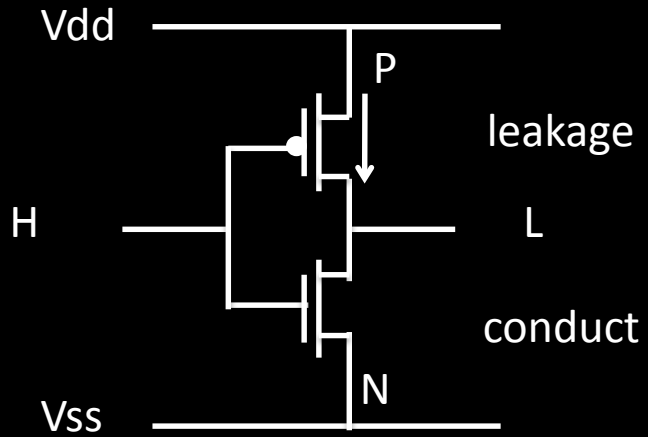
Intel (Fun) Projection from 2004

How do we burn power?

Switching Circuits & Leakage => Transistors



CMOS Inverter



Dynamic / Switching Power:

- Charging a capacitor network

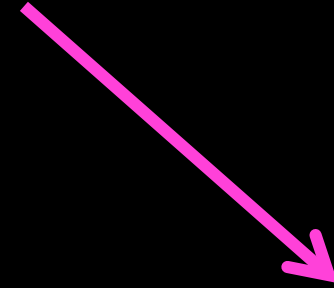
$$P \propto f C_L V_{dd}^2$$

- Reduce frequency ☹️
- Reduce capacitance
=> device size ☹️
- Reduce voltage 😊

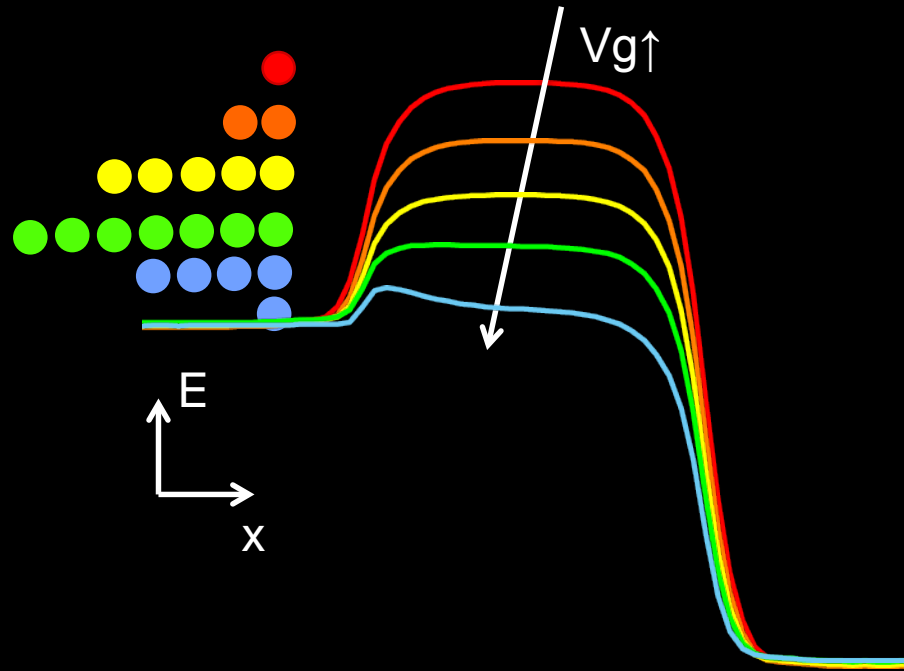
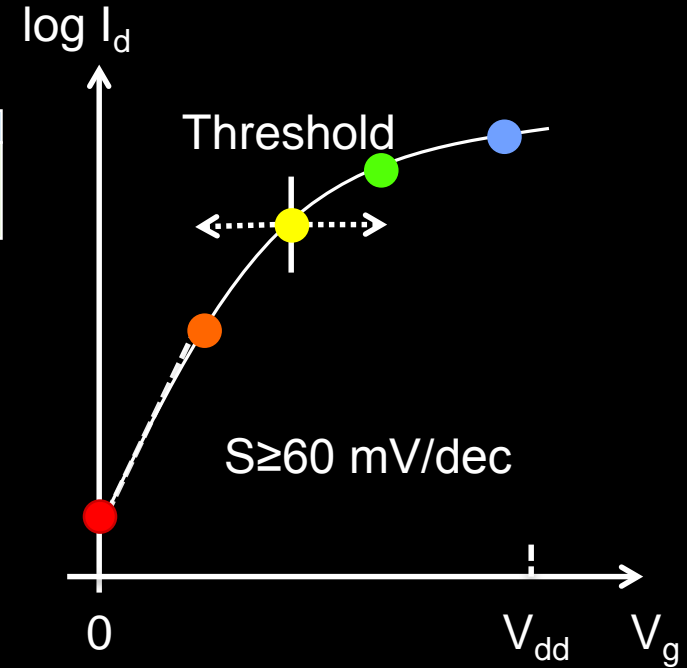
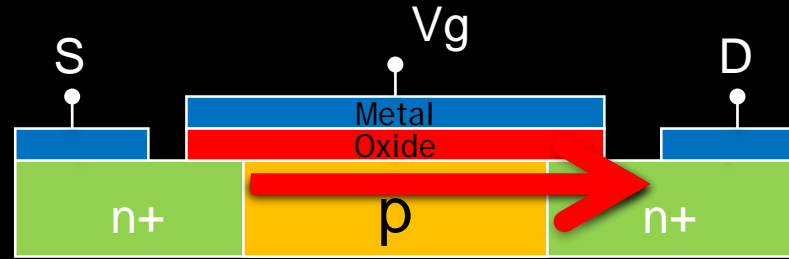
Static Power:

- Leakage through transistors

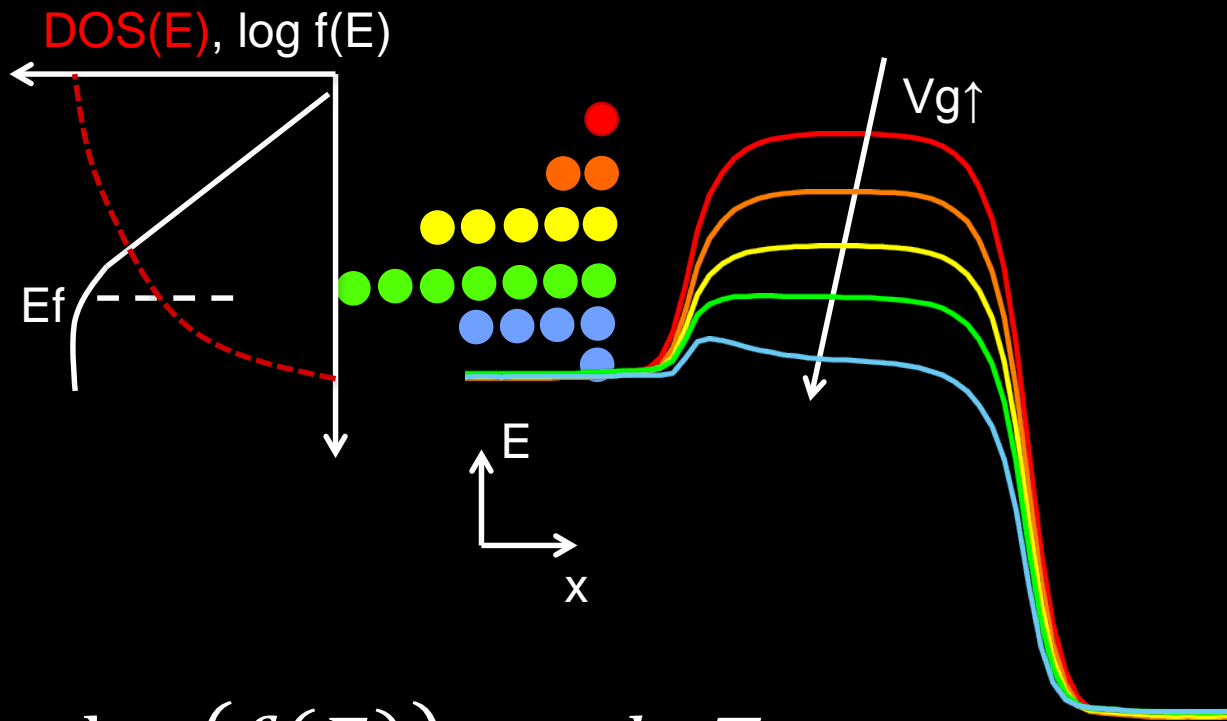
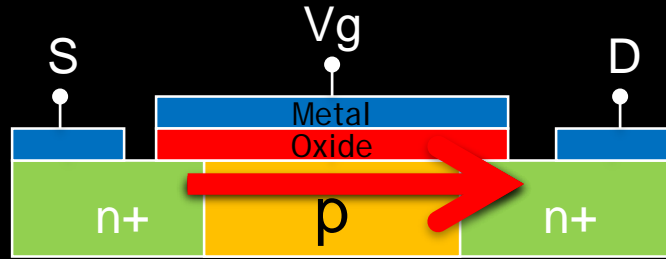
$$P \propto I_{OFF} \propto 1/\exp(V_{dd}) \quad \text{☹️}$$



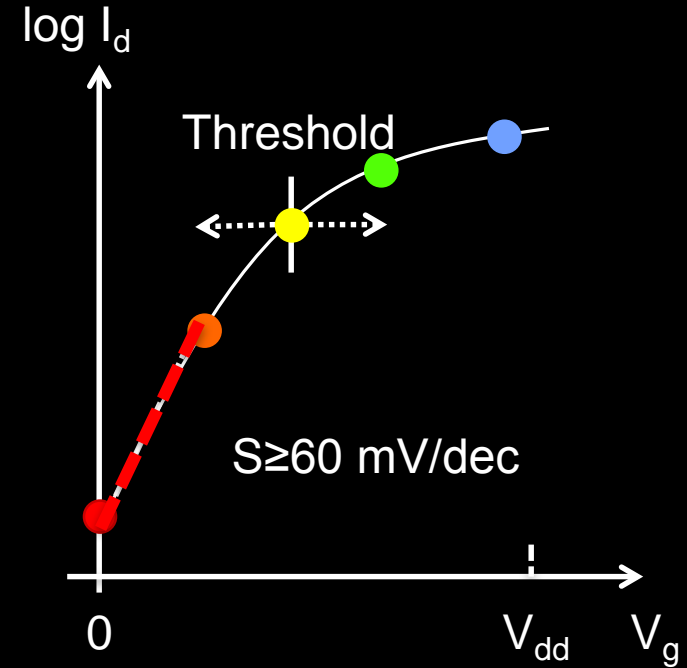
"Fundamental" Limit



"Fundamental" Limit



$$\log(f(E)) \propto -k_B T$$



$$S = 2.3m \left(\frac{k_B T}{q} \right) \frac{\text{mV}}{\text{dec}}$$

$$m = \left(1 + \frac{C_D}{C_{OX}} \right) \geq 1$$

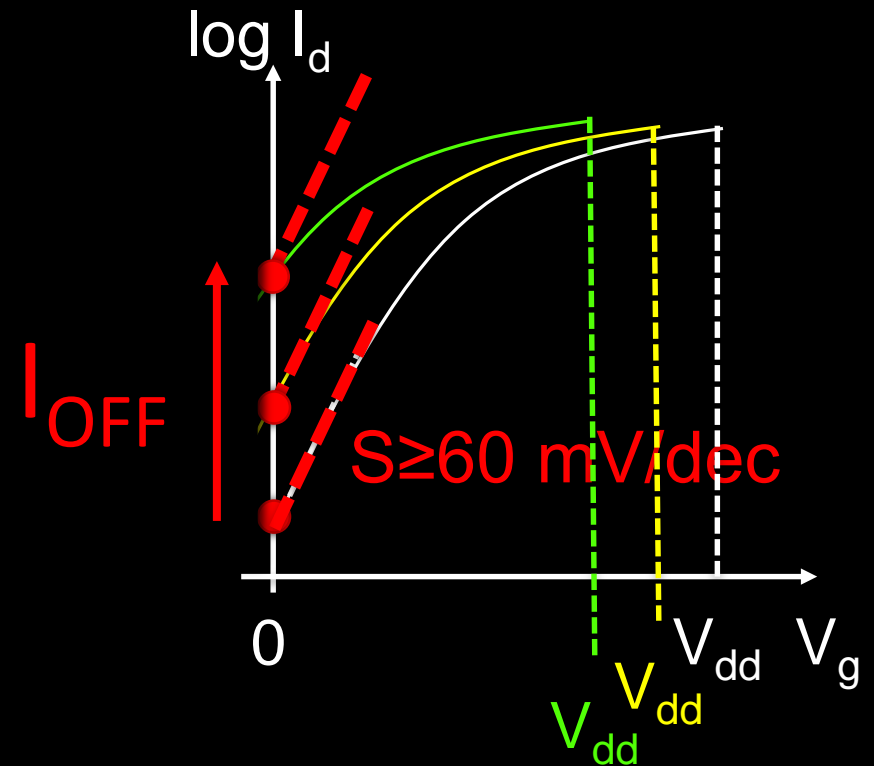
Device Scaling for Performance

Dynamic / Switching Power:

- Charging a capacitor network

$$P \propto f C_L V_{dd}^2$$

- Reduce supply voltage

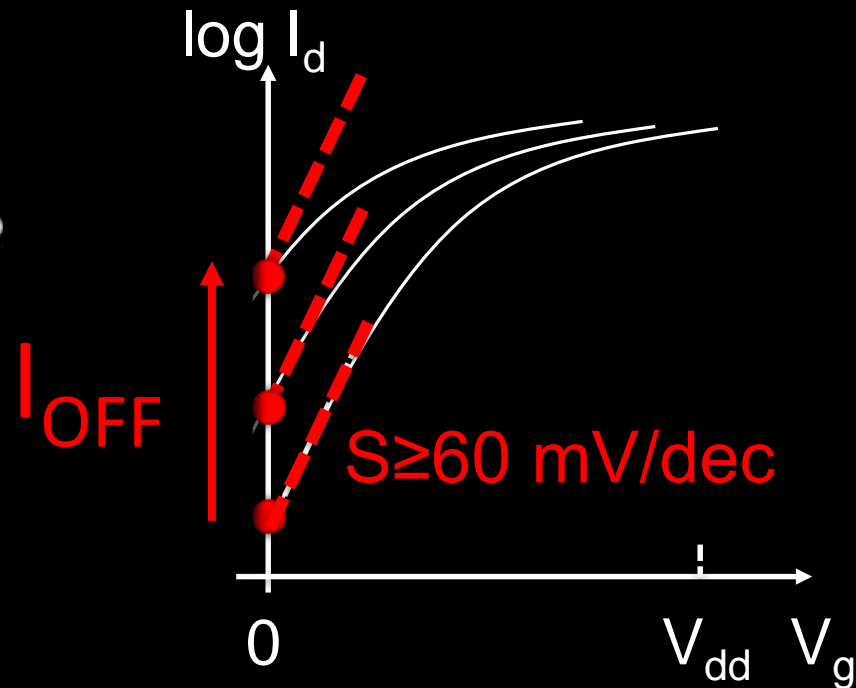
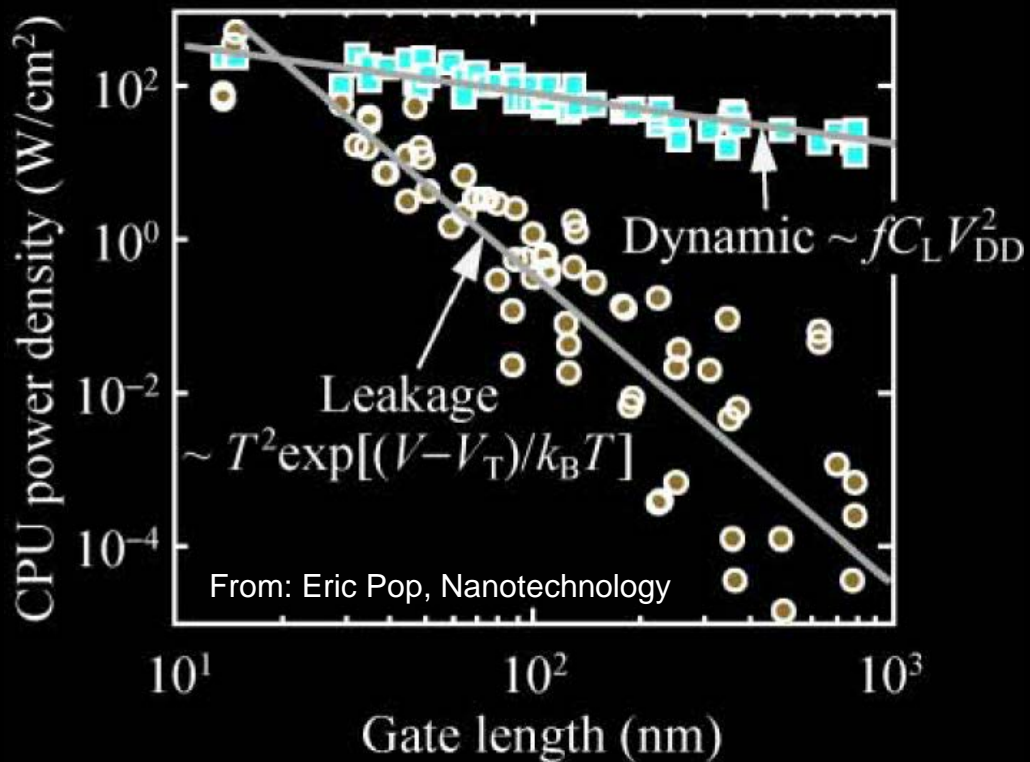


Static Power:

- Leakage through transistors

$$P \propto I_{OFF} \propto 1/\exp(V_{DD})$$

Device Scaling for Performance

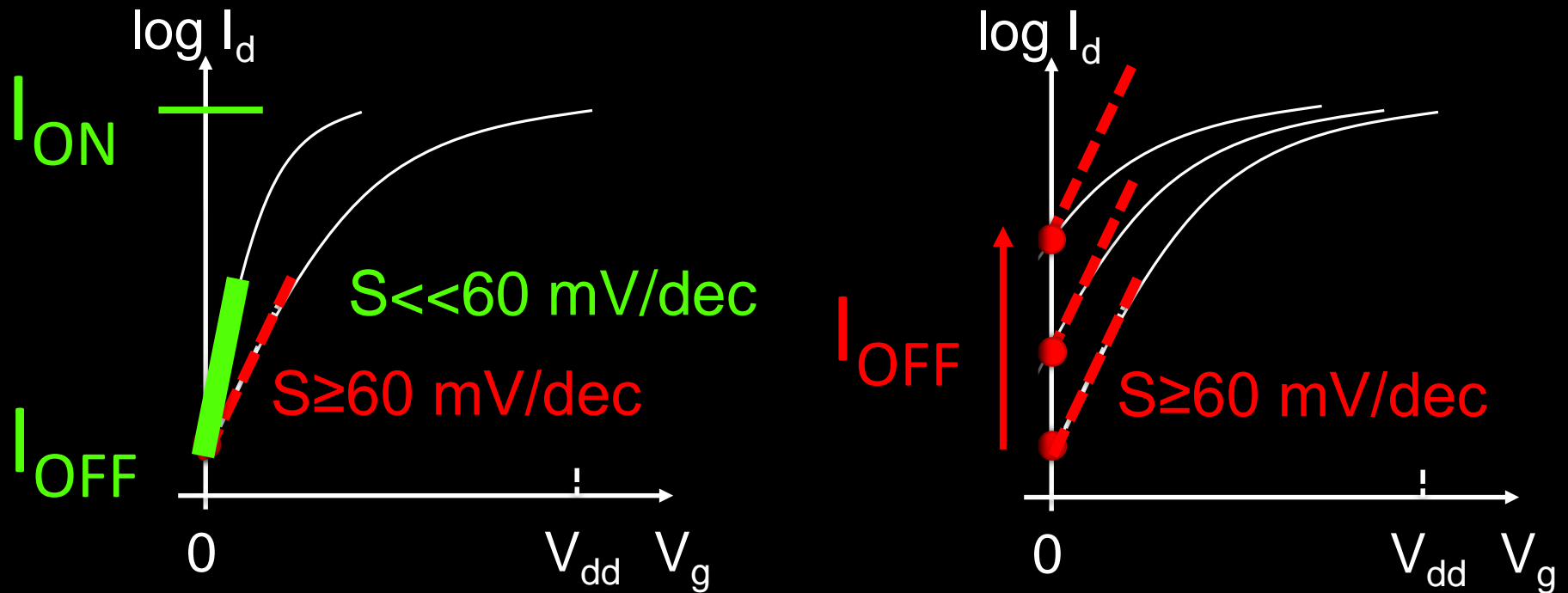


Static Power:

➤ Leakage through transistors

$$P \propto I_{OFF} \propto \cancel{1/\exp(V_{DD})}$$

Device Scaling for Performance

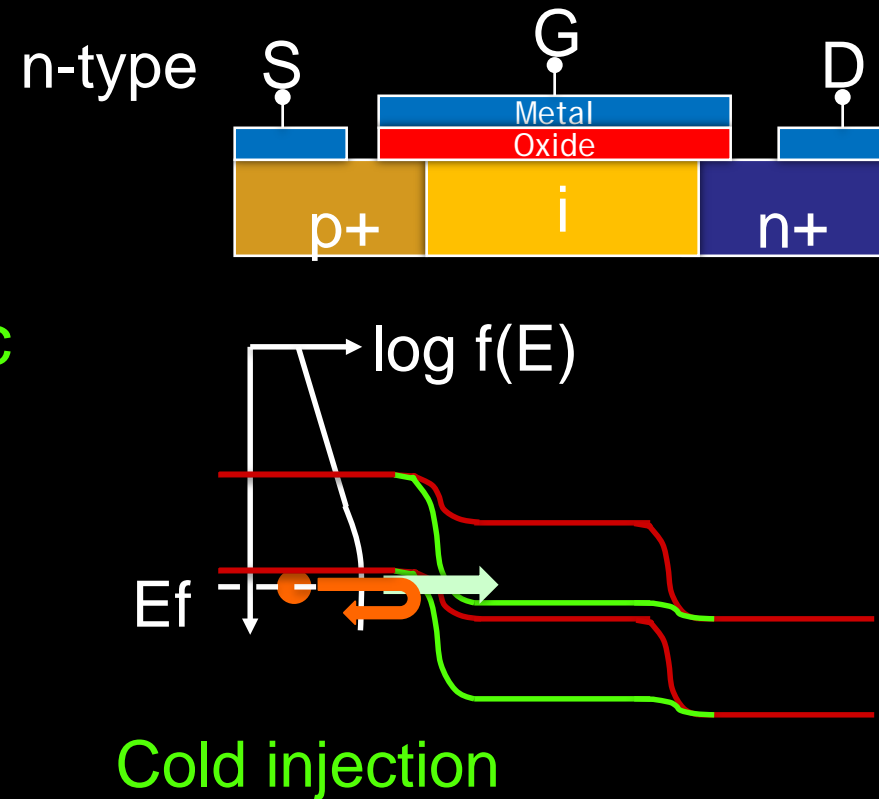
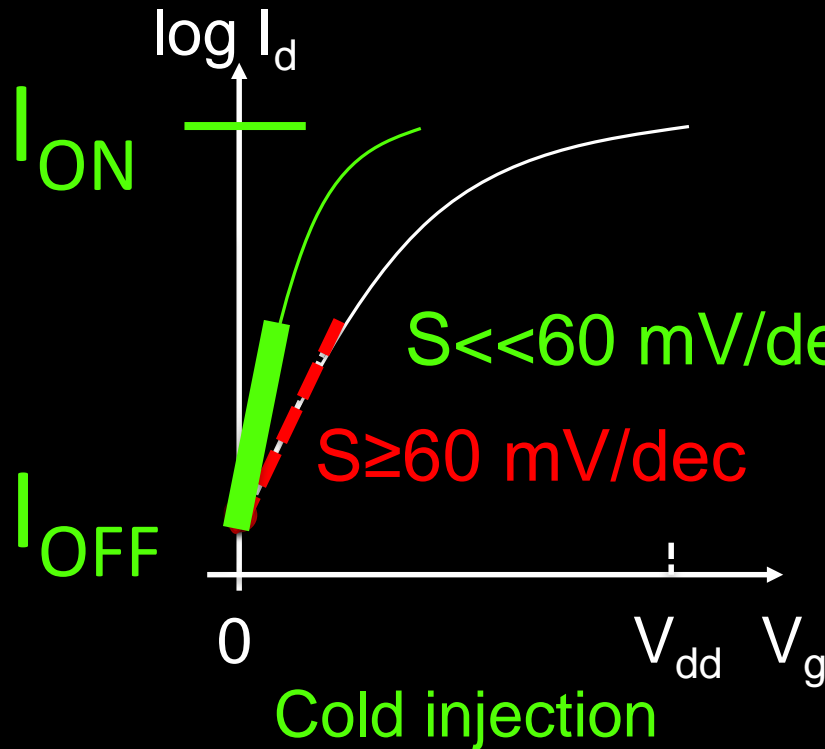


Static Power:

➤ Leakage through transistors

$$P \propto I_{OFF} \propto \cancel{1/\exp(V_{DD})}$$

Need a Different Switch



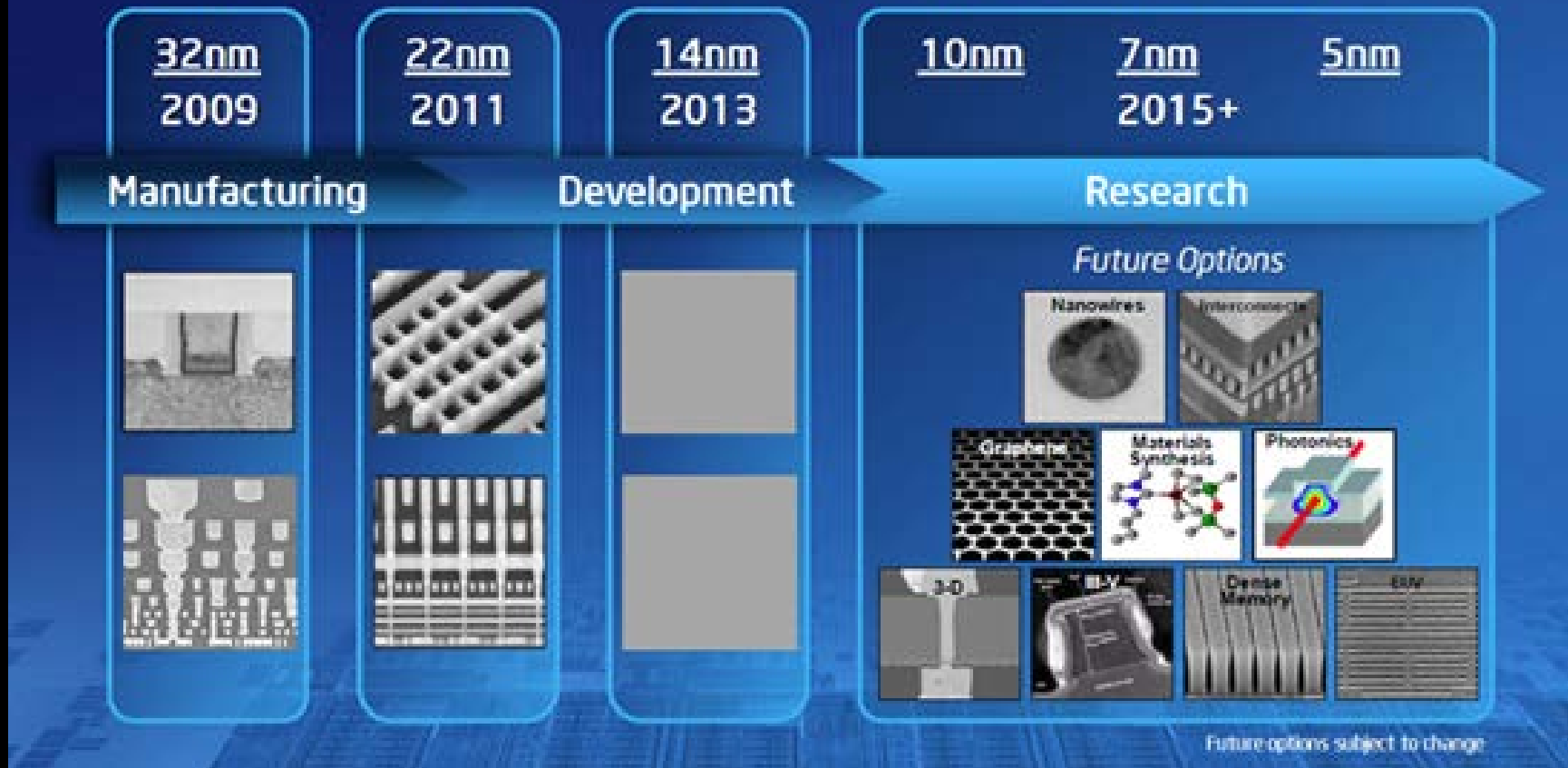
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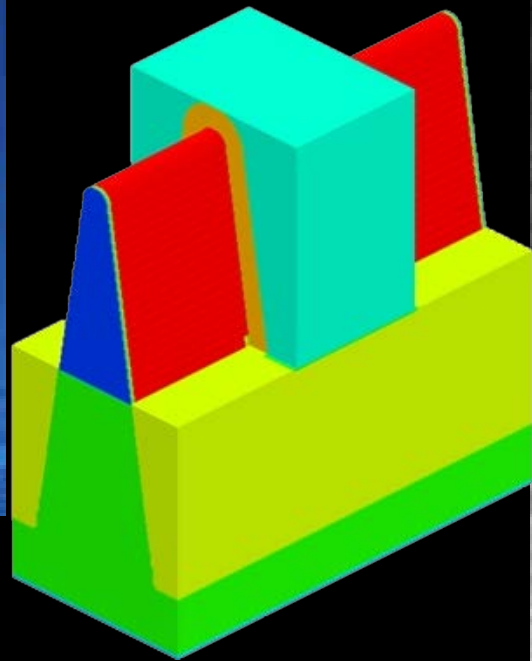
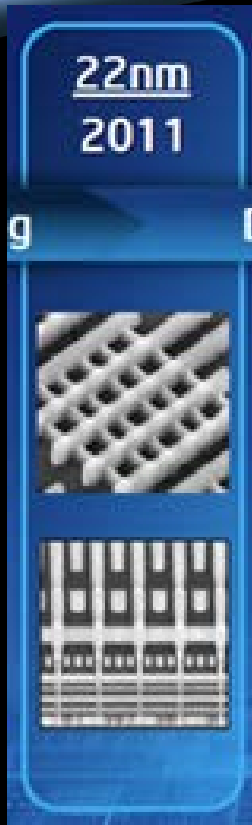
Intel Roadmap

Innovation Enabled Technology Pipeline *Our Visibility Continues to Go Out ~10 Years*

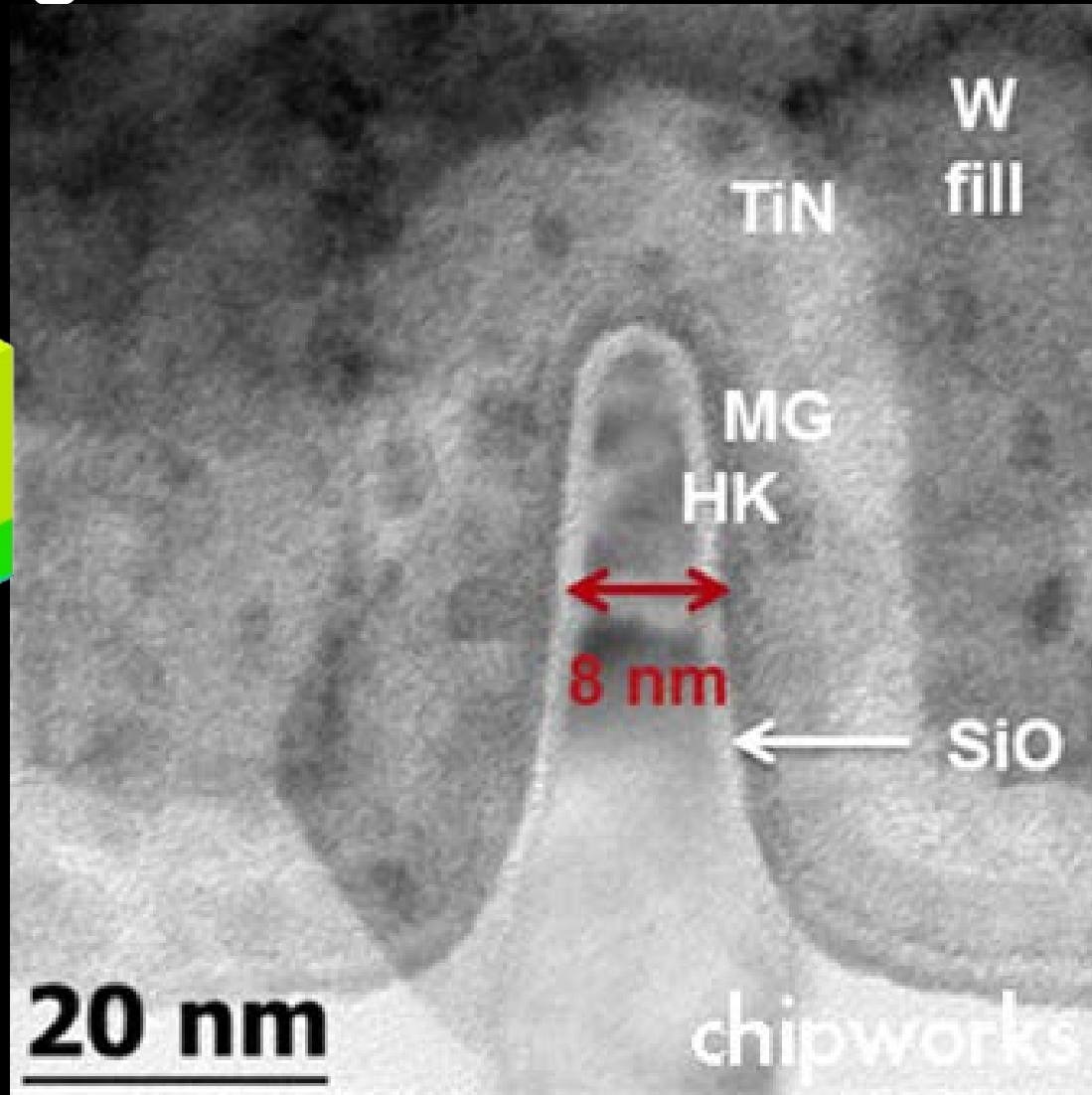


Today: non-planar 3D devices

Better gate control!

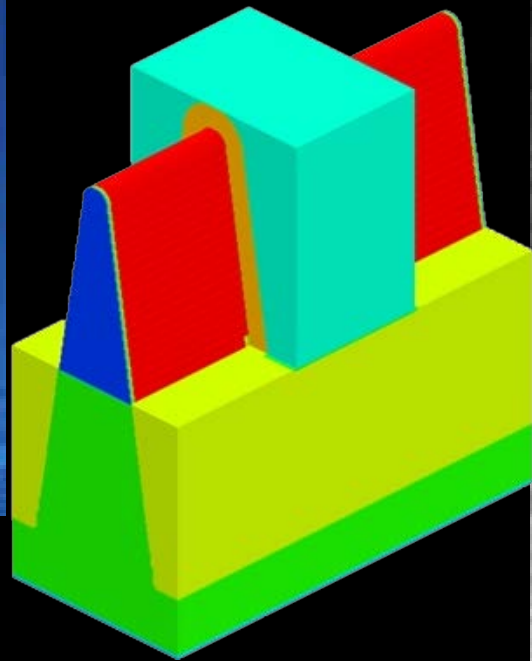
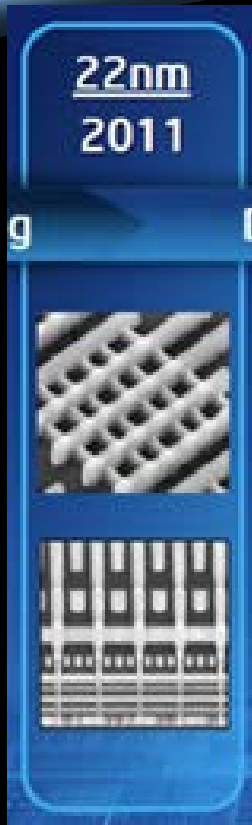


Intel 22nm finFET



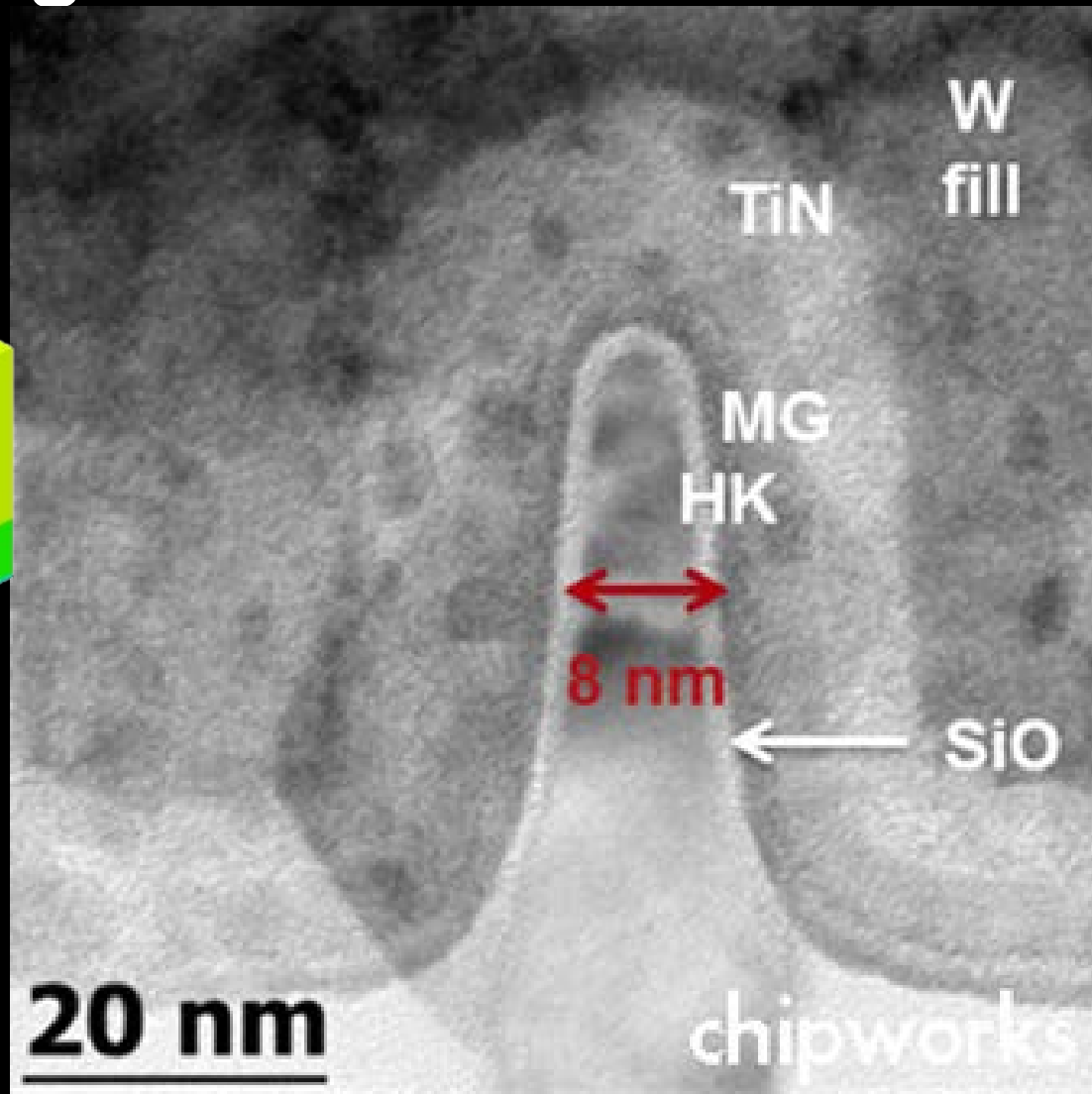
Today: non-planar 3D devices

Better gate control!



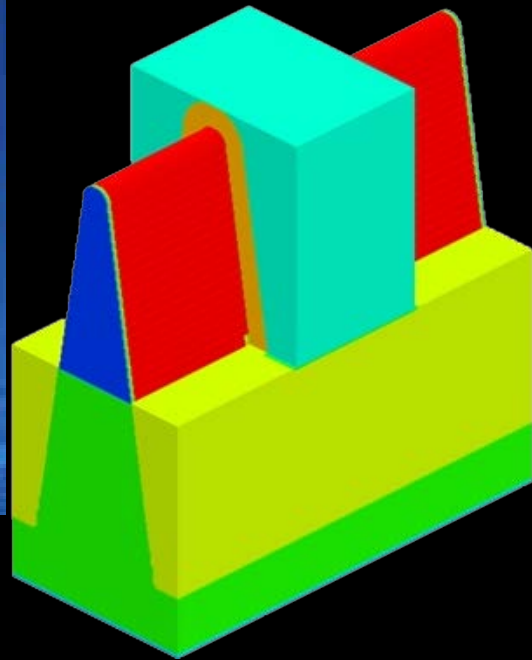
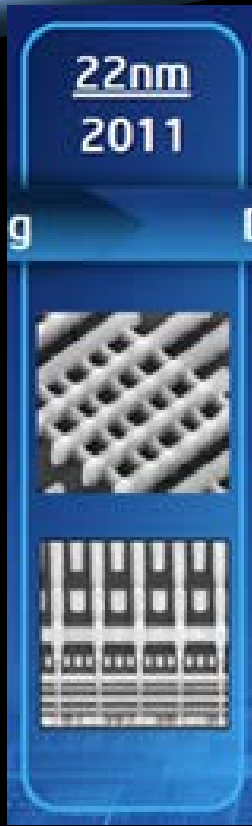
22nm = 176 atoms

8nm = 64 atoms



Today: non-planar 3D devices

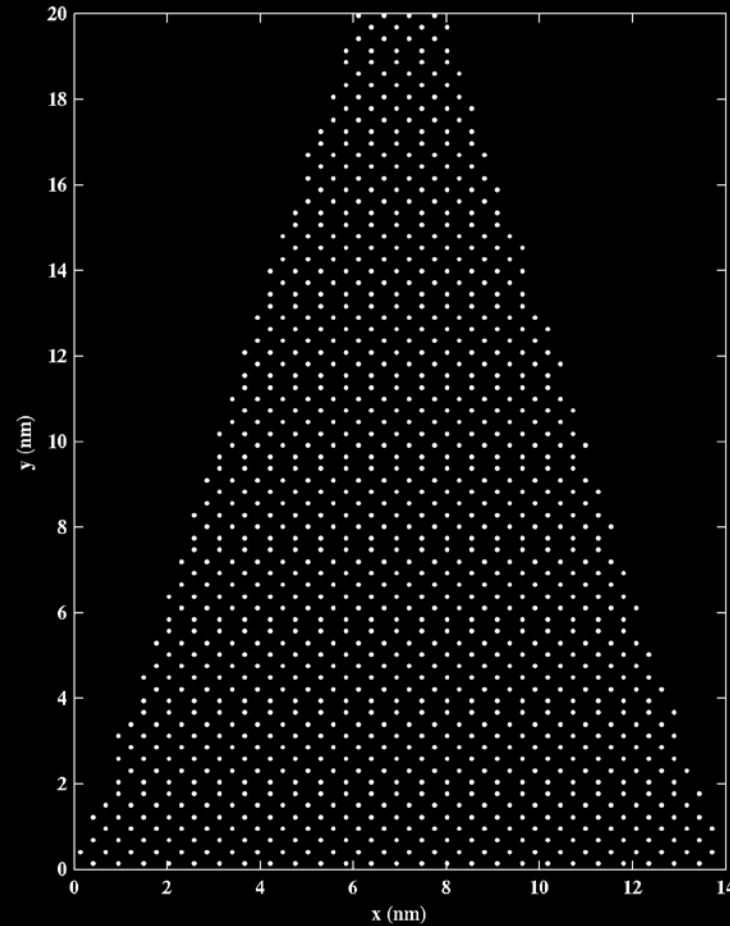
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22nm = 176 atoms

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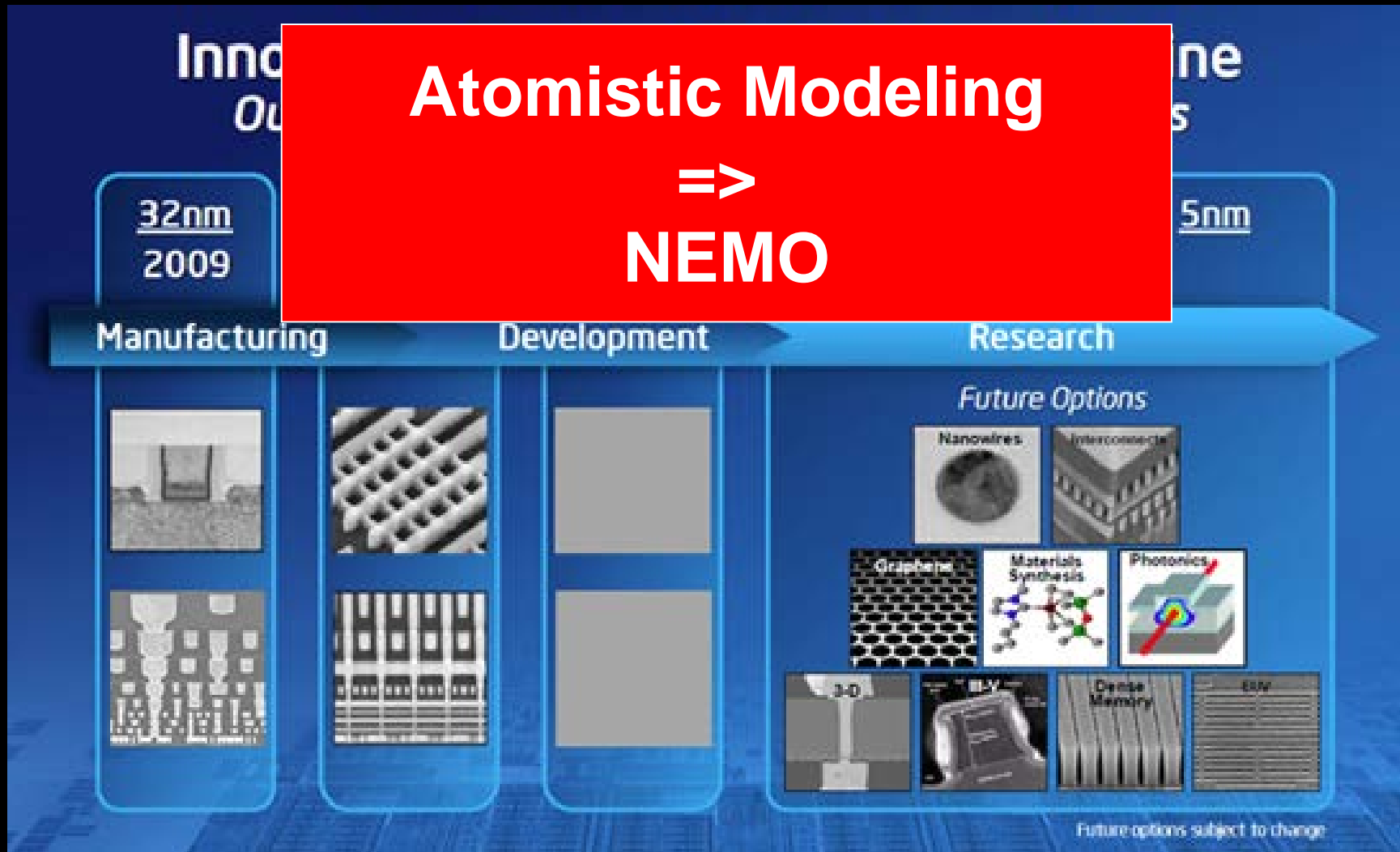
1,085 atoms



http://www.goldstandardsimulations.com/index.php/news/blog_search/simulation-analysis-of-the-intel-22nm-finfet/

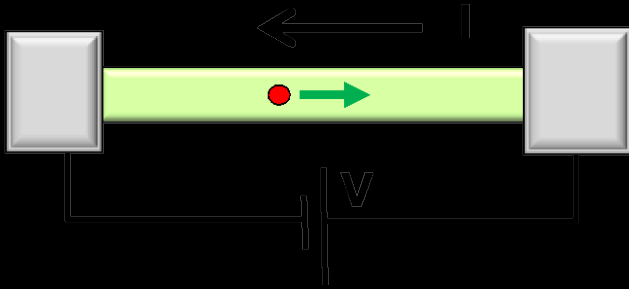
<http://www.chipworks.com/media/wpmu/uploads/blogs.dir/2/files/2012/08/Intel22nmPMOSfin.jpg>

Roadmap of finite atoms!



nm Node	22	14	10	7	5
Node atoms	176	122	80	56	40
Critical atoms	64	44 _(?)	29 _(?)	20 _(?)	14 _(?)
Electrons	160-190	64-80	30-38	18-23	11-15

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$$= q \times n \times v \times A$$

charge density velocity area

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