

Section 31 MOSFET Non-Idealities

Gerhard Klimeck

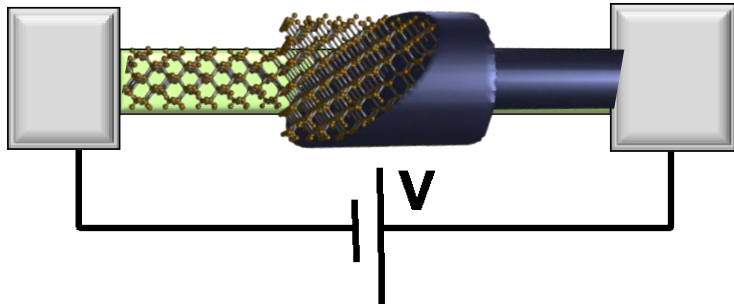
gekco@purdue.edu



School of Electrical and
Computer Engineering

Section 31

MOSFET Non-Idealities



$$I = G \times V$$

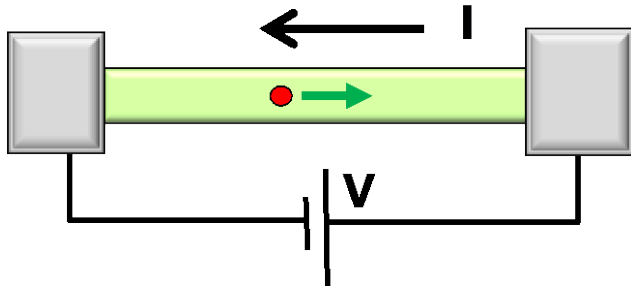
$$= q \times n \times v \times A$$

↑ charge density
 ↑ velocity
 ↑ area

	Equilibrium	DC	Small signal	Large Signal	Circuits
PN Diode	◇	◇	◇	◇	
Schottky Diode	◇	◇	◇		
BJT/ HBT	◇ ◇	◇ ◇	◇		
MOScap MOSFET	◇ ◇	◇ ◇	◇	◇	

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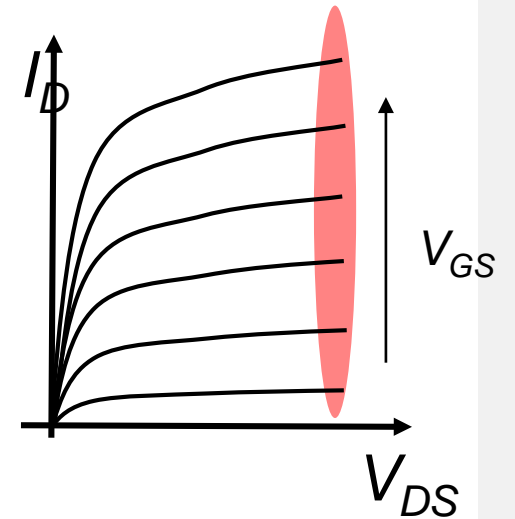
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- 1 • 31.1 Flat band voltage - What is it and how to measure it?
- 2 • 31.2 Threshold voltage shift due to trapped charges
- 3 • 31.3 Physics of interface traps

$$I_D(V_D = V_{DD}) \sim (V_G - V_{th})^\alpha$$

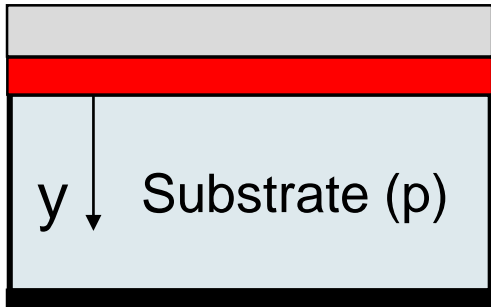
$$1 < \alpha < 2$$

$$V_{th} = V_{th,ideal} + \phi_{MS} - \frac{\gamma_M Q_M}{C_o} - \frac{Q_F}{C_o} - \frac{Q_{IT}(\phi_s)}{C_o}$$

Metal contact
 Charge in oxide
 Fixed charge
 interface traps

(1) Idealized MOS Capacitor

In the idealized MOS capacitor, the Fermi Levels in metal and semiconductor align perfectly so that at zero applied bias, the energy bands are flat

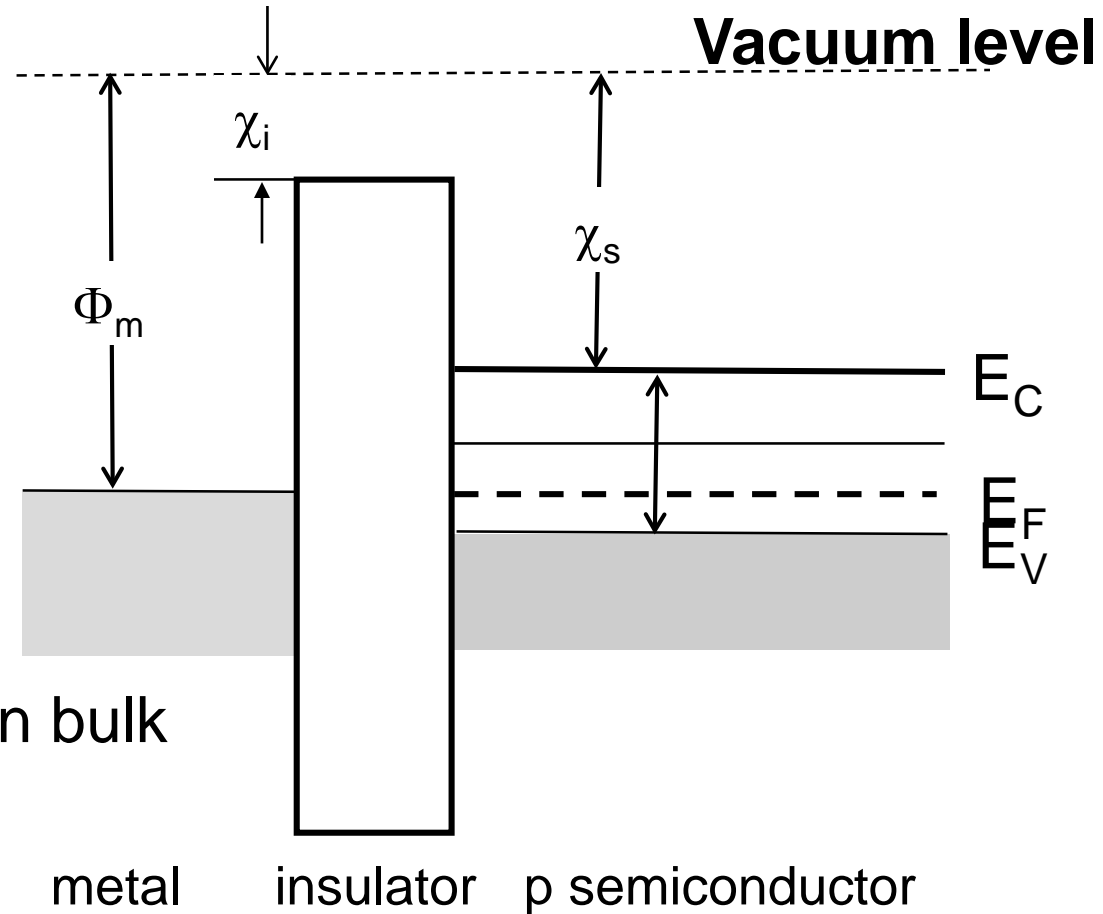


Recall that

$$Q_i = C_{ox} (V_G - V_{th,ideal})$$

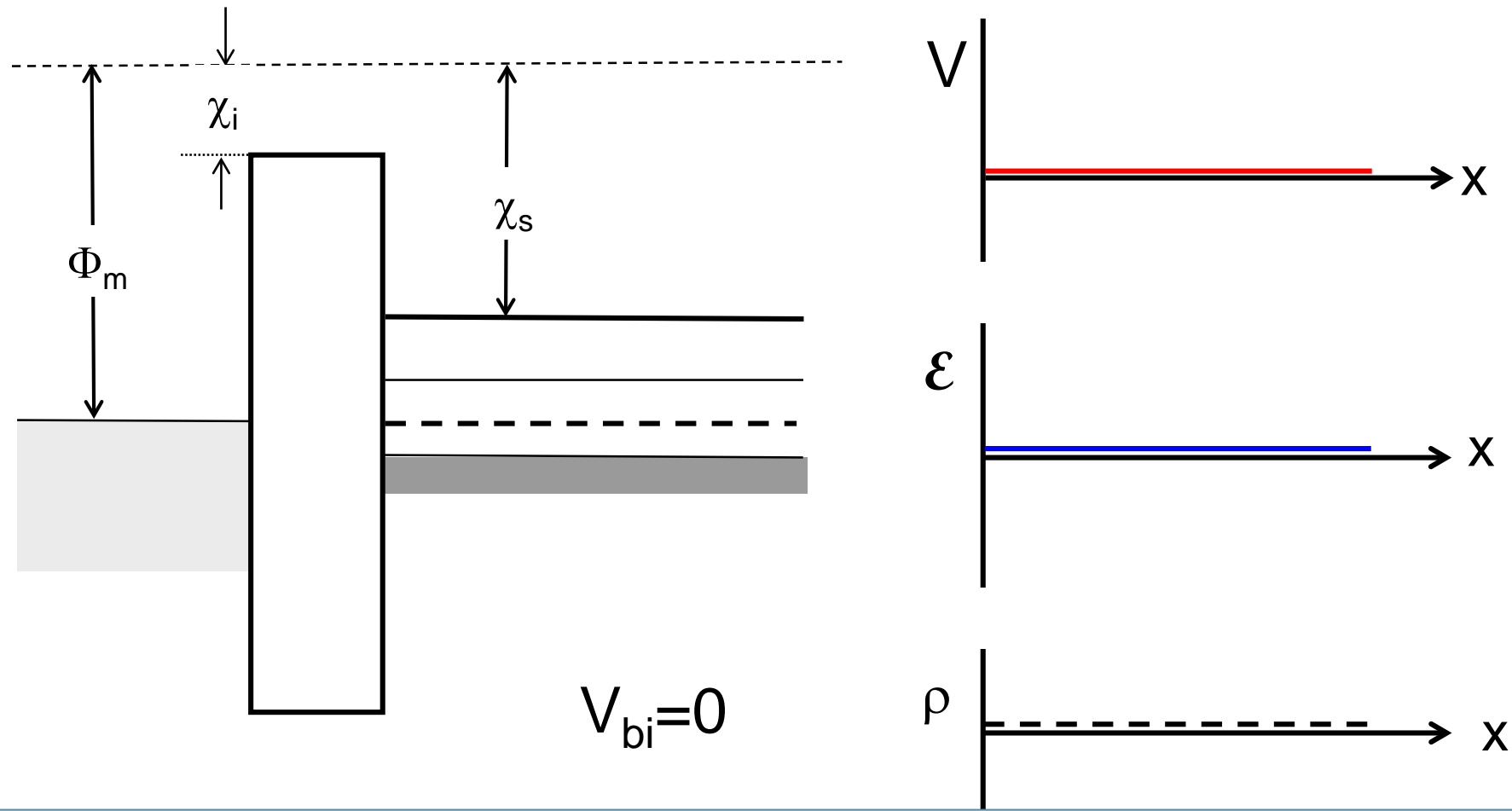
Threshold: Onset of inversion
 Inversion charge=Doping level in bulk

$$V_{th,ideal} = \psi_s - \frac{Q_B}{C_{ox}} \Big|_{\psi_s = 2\phi_F}$$



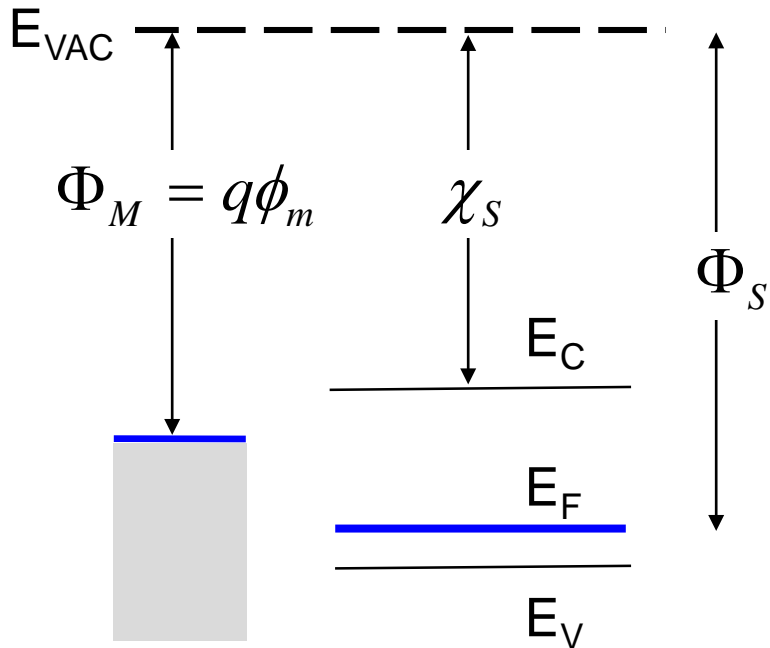
In historical perspective: Aluminum => poly => back to metals

Potential, Field, Charges

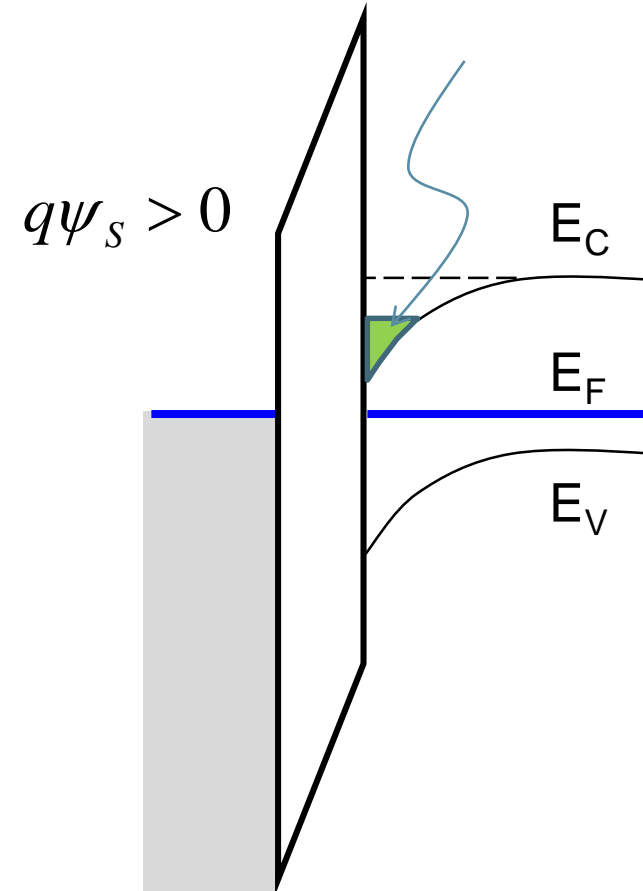


No built in potential, fields or charges at zero applied bias in the idealized MOS structure

Real MOS Capacitor with $\Phi_M < \Phi_S$



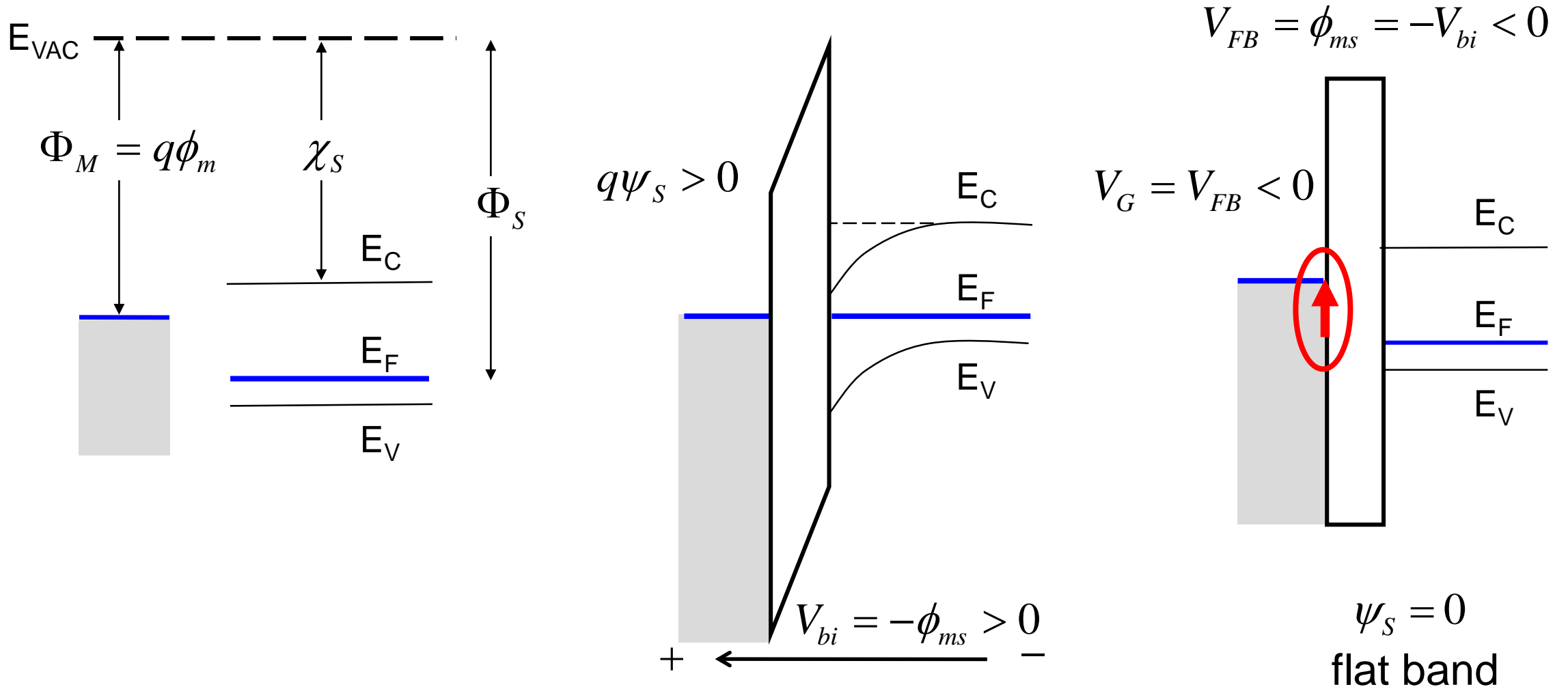
Note the difference



In reality, the metal and semiconductor Fermi Levels are never aligned perfectly \rightarrow when you bring them together there is charge transfer from the bulk of the semiconductor to the surface so that we have alignment

Do we need to apply less or more V_G to invert the channel ?

Real MOS Capacitor with $\Phi_M < \Phi_S$ in Flatband Condition



The Flatband Voltage is the voltage applied to the gate that gives zero-band bending in the MOS structure. Applying this voltage nullifies the effect of the built-in potential. This voltage needs to be incorporated into the idealized MOS analysis while calculating threshold voltage

How to Calculate Built-in or Flat-band Voltage

The presence of a flatband voltage lowers or raises the threshold voltage of a MOS structure.

$$qV_{bi} = (\chi_s + E_g - \Delta_p) - \Phi_M$$

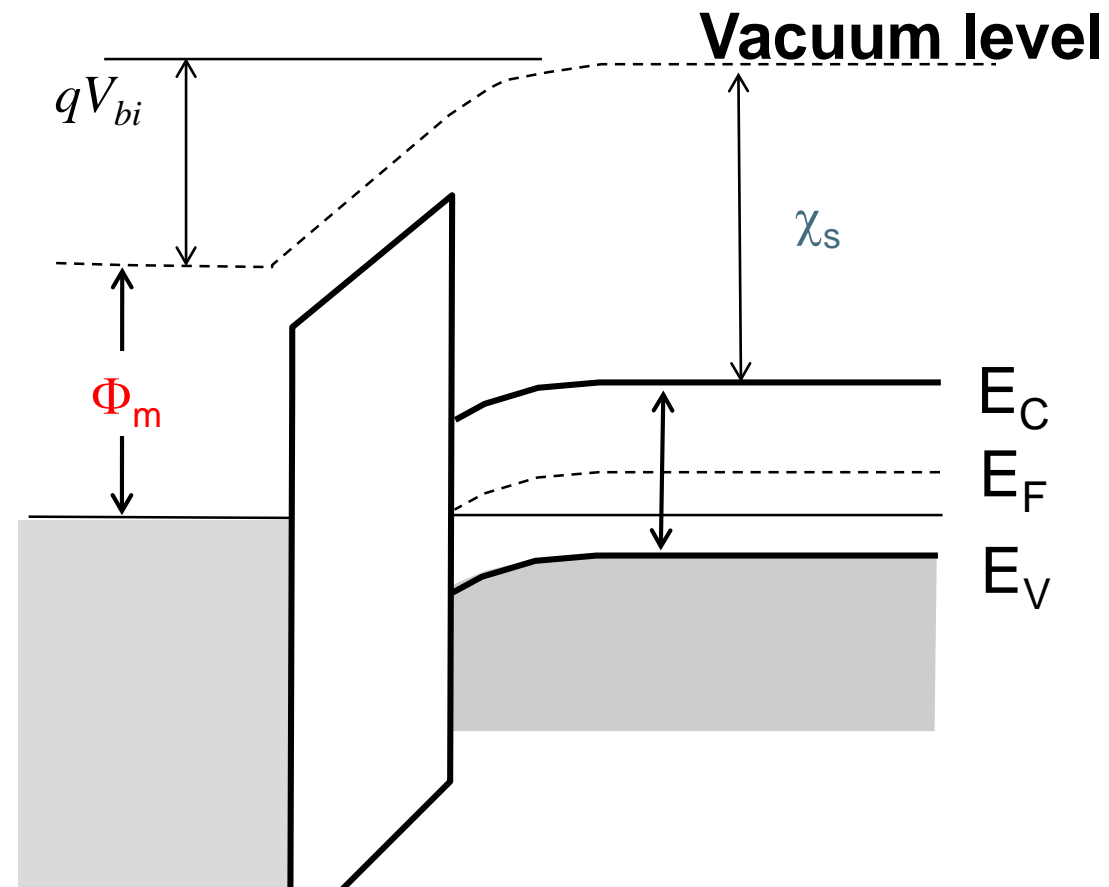
$$= qV_{FB} \equiv \phi_{MS}$$

$$V_{th,ideal} = \psi_s - \frac{Q_B}{C_{ox}} \Big|_{\psi_s = 2\phi_F}$$

Therefore,

$$Q_i = C_{ox} (V_G - V_{th})$$

$$V_{th} = \left(2\phi_F - \frac{Q_B}{C_{ox}} \right) - V_{FB}$$



Engineering question →

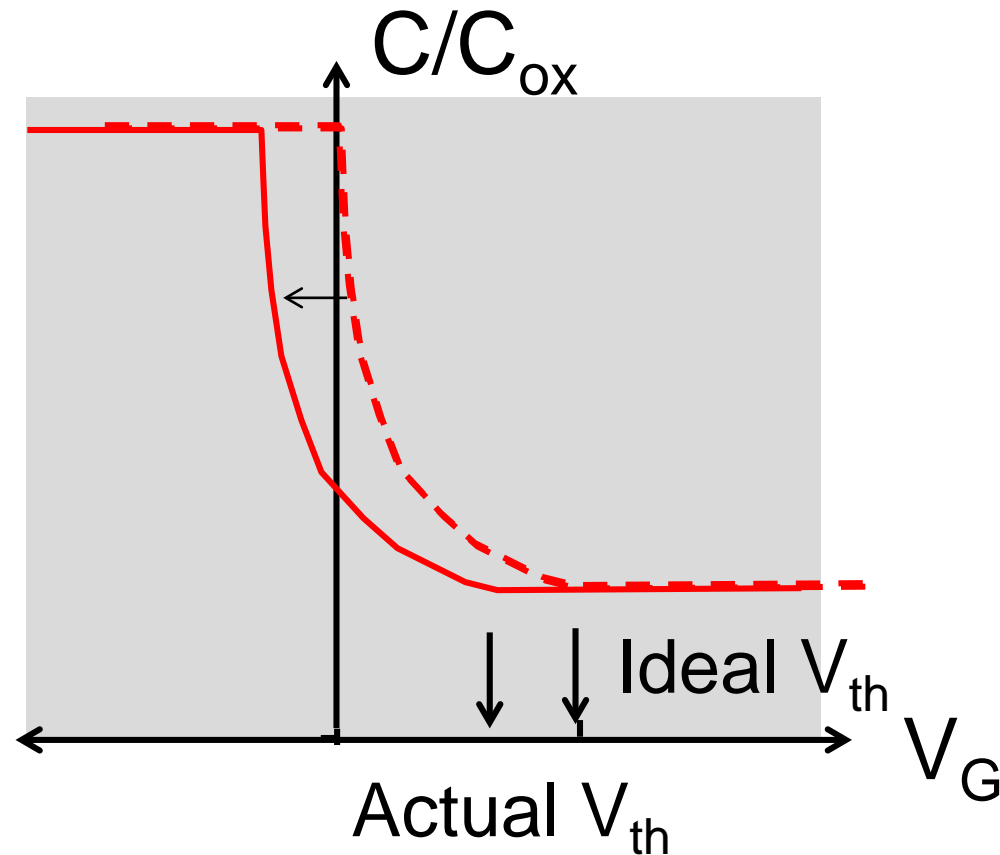
Is it desirable to have a metal having a work function greater or less than the electron affinity+($E_C - E_F$) in the semiconductor?

Measure of Flat-band shift from C-V Characteristics

The transition point between accumulation and depletion in a non-ideal MOS structure is shifted to the left when the metal work function is smaller than the electron affinity $+(E_c - E_f)$. At **zero applied bias the semiconductor is already depleted** so that a very small positive bias inverts the channel. The flatband voltage is the amount of voltage required to shift the curve such that the transition point is at zero bias.

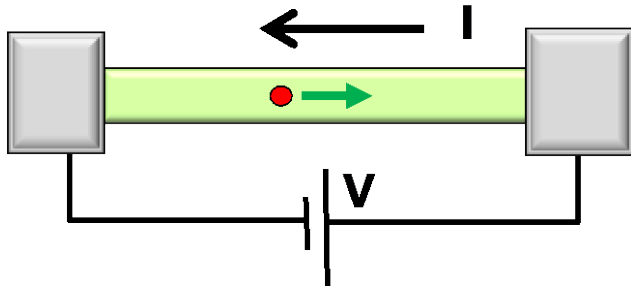
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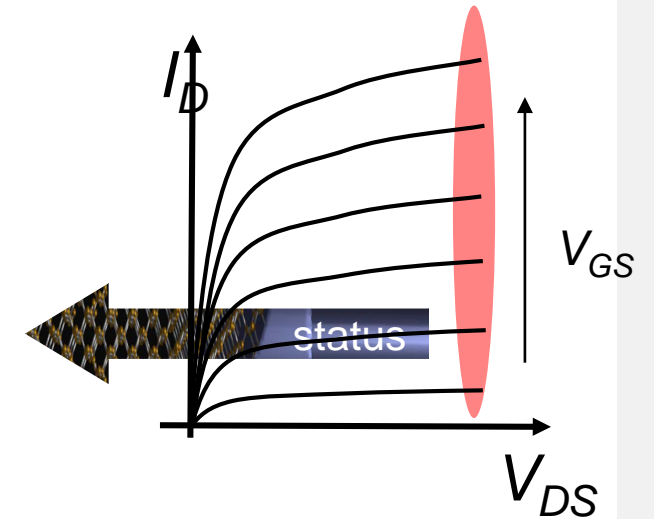
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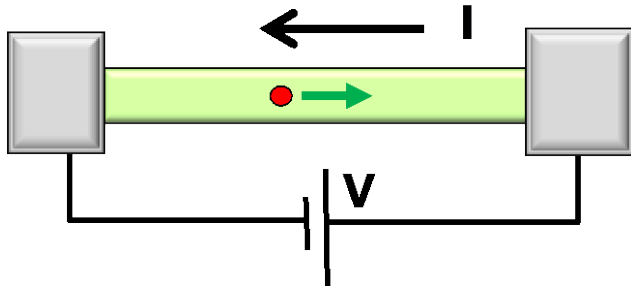
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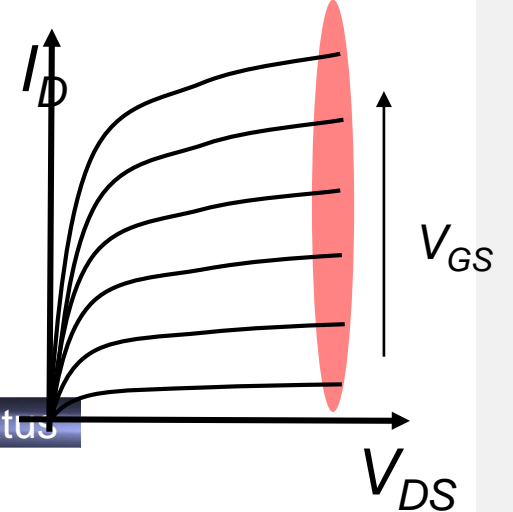
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