SCHRED version 2.1

USER MANUAL

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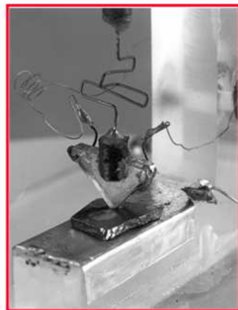
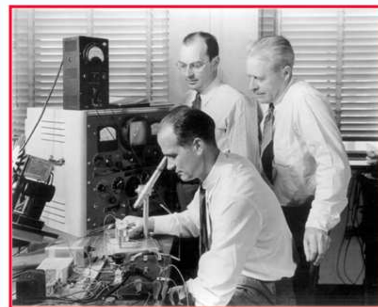
1. Some Historical Data

A stylized replica of the first transistor

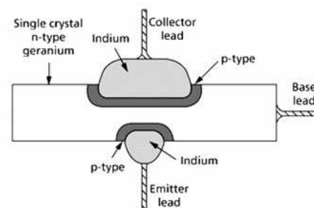


Original point-contact transistor (1947)



Inventors of the transistor: William Shockley, John Bardeen and Walter Brattain

First grown transistor (1950)



The beginning of the transistor era.

Semiconductors had been used in the electronics field for some time before the invention of the transistor. Around the turn of the 20th century they were quite common as detectors in radios, used in a device called a "cat's whisker". These detectors were somewhat troublesome, however, requiring the operator to move a small tungsten filament (the whisker) around the surface of a galena (lead sulfide) or carborundum (silicon carbide) crystal until it suddenly started working. Then, over a period of a few hours or days, the cat's whisker would slowly stop working and the process would have to be repeated. At the time their operation was completely mysterious. After the introduction of the more reliable and amplified vacuum tube based radios, the cat's whisker systems quickly disappeared. The "cat's whisker" is a primitive example of a special type of diode still popular today, called a Schottky diode.

During World War II, radar research quickly pushed radar receivers to operate at ever higher frequencies and the traditional tube based radio receivers no longer worked well. The introduction of the cavity magnetron from Britain to the United States in 1940 during the Tizard Mission resulted in a pressing need for a practical high-frequency amplifier. On a whim, Russell Ohl of Bell Laboratories decided to try a cat's whisker. By this point they had not been in use for a number of years, and no one at the labs had one. After hunting one down at a used radio store in Manhattan, he found that it worked much better than tube-based systems. Ohl investigated why the cat's whisker functioned so well. He spent most of 1939 trying to grow more pure versions of the crystals. He soon found that with higher quality crystals their finicky behaviour went away, but so did their ability to operate as a radio detector. One day he found one of his purest crystals nevertheless worked well, and interestingly, it had a clearly visible crack near the middle. However as he moved about the room trying to test it, the detector would mysteriously work, and then stop again. After some study he found that the behaviour was controlled by the light in the room–more light caused more conductance in the crystal. He invited several other people to see this crystal, and Walter Brattain immediately realized there was some sort of junction at the crack. Further research cleared up the remaining mystery. The crystal had cracked because either side contained very slightly different amounts of the impurities Ohl could not remove–about 0.2%. One side of the crystal had impurities that added extra electrons (the carriers of electrical current) and made it a "conductor". The other had impurities that wanted to bind to these electrons, making it (what he called) an "insulator". Because the two parts of the crystal were in contact with each other, the electrons could be pushed out of the conductive side which had extra electrons (soon to be known as the *emitter*) and replaced by new ones being provided (from a battery, for instance) where they would flow into the insulating portion and be collected by the whisker filament (named the *collector*). However, when the voltage was reversed the electrons

being pushed into the collector would quickly fill up the "holes" (the electron-needy impurities), and conduction would stop almost instantly. This junction of the two crystals (or parts of one crystal) created a solid-state diode, and the concept soon became known as semiconduction. The mechanism of action when the diode is off has to do with the separation of charge carriers around the junction. This is called a "depletion region".

Armed with the knowledge of how these new diodes worked, a vigorous effort began in order to learn how to build them on demand. Teams at Purdue University, Bell Labs, MIT, and the University of Chicago all joined forces to build better crystals. Within a year germanium production had been perfected to the point where military-grade diodes were being used in most radar sets. After the war, William Shockley decided to attempt the building of a triode-like semiconductor device. He secured funding and lab space, and went to work on the problem with Brattain and John Bardeen.

The key to the development of the transistor was the further understanding of the process of the electron mobility in a semiconductor. It was realized that if there was some way to control the flow of the electrons from the emitter to the collector of this newly discovered diode, one could build an amplifier. For instance, if you placed contacts on either side of a single type of crystal the current would not flow through it. However if a third contact could then "inject" electrons or holes into the material, the current would flow. Actually doing this appeared to be very difficult. If the crystal were of any reasonable size, the number of electrons (or holes) required to be injected would have to be very large -– making it less than useful as an amplifier because it would require a large injection current to start with. That said, the whole idea of the crystal diode was that the crystal itself could provide the electrons over a very small distance, the depletion region. The key appeared to be to place the input and output contacts very close together on the surface of the crystal on either side of this region. Brattain started working on building such a device, and tantalizing hints of amplification continued to appear as the team worked on the problem. Sometimes the system would work but then stop working unexpectedly. In one instance a non-working system started working when placed in water. Ohl and Brattain eventually developed a new branch of quantum mechanics known as surface physics to account for the behaviour. The electrons in any one piece of the crystal would migrate about due to nearby charges. Electrons in the emitters, or the "holes" in the collectors, would cluster at the surface of the crystal where they could find their opposite charge "floating around" in the air (or water). Yet they could be pushed away from the surface with the application of a small amount of charge from any other location on the crystal. Instead of needing a large supply of injected electrons, a very small number in the right place on the crystal would accomplish the same thing. Their

understanding solved the problem of needing a very small control area to some degree. Instead of needing two separate semiconductors connected by a common, but tiny, region, a single larger surface would serve. The emitter and collector leads would both be placed very close together on the top, with the control lead placed on the base of the crystal. When current was applied to the "base" lead, the electrons or holes would be pushed out, across the block of semiconductor, and collect on the far surface. As long as the emitter and collector were very close together, this should allow enough electrons or holes between them to allow conduction to start. The Bell team made many attempts to build such a system with various tools, but generally failed. Setups where the contacts were close enough were invariably as fragile as the original cat's whisker detectors had been, and would work briefly, if at all. Eventually they had a practical breakthrough. A piece of gold foil was glued to the edge of a plastic wedge, and then the foil was sliced with a razor at the tip of the triangle. The result was two very closely spaced contacts of gold. When the plastic was pushed down onto the surface of a crystal and voltage applied to the other side (on the base of the crystal), current started to flow from one contact to the other as the base voltage pushed the electrons away from the base towards the other side near the contacts. The point-contact transistor had been invented. While the device was constructed a week earlier, Brattain's notes describe the first demonstration to higher-ups at Bell Labs on the afternoon of 23 December 1947, often given as the birthdate of the transistor. The "PNP point-contact germanium transistor" operated as a speech amplifier with a power gain of 18 in that trial. Known generally as a point-contact transistor today, John Bardeen, Walter Houser Brattain, and William Bradford Shockley were awarded the Nobel Prize in physics for their work in 1956.

Bell Telephone Laboratories needed a generic name for their new invention: "Semiconductor Triode", "Solid Triode", "Surface States Triode" [sic], "Crystal Triode" and "Iotatron" were all considered, but "transistor", coined by John R. Pierce, won an internal ballot. The rationale for the name is described in the following extract from the company's Technical Memoranda (May 28, 1948) [26] calling for votes: Transistor. This is an abbreviated combination of the words "transconductance" or "transfer", and "varistor". The device logically belongs in the varistor family, and has the transconductance or transfer impedance of a device having gain, so that this combination is descriptive.

Shockley was upset about the device being credited to Brattain and Bardeen, who he felt had built it "behind his back" to take the glory. Matters became worse when Bell Labs lawyers found that some of Shockley's own writings on the transistor were close enough to those of an earlier 1925 patent by Julius Edgar Lilienfeld that they thought it best that his name be left off the patent application. Shockley was incensed, and decided to demonstrate who was the real brains of

the operation. Only a few months later he invented an entirely new type of transistor with a layer or 'sandwich' structure. This new form was considerably more robust than the fragile point-contact system, and would go on to be used for the vast majority of all transistors into the 1960s. It would evolve into the bipolar junction transistor. With the fragility problems solved, a remaining problem was purity. Making germanium of the required purity was proving to be a serious problem, and limited the number of transistors that actually worked from a given batch of material. Germanium's sensitivity to temperature also limited its usefulness. Scientists theorized that silicon would be easier to fabricate, but few bothered to investigate this possibility. Gordon K. Teal was the first to develop a working silicon transistor, and his company, the nascent Texas Instruments, profited from its technological edge. Germanium disappeared from most transistors by the late 1960s.

Within a few years, transistor-based products, most notably radios, were appearing on the market. A major improvement in manufacturing yield came when a chemist advised the companies fabricating semiconductors to use distilled water rather than tap water: calcium ions were the cause of the poor yields. "Zone melting", a technique using a moving band of molten material through the crystal, further increased the purity of the available crystals.

2. MOS Capacitors Description and SCHRED Examples

2.1 MOS Capacitors

2.2 SCHRED Examples for MOS Capacitors

2.2.1 Example 1: MOS Capacitor - Semiclassical vs. Quantum-Mechanical Model

2.2.2 Example 2: MOS Capacitor - Quantum-Mechanical Model Elaborated

2.2.3 MOS Capacitor – Poly-Depletion and Quantum-Mechanical Effects

2.2.4 Advanced Exercise 1: MOS Capacitors - Variation of the threshold voltage shift with doping.

2.2.5 Advanced Exercise 2: MOS Capacitors – Total capacitance degradation vs. different technology

2.1 MOS Capacitors

Integral part of any MOSFET device is the MOS capacitor. Regarding the MOS capacitors, the induced interface charge is closely linked to the shape of the electron energy bands of the semiconductor near the interface. At zero applied voltage, the bending of the energy bands is ideally determined by the difference in the work functions of the metal and the semiconductor. This band bending changes with the applied bias and the bands become flat when we apply the so-called flat-band voltage given by

$$V_{FB} = \Phi_M - \Phi_{sc},$$

where Φ_M and Φ_{sc} are the work functions of the metal and the semiconductor, respectively, X_s is the electron affinity for the semiconductor, E_c is the energy of the conduction band edge, and E_F is the Fermi level at zero applied voltage. The various energies involved are indicated in Figure 2.1, where we show typical band diagrams of a MOS capacitor at zero bias.

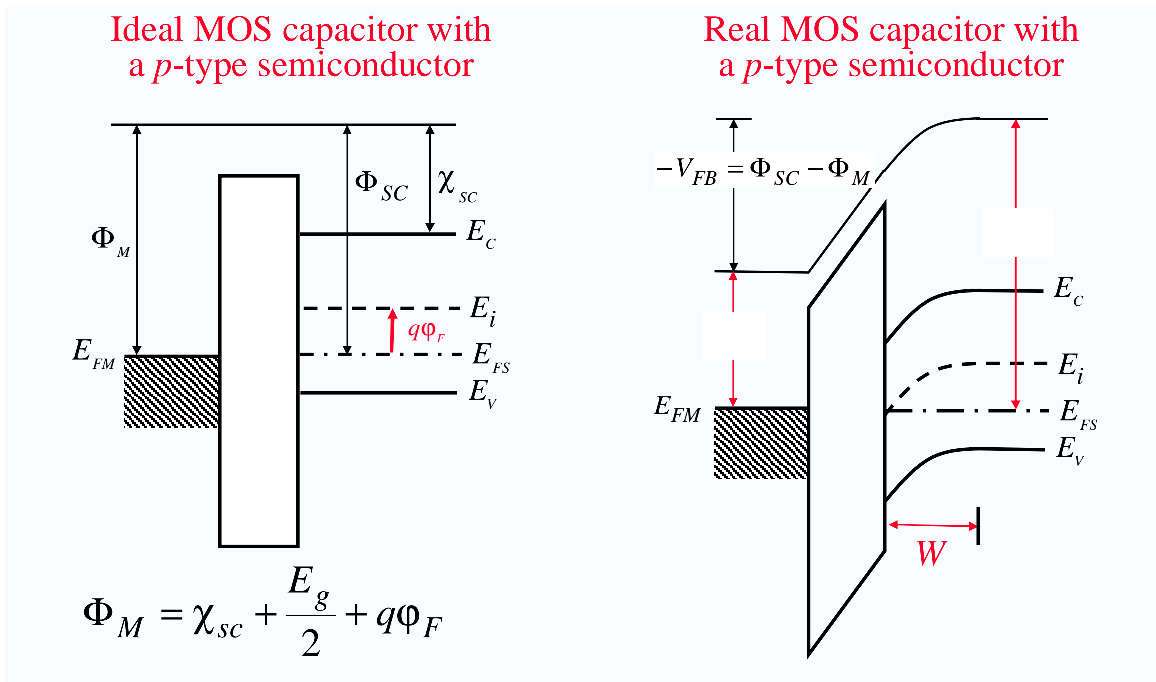


Figure 2.1. Left panel – Energy band diagram of ideal MOS capacitor. Right panel – energy band diagram of a real MOS capacitor.

At stationary conditions, no net current flows in the direction perpendicular to the interface owing to the very high resistance of the insulator layer (however, this does not apply to very thin oxides of a few nanometers, where tunneling becomes important). Hence, the Fermi level will remain constant inside the semiconductor, independent of the biasing conditions. However, between the semiconductor and the metal contact, the Fermi level is shifted by $E_{FM} - E_{Fs} = qV_G$ (see Figures 2.2 and 2.3). Hence, we have a quasi-equilibrium situation in which the semiconductor can be treated as if in thermal equilibrium.

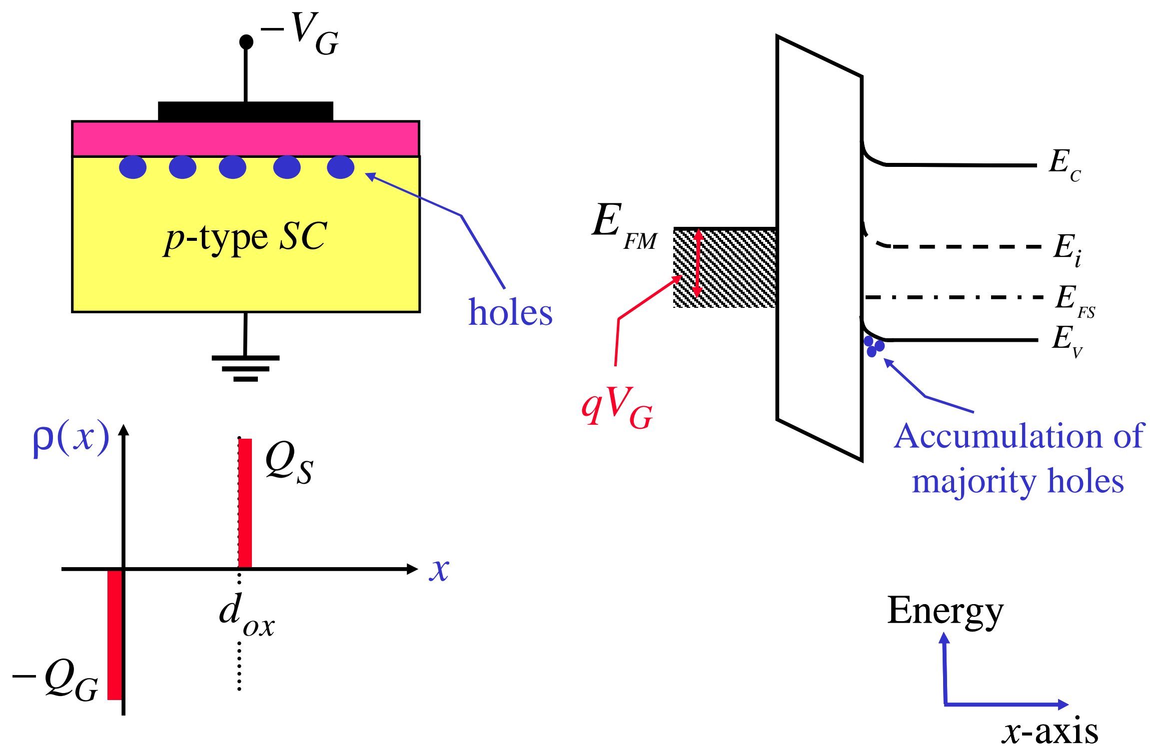


Figure 2.2 MOS capacitor under accumulation conditions.

A MOS structure with a *p*-type semiconductor will enter the *accumulation* regime of operation when the voltage applied between the metal and the semiconductor is more negative than the flat-band voltage ($V_{FB} < 0$ in Figure 2.2). In the opposite case, when $V_G > V_{FB}$, the semiconductor–oxide interface first becomes depleted of holes and we enter the so-called *depletion* regime (Figure 2.3 – top panel). By increasing the applied voltage, the band bending becomes so large that the energy difference between the Fermi level and

the bottom of the conduction band at the insulator–semiconductor interface becomes smaller than that between the Fermi level and the top of the valence band. This is called inversion regime of operation (Figure 2.3 bottom panel).

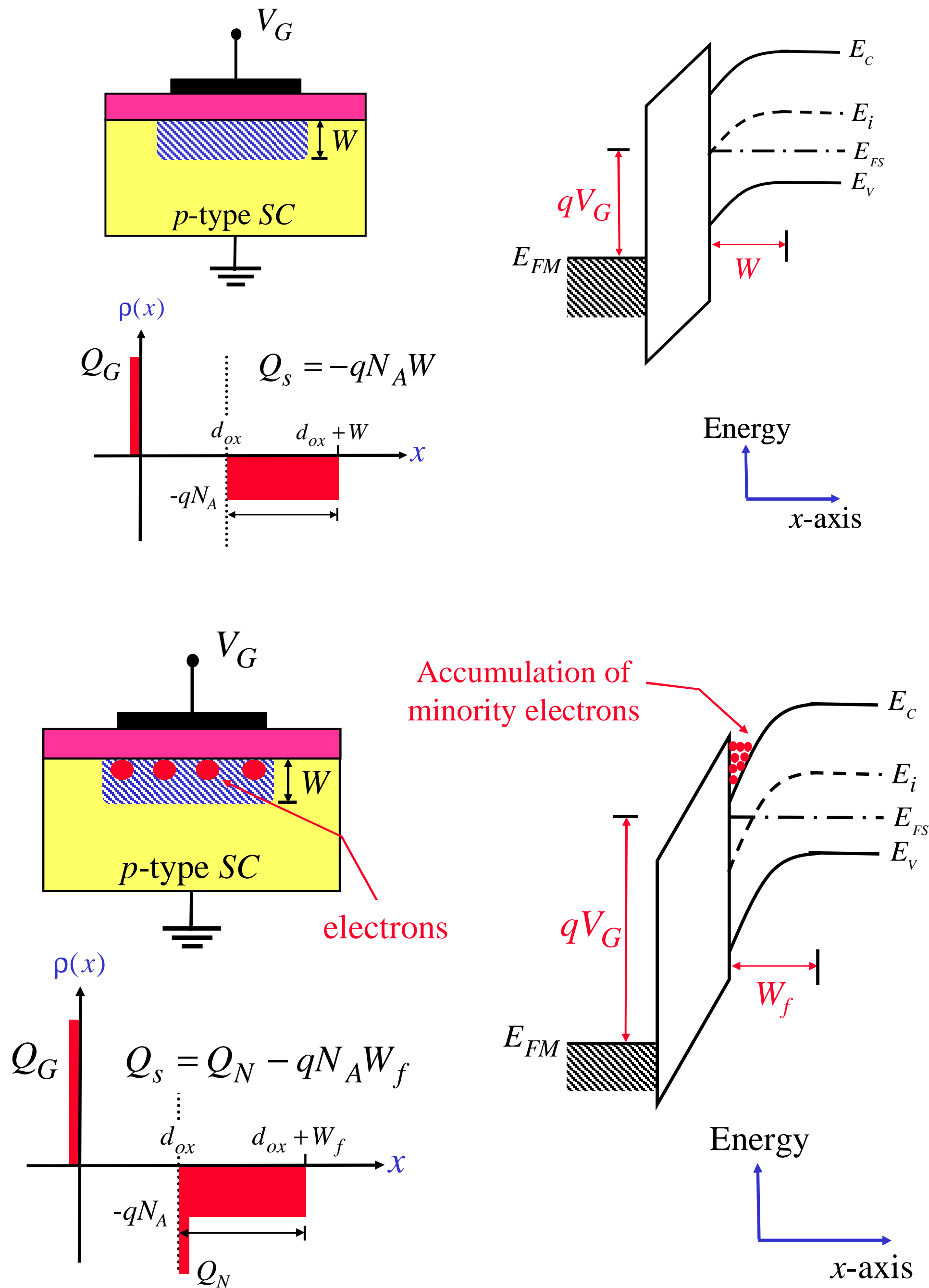


Figure 2.3 MOS capacitor under depletion conditions – top panel, and inversion conditions – bottom panel.

Carrier statistics tells us that the electron concentration then will exceed the hole concentration near the interface and we enter the *inversion* regime. At still larger applied voltage, we finally arrive at a situation in which the electron volume concentration at the interface exceeds the doping density in the semiconductor. This is the strong inversion case in which we have a significant conducting sheet of inversion charge at the interface (Figure 2.3 – bottom panel). In the description that follows, the symbol φ is used to signify the potential in the semiconductor measured relative to the potential at a position x deep inside the semiconductor. Note that φ becomes positive when the bands bend down, as in the example of a p-type semiconductor shown in Figure 2.3. From equilibrium electron statistics, we find that the intrinsic Fermi level E_i in the bulk corresponds to an energy separation $q\varphi_F$ from the actual Fermi level E_F of the doped semiconductor,

$$\varphi_F = V_T \ln\left(\frac{N_A}{n_i}\right) > 0$$

where V_T is the thermal voltage, N_A is the shallow acceptor density in the p-type semiconductor and n_i is the intrinsic carrier density of silicon. According to the usual definition, strong inversion is reached when the total band bending equals $2q\varphi_F$, corresponding to the surface potential $\varphi_s = 2\varphi_F$. Values of the surface potential such that $0 < \psi_s < 2\varphi_F$ correspond to the depletion and the weak inversion regimes, $\psi_s = 0$ is the flat-band condition, and $\psi_s < 0$ corresponds to the accumulation mode. Note that deep inside the semiconductor, we have $\varphi(\infty) = 0$. At the flat-band condition ($V_G = V_{FB}$), the surface charge is equal to zero. In accumulation ($V_G < V_{FB}$), the surface charge is positive, and in depletion and inversion ($V_G > V_{FB}$), the surface charge is negative.

In order to relate the semiconductor surface potential to the applied voltage V_G, we have to investigate how this voltage is divided between the insulator and the semiconductor. Using the condition of continuity of the electric flux density at the semiconductor–insulator interface, we find $\varepsilon_s F_s = \varepsilon_{ox} F_{ox}$, where ε_{ox} is the permittivity of the oxide layer and F_{ox} is the constant electric field in the insulator (assuming no space

charge). Hence, with an insulator thickness d_{ox}, the voltage drop across the insulator becomes $F_{ox}d_{ox}$. Accounting for the flat-band voltage, the applied voltage can be written as $V_G = V_{FB} + \varphi_s + \varepsilon_s F_s/c_{ox}$ where $c_{ox} = \varepsilon_{ox}/d_{ox}$ is the insulator capacitance per unit area.

The threshold voltage $V_G = V_{th}$, corresponding to the onset of the strong inversion, is one of the most important parameters characterizing metal-insulator-semiconductor devices. As discussed above, strong inversion occurs when the surface potential φ_s becomes equal to $2\varphi_F$. For this surface potential, the charge of the free carriers induced at the insulator–semiconductor interface is still small compared to the charge in the depletion layer, and the threshold voltage is calculated using:

$$V_G = \varphi_s + \frac{1}{C_{ox}}\sqrt{2qN_A\varepsilon_s\varepsilon_0\varphi_s}, \quad \text{where} \quad C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{d_{ox}}$$

$$V_{th} = V_G \quad \text{for which} \quad \varphi_s = 2\varphi_F$$

Note that the threshold voltage may also be affected by so-called fast surface states at the semiconductor–oxide interface and by fixed charges in the insulator layer. However, this is not a significant concern with modern day fabrication technology.

The threshold voltage separates the subthreshold regime, where the mobile carrier charge increases exponentially with increasing applied voltage V_G, from the above-threshold regime, where the mobile carrier charge is linearly dependent on the applied voltage V_G. However, there is no clear point of transition between the two regimes, so different definitions and experimental techniques have been used to determine V_{th}.

Well above threshold, the charge density of the mobile carriers in the inversion layer can be calculated using the parallel plate charge control model. This model gives an adequate description for the strong inversion regime of the MOS capacitor, but fails for applied voltages near and below threshold (i.e., in the weak inversion and depletion regimes). Several expressions have been proposed for a unified charge control model (UCCM) that covers all the regimes of operation. Details of the UCCM can be found elsewhere.

2.2 SCHRED Examples for MOS Capacitors

As pointed out in the description of SCHRED file that can be found on the SCHRED web-page, the quantum mechanical calculation primarily has two distinct features that differ from classical results. One is the quantization of available energy (along with different density of states than the classical) and another is the distribution of carriers (electrons as well as holes) inside the semiconductor. Most of the terminal behaviors that are attributed as quantum effects are some sort of manifestation of above two features. In the examples to follow in this part of tutorial, the main objective will be to address the major quantum effects that are seen in sub 100nm MOSFETs and in the process to learn to use SCHRED version 2.1 to understand some of the physics behind MOSFETs of such small scales. The examples that have been prepared for this purpose are listed and elaborated below.

Example 1: MOS Capacitor - Semiclassical vs. Quantum-Mechanical Model
Example 2: MOS Capacitor – Quantum-Mechanical Model Elaborated
Example 3: MOS Capacitor - Poly-Depletion and Quantum Mechanical Effects
Advanced Exercise 1: MOS Capacitors - Variation of the threshold voltage shift with doping.
Advanced Exercise 2: MOS Capacitors – Total capacitance degradation vs. different technology

2.2.1 Example 1: MOS Capacitor - Semiclassical vs. Quantum-Mechanical Model

The purpose of this example is to examine some basic concepts for MOS capacitors and to also point out the differences between the semi-classical and quantum-mechanical charge description at the interface. In this example we will examine MOS capacitor with the following properties: the gate is made of metal with worfunction equal to the silicon affinity. For this device structure we will plot and discuss:

(a) The conduction band profile for applied bias V_G=2 V (Figure 2.4)

(b) The electric field variation for V_G=2 V (Figure 2.5)

(c) The total charge density for applied bias V_G=2 V calculated semi-classically and quantum-mechanically (Figure 2.6)

The conduction band profile for this MOS capacitor is shown in Figure 2.4. We assume that there are no charges in the oxide. From the results shown it is clear that the electrostatic potential (energy) varies linearly in the oxide region and quadratically in the depletion region where we have finite amount of ionized acceptors (constant charge) and some amount of inversion layer electrons which gives rise to deviation from the quadratic behavior in the conduction band variation.

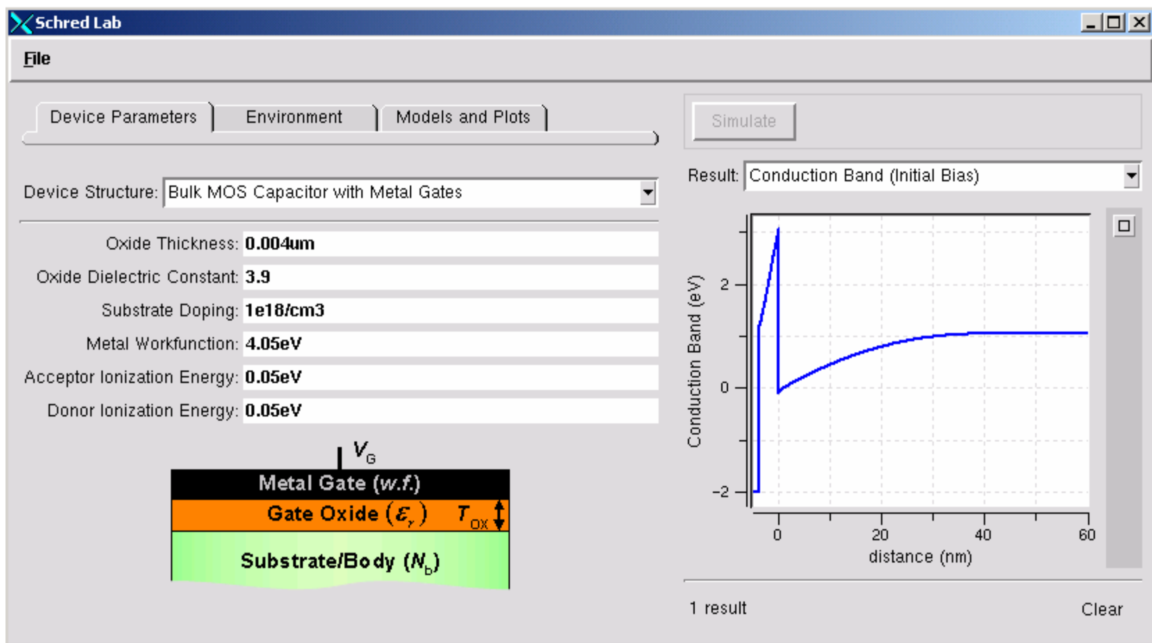


Figure 2.4 Conduction band profile in a MOS capacitor with p-type substrate for applied bias V_G=2 V.

The electric field variation in the MOS capacitor for the same bias conditions is shown in Figure 2.5. From the results presented we see that in the region where the potential is varying linearly, the electric field is constant (oxide) and when the potential varies quadratically with distance the electric field shows linear variation

(semiconductor). This is to be expected as the electric field is proportional to the gradient of the electrostatic potential.

Another important observation is that the electric field is discontinuous at the SC/oxide interface and this result follows from the fact that the perpendicular components of the displacement vector have to be continuous across the interface if there are no interface charges. Thus, due to the dielectric constants difference the field in the oxide side of the interface is approximately three times larger that the electric field on the semiconductor side of the interface. These observations are clearly demonstrated in Figure 2.5 below.

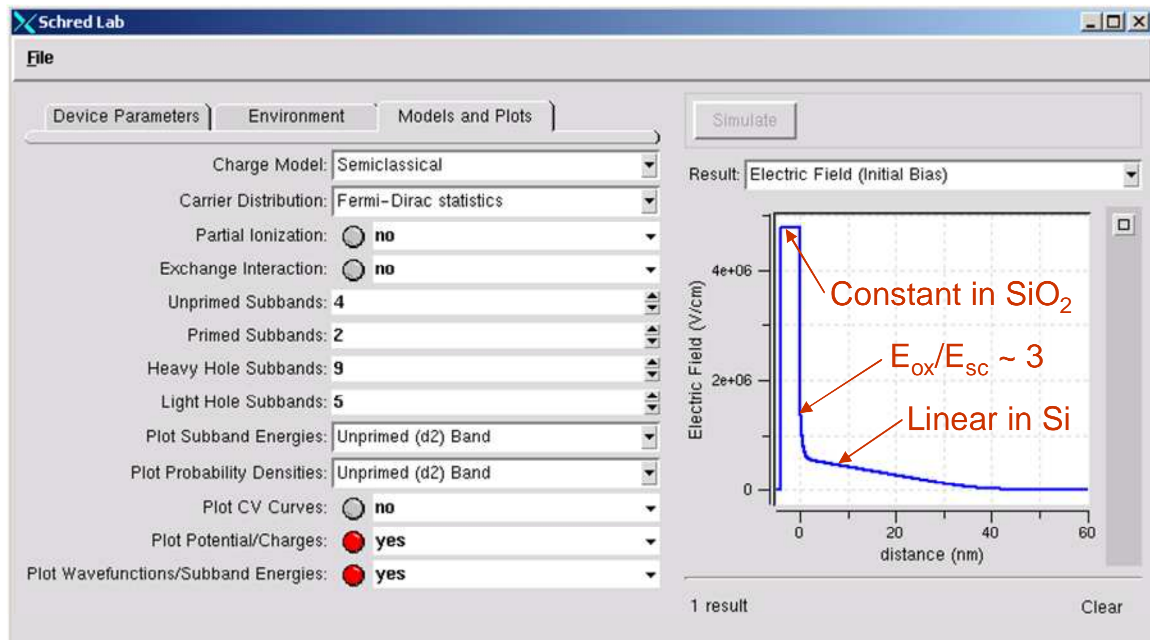


Figure 2.5 Electric field variation in MOS capacitors in depletion/inversion for V_G=2 V.

The total charge density calculated semi-classically and quantum-mechanically for V_G=2V is shown in Figures 2.6, respe6ctively. We see that since the semi-classical electron density varies exponentially with the potential, and since the potential energy is the smallest at the interface, the electron density peaks at the semiconductor side of the semiconductor/oxide interface and dies out exponentially when going towards the bulk of the semiconductor. Contrary to this behavior, the quantum-mechanical electron density vanishes at the semiconductor/oxide interface because of the large barrier (3.2 eV) and

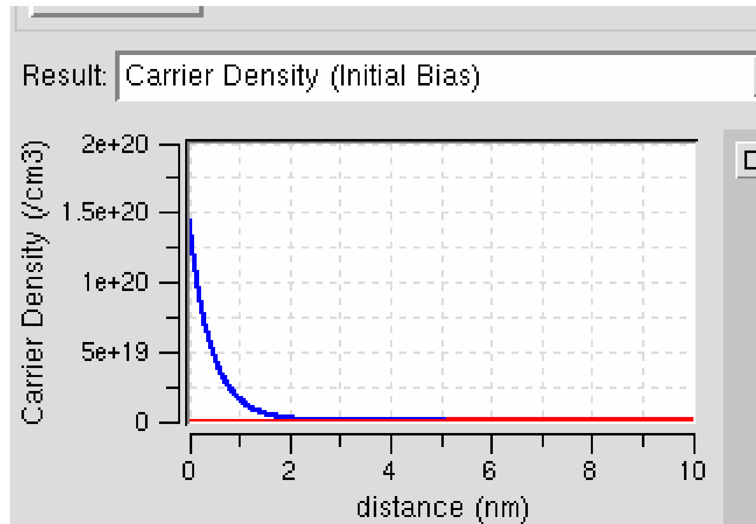
the peak of the electron density is away from the interface, which means that the average distance of the carriers increases for the quantum-mechanical case. The average distance of the carriers from the SC/oxide interface (that corresponds to x=0), is calculated using

$$z_{av} = \frac{\int_0^\infty z n(z) dz}{\int_0^\infty n(z) dz}$$

for the semiclassical case and

$$z_{av} = \frac{\sum_i N_i z_i}{N_S}, \qquad z_i = \frac{\int_0^\infty z \psi_i^2(z) dz}{\int_0^\infty \psi_i^2(z) dz}$$

for the quantum-mechanical case, where N_i is the sheet density in the *i*th subband, N_S is the total sheet density and $\psi_i(z)$ is the *i*th subband wavefunction. Since the average distance of the carriers is larger for the quantum-mechanical case this leads to a reduction of the inversion layer capacitance and as we will see later, this will lead to about 10-15% device transconductance degradation. Namely, the gate has decreased control of the charge in the channel. As in the semiclassical model, the quantum-mechanically calculated inversion electron density decreases to zero as we go deeper into the substrate.



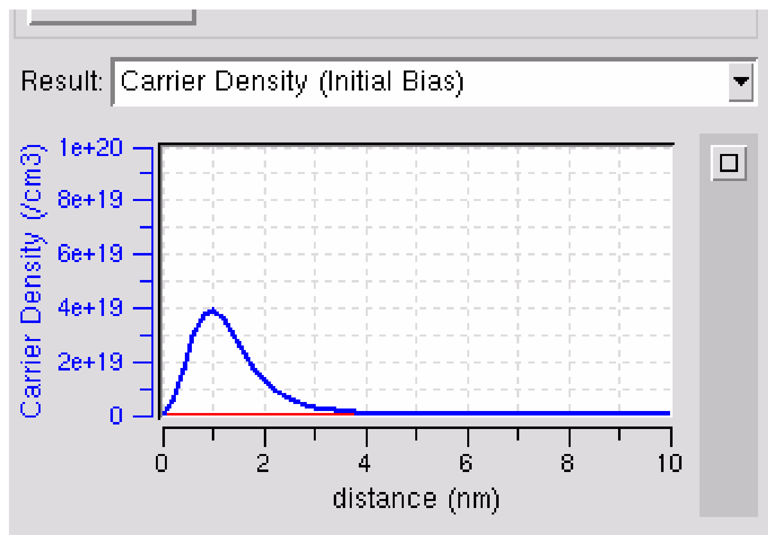


Figure 2.6 Semiclassically calculated inversion charge density (top panel) and quantum-mechanically calculated charge density (bottom panel).

2.2.2 Example 2: MOS Capacitor - Quantum-Mechanical Model Elaborated

The purpose of this example is to further elaborate the quantum-mechanical charge description at the interface and its implications on MOSFET operation. In this example we will again examine the MOS capacitor given in Example 1. Namely, the gate is made of metal, the thickness of the SiO_2 layer is t_{ox}=2 nm and the doping of the p-type substrate is $N_A=5\times10^{18}$ cm^{-3}. For this device structure we will plot and discuss:

(a) The sheet density N_S variation with the gate voltage V_G, for gate voltage varying between 0.5 and 2.5 V (Figure 2.7).

(b) Quantum-mechanical variation of the average distance versus applied gate bias V_G (Figure 2.8).

(c) The subband energy variation with the applied gate bias V_G (Figure 2.9).

(d) The shape of the wavefunctions from the unprimed and primed ladder of subbands for $V_G = 2V$ (Figure 2.10).

The variation of the sheet electron density versus applied gate bias V_G is shown in Figure 2.7 below. First we clearly see that in the inversion mode the sheet electron density is proportional to the gate bias. The approximate threshold voltage is found at the intersection of the two lines that are drown on the graph and denote the regions of constant and linear variation of the sheet electron density. Clearly, from gate voltage zero (or flat-band voltage) to gate voltage that equals the threshold voltage, the device operates in a depletion mode and for gate voltage larger than the threshold voltage the device operates under inversion conditions.

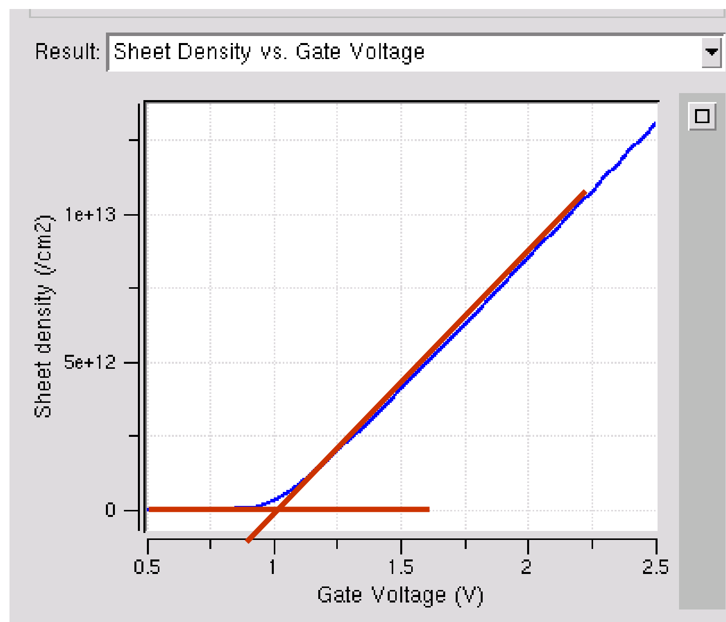


Figure 2.7. Variation of the sheet inversion electron density vs. gate bias in depletion and inversion mode of MOS-capacitor operation.

The variation of the average distance of the electrons and holes when using quantum-mechanical model for the electron density distribution in the inversion layer is shown in Figure 2.8. We see several important features. First, the electrons are more confined with increasing the gate voltage and exhibit smaller average distance from the semiconductor oxide interface with increasing the gate bias. The opposite is true for holes. Second, we observe that with increasing gate bias, electrons are more and more confined and the holes are not confined at all. The electron confinement increases with increasing positive gate bias because the well becomes narrower. Since the carriers are in this case confined closer to the interface, interface-roughness will start to play more important role and degrade the bulk mobility that is on the order of 1500 cm^2/V-s for bulk Si to an inversion layer mobility on the order of 200 cm^2/V-s for the highest doped samples (smallest devices). This will have significant implications on the transport characteristics of the device.

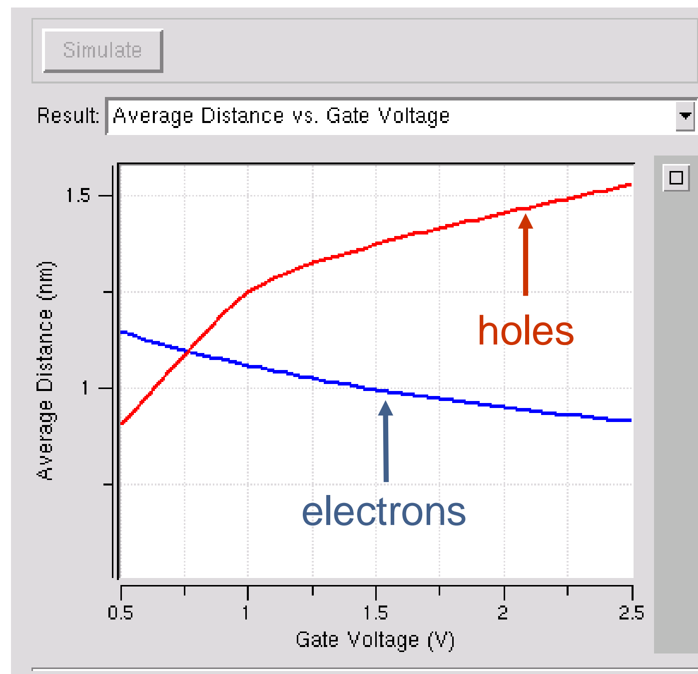


Figure 2.8. Average distance of electrons and holes in silicon inversion layer vs. gate bias. The electron average distance is calculated assuming quantum mechanical charge description of the electrons. If a semiclassical model for the electron charge description were used, the average distance would be about three times larger (not shown on this figure).

The subband energy variation from both unprimed (Δ_2) and primed (Δ_4) ladder of subbands is shown in Figure 2.9. From the results presented we observe two clearly pronounced features. Both of them are related to the fact that as we increase the positive gate bias and we drive the MOS capacitor further into inversion, the triangular potential well narrows. Narrower triangular potential well means higher value for the subband energies and increased subband separation. This, in turn, has significant implications on the population of the various subbans from the Δ_2 and Δ_4 band. Namely, with increasing the gate bias we are moving into the electronic quantum limit in which most of the carriers will be residing in the ground subband of the unprimed (Δ_2) ladder of subbands. Since for (100) orientation of the interface these carriers have the light mass in the transport direction, that means increased electron mobility. As we already said, since the average distance decreases interface-roughness will play more significant role. Hence, we have increased mobility due to reduced final density of states function and decrease in the mobility due to stronger influence of interface-roughness scattering. To get results in agreement with experiments for such structures both effects have to be simultaneously taken into account and that is accomplished by treating carriers as quasi-2D electron gas and taking interface-roughness into account in the transport model.

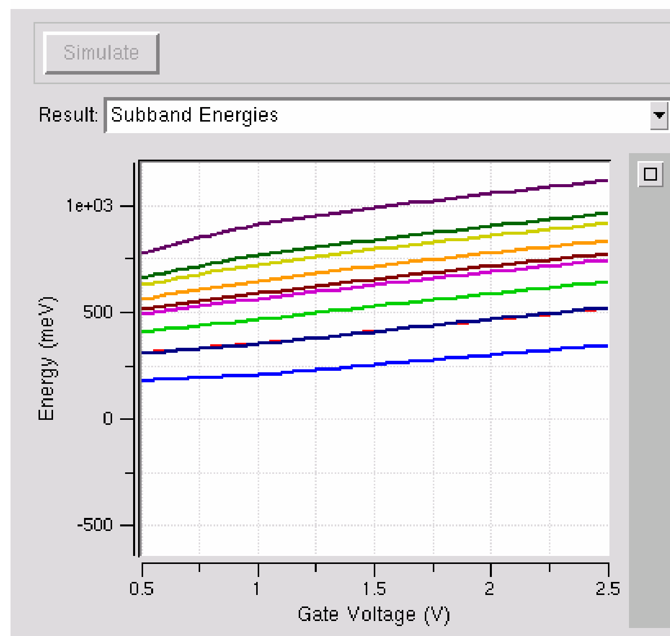


Figure 2.9. Variation of the Δ_2-band and Δ_4-band subbands versus applied gate bias.

Finally, in Figure 2.10 we show the wavefunctions of the lowest 4 subbands from the unprimed (Δ_2) band and the lowest 2 subbands from the primed (Δ_4 band). We see that the *n*th wavefunction has *n*-1 intersections with the *x*-axis. Since the subband energies of the Δ_4 band are higher in energy where the triangular well is wider, the spread of the wavefunctions corresponding to the lowest two subbands from the primed (Δ_4) ladder of subbands is larger when compared to that of the lowest two subbands from the unprimed (Δ_2) ladder of subbands.

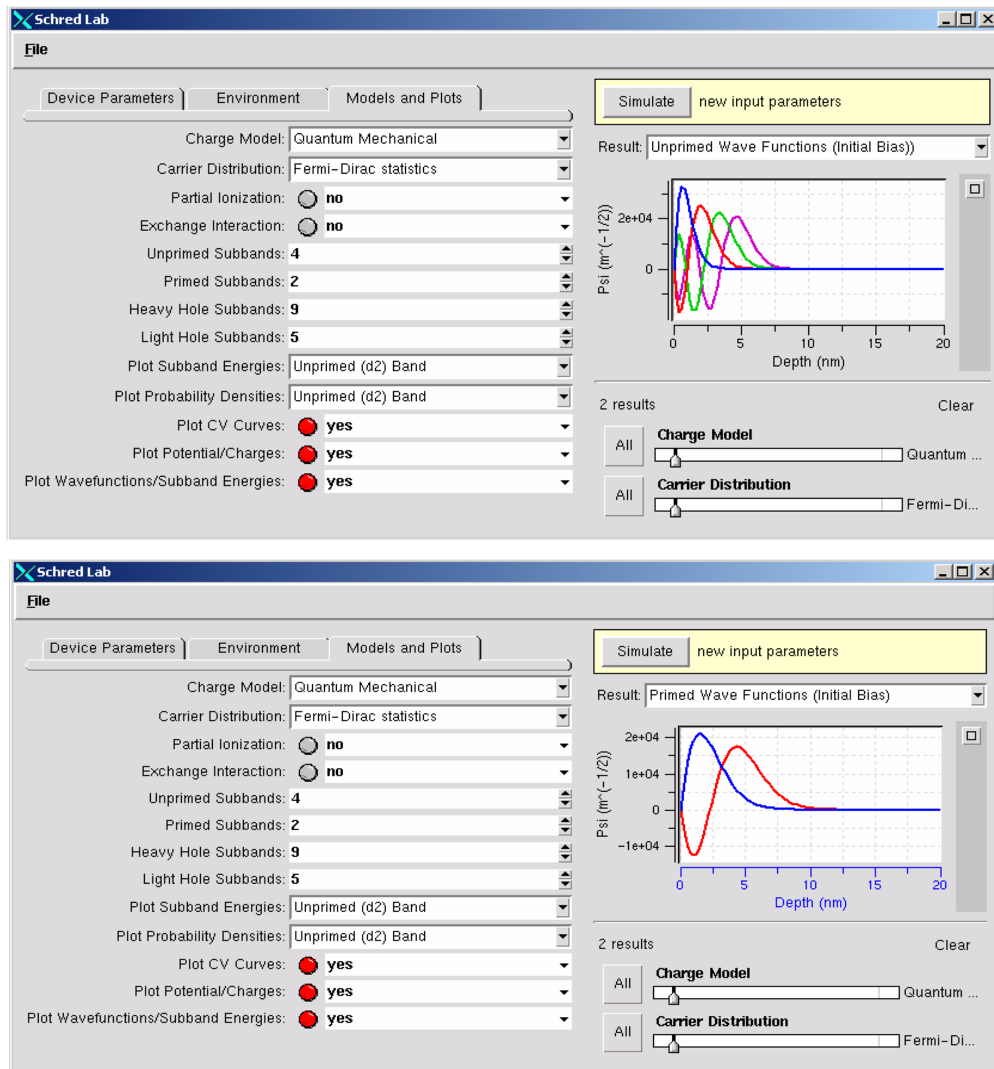


Figure 2.10. Wavefunctions corresponding to the lowest 4 subbands from unprimed (Δ_2) ladder of subbands (top panel), and wavefunctions corresponding to the lowest two subbands from the primed (Δ_4) ladder of subbands.

2.2.3 Example 3: MOS Capacitor – Poly-Depletion and Quantum-Mechanical Effects

In this example we also consider a simple MOS capacitor. The gate is made of n+ polysilicon in this case, the thickness of the SiO2 layer is t_{ox}=2 nm and the doping of the p-type substrate is $N_A=5\times10^{18}$ cm^{-3}. The doping of the polysilicon gate equals $N_D=5\times10^{19}$ cm^{-3}, which is on the low side. For this device structure we plot:

(a) The conduction band profile for applied bias V_G=2 V (Figure 2.11)

(b) Total charge density for applied bias V_G=2 V (Figure 2.12)

(c) The electric field profile for applied bias V_G=2V (Figure 2.13)

(d) The gate voltage variation of the low-frequency total gate capacitance when using semiclassical and quantum-mechanical model for the charge description. Vary V_G between -2V and 3V

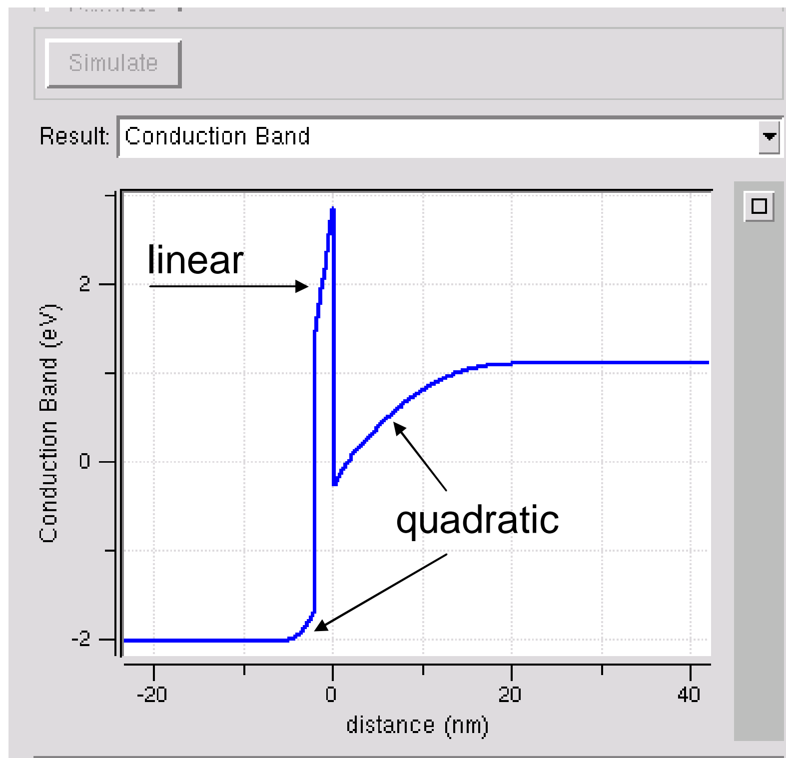


Figure 2.11. Conduction band profile for V_G=2 V.

First we discuss the conduction band edge variation (Figure 2.11). Because of the constant doping in the semiconductor and the polysilicon gate, the potential varies quadratically in these two regions. Since there are no charges in the oxide, the potential variation there is linear. When the doping of the polysilicon gate increases, the gate itself behaves more like a metal and there is smaller voltage drop across the poly-gate depletion region.

Next we examine the charge density variation (Figure 2.12). Charge density is constant under depletion conditions until it starts decaying exponentially with the extrinsic Debye length. Inversion charge density in the semiconductor decays exponentially from the sc/oxide interface. Under depletion conditions there is either none or very small electron charge density; therefore, the inversion layer contribution to the total charge density in the semiconductor is negligible.

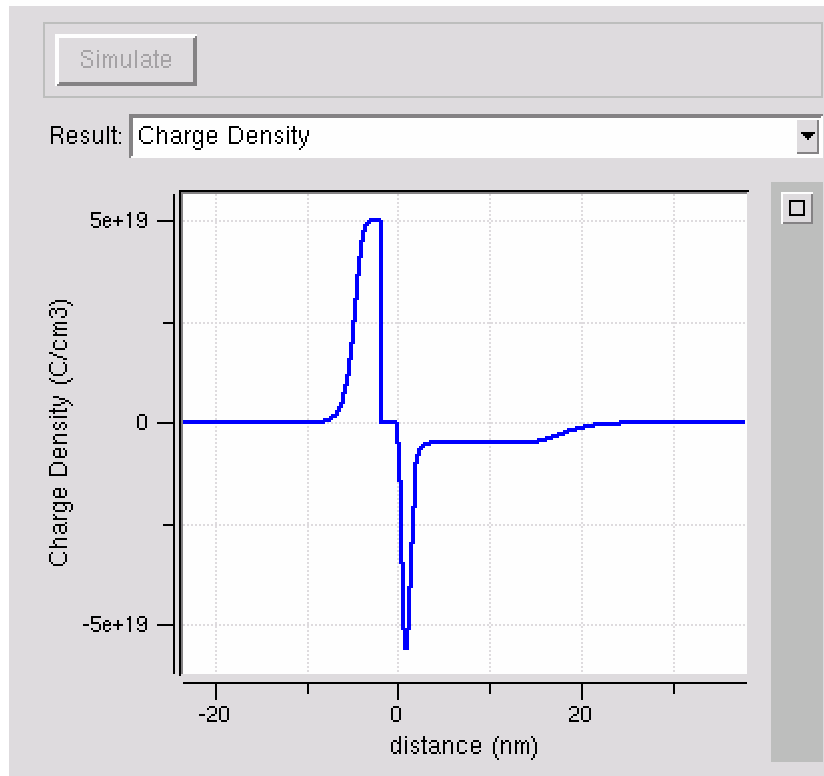
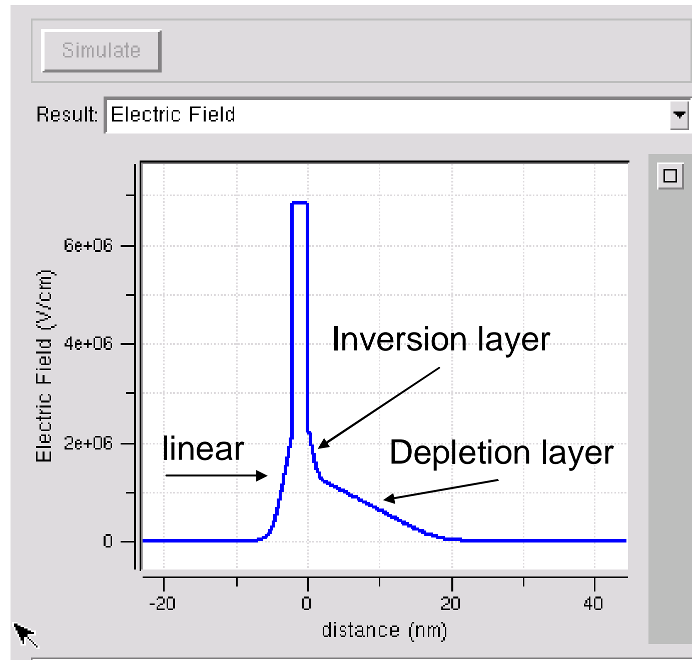


Figure 2.12. Total charge density variation for V_G=2 V.

The electric field varies linearly in the polysilicon gate and the silicon substrate and it is constant in the oxide that is free of charges (Figure 2.13). The electric field in the

oxide vs. the electric field in the semiconductor for zero interface charge equals the ratio of the semiconductor vs. oxide dielectric constant, which for the case of Si/SiO_2 system is approximately 3, i.e. the oxide field is three times larger than the semiconductor field at the interface.



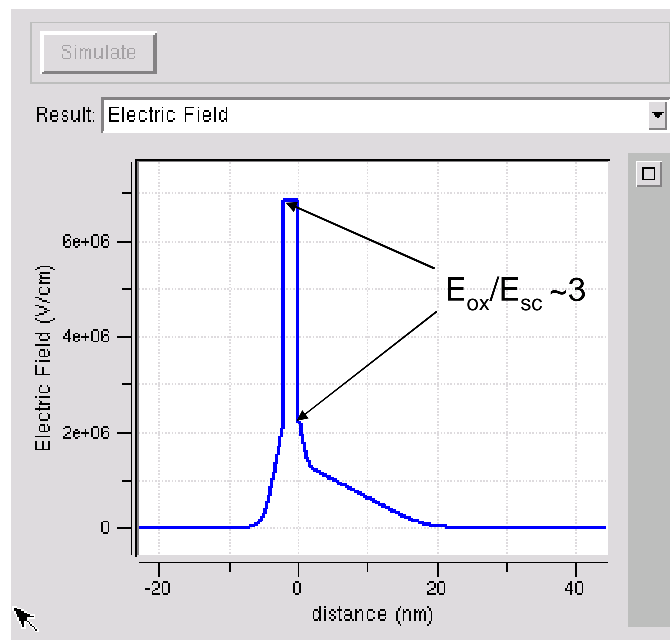


Figure 2.13. Electric field variation for V_G=2 V.

The low-frequency CV curve goes from accumulation through depletion towards inversion mode. Note that the threshold voltage for the semiclassical model is ~0.75 V assuming that the minimum in the capacitance denotes the maximum in the threshold voltage. For quantum-mechanical model it is ~ 1V; therefore the use of the quantum model gives rise to threshold voltage shift of about 250 mV, which is significant and physically justified value. In inversion, there is about 10% degradation of the total gate capacitance when using the quantum-mechanical model.

There are other features that have been observed while preparing this example. In inversion, if the gate is metal, the capacitance degradation is almost constant and can be accounted for by using effective oxide thickness $t_{eff} > t_{ox}$. For the case of a poly-gate, the low-frequency capacitance in inversion conditions has pronounced gate voltage dependence and the total gate capacitance C_{tot} decreases with increasing V_G. Because of this, nowadays state-of-the-art MOSFETs use metal gates.

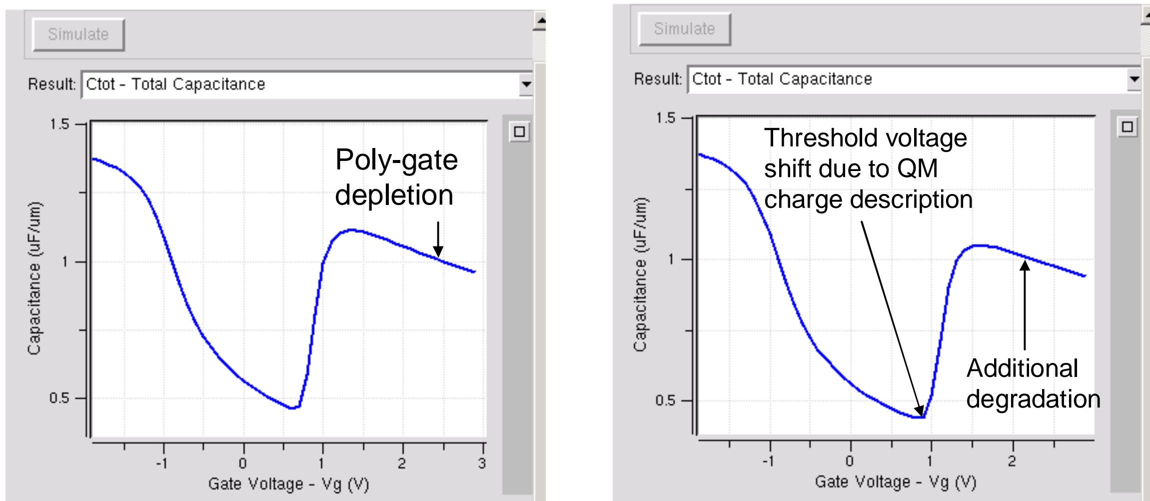


Figure 2.14. Inversion layer capacitance when using semiclassical (left panel) model for the charge description and the quantum-mechanical (right panel) model for the charge description vs gate bias.

2.2.4 Advanced Exercise 1: MOS Capacitors - Variation of the threshold voltage shift with doping.

In this example we want to elaborate on the variation of the threshold voltage shift with substrate doping when using quantum-mechanical vs. semi-classical models for the inversion layer electrons. For that purpose, we consider a simple MOS capacitor structure with aluminum gate. The thickness of the oxide region equals 4 nm and the substrate is p-type with doping N_A that varies between 10^{16} cm^{-3} and 10^{19} cm^{-3}. Using SCHRED we consider two cases for the charge description in the semiconductor: semi-classical with Fermi-Dirac statistics and quantum-mechanical model. We follow these steps to arrive at a plot that gives us the shift in the threshold voltage versus N_A due to quantum-mechanical charge description: We assume that the threshold voltage equals the gate voltage V_G for which the sheet electron density equals 10^{12} cm^{-2}. We then register the V_G values for both quantum and classical model and subtract V_G(classical) from V_G(quantum). The threshold voltage shift variation vs. substrate doping that we arrive at is shown in Figure 2.15 where we also add experimental data. As expected, the threshold voltage shift increases for higher substrate doping densities for which we have more pronounced quantum mechanical effects.

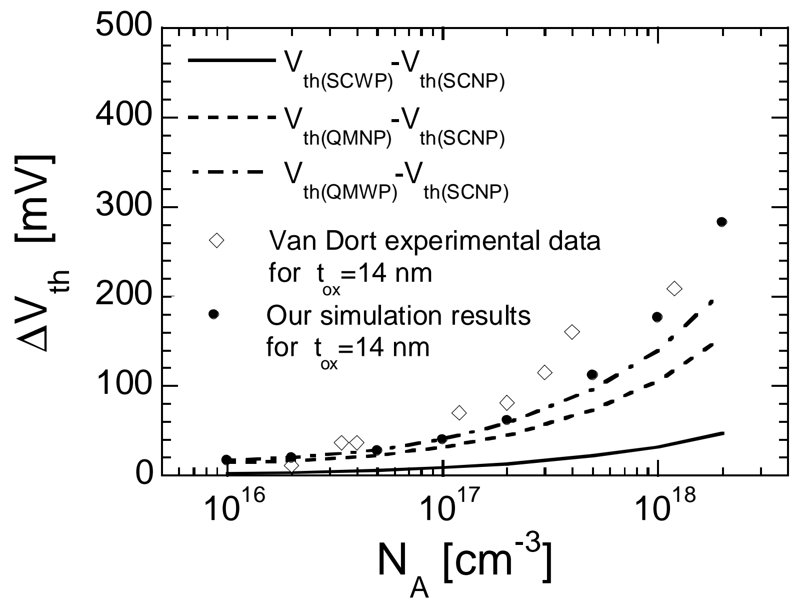


Figure 2.15. Threshold voltage shift vs. substrate doping.

2.2.5 Advanced Exercise 2: MOS Capacitors – Total capacitance degradation vs. different technology

It is well known that the degradation of the total gate capacitance versus the inversion layer capacitance becomes more pronounced when scaling the device dimensions mainly due to increase in the substrate doping and the decrease of the oxide capacitance. This, in turn, leads to a degradation of the device transconductance, which determines the device on-state current. For simplicity we will assume in this example that the doping does not change for different technology nodes ($N_A=10^{18}$ cm^{-3}), but the oxide thickness changes. Following the steps outlined below we arrive at a plot that describes capacitance degradation versus technology node:

We first calculate the low-frequency CV-curves for gate voltage between 0 and 3V using SCHRED simulator and both classical and quantum-mechanical model for the charge in the channel. We then register the value of the low-frequency curve for applied bias V_G=2.5 V and calculate the ratio of C(quantum) versus C(classical). In Figure 2.16, we show simulated C_{tot} to oxide capacitance C_{ox} for metal/*p*-substrate and *n*+-poly/*p*-substrate MOS capacitors, as a function of the physical oxide thickness t_{ox} and the doping of the polysilicon gates N_D, assuming V_G=3 V. The high value for V_G, used here, may overestimate the severity of the bias dependent attenuation for thinner oxides, but a consistent value for V_G is useful for the purpose of tabulating the simulated results. The results shown clearly demonstrate that classical charge model and Maxwell-Boltzmann (non-degenerate) statistics are clearly inadequate for oxide thickness below 10 nm. Even use of Fermi-Dirac statistics in the classical charge description can lead to significant errors in the estimate of the total gate capacitance for devices with metal gates and oxide thickness less than 5 nm, due to the higher surface fields and, therefore, pronounced quantum-mechanical size-quantization effect in the channel. For example, the classical model that uses Maxwell-Boltzmann (Fermi-Dirac) statistics predicts that, for the device with t_{ox} = 1 nm, C_{tot}/C_{ox} = 0.983 (0.882). On the other hand, the quantum-mechanical model predicts that C_{tot}/C_{ox} =0.795, which leads to relative error of 23.65 (10.94) %. As

previously noted, the depletion of the poly-silicon gates will further degrade the total gate capacitance.

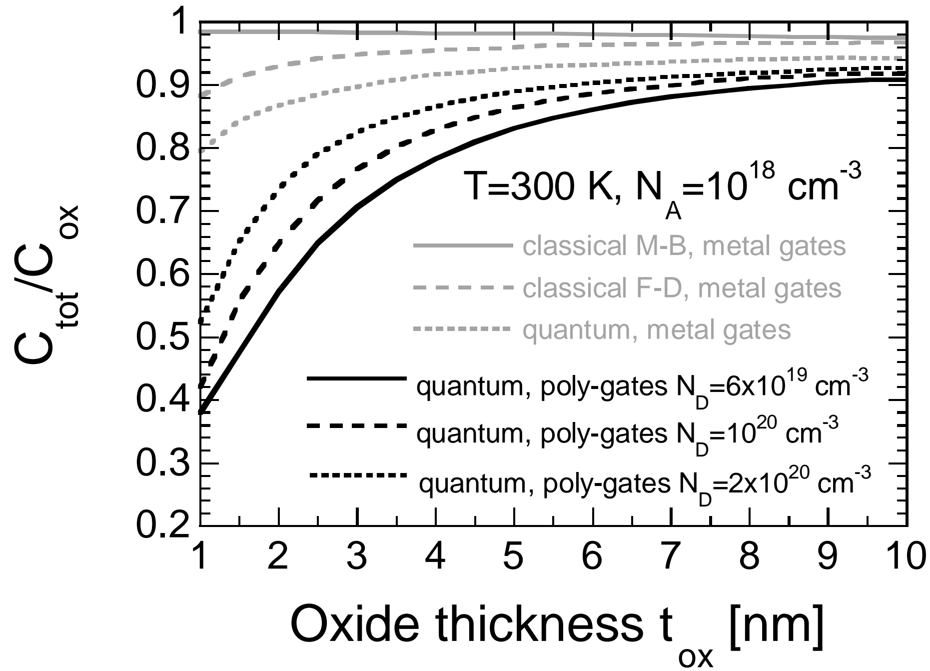


Figure 2.16. Simulated C_{tot} to oxide capacitance C_{ox} for metal/*p*-substrate and *n*+-poly/*p*-substrate MOS capacitors, as a function of the physical oxide thickness t_{ox} and the doping of the polysilicon gates N_D. We use V_G =3 V.

3. Dual-Gate Capacitors Description and SCHRED Examples

3.1 Need for Dual-Gate Capacitors

3.2 SCHRED Examples for Dual-Gate Capacitors

3.2.1 Example 1: DG Capacitor – Influence of Back Gate

3.2.2 Example 2: DG Capacitor – Quantum-Mechanical Charge Density

3.2.3 Example 3: DG Capacitor - Capacitance and Threshold Voltage

3.1 Need for Dual-Gate Capacitors

For digital circuits, a figure of merit for MOSFETs for unloaded circuits is CV/I , where C is the gate capacitance, V is the voltage swing, and I is the current drive of the MOSFET. For loaded circuits, the current drive of the MOSFET is of paramount importance. Keeping in mind both the CV/I metric and the benefits of a large current drive, we note that device performance may be improved by: (1) inducing a larger charge density for a given gate voltage drive; (2) enhancing the carrier transport by improving the mobility, saturation velocity, or ballistic transport; (3) ensuring device scalability to achieve a shorter channel length; and (4) reducing parasitic capacitances and parasitic resistances. For capitalizing these opportunities, the proposed technology options generally fall into two categories: (I) new materials and (II) new device structures. In many cases, the introduction of a new material requires the use of a new device structure, or vice versa. To fabricate devices beyond current scaling limits, IC companies are simultaneously pushing the planar, bulk silicon CMOS design while exploring alternative gate stack materials (high-*k* dielectric[i] and metal gates), band engineering methods (using strained Si[ii,iii,iv] or SiGe[5]), and alternative transistor structures. The concept of a band-engineered transistor is to enhance the mobility of electrons and/or holes in the channel by modifying the band structure of silicon in the channel in a way such that the physical structure of the transistor remains substantially unchanged. The enhanced mobility increases the transistor transconductance (g_m) and on-drive current (I_{on}).

The challenge in identifying suitable high-*k* dielectrics and metal gates for both conventional PMOS (*p*-channel MOS) and NMOS (*n*-channel MOS) transistors has led to early adoption of alternative transistor designs (see Figure 3.1). These include primarily partially-depleted (PD) and fully-depleted (FD) silicon-on-insulator (SOI) devices. Today there is also an extensive research in double-gate (DG) structures, and FinFET transistors[v], which have better electrostatic integrity and theoretically have better transport properties than single-gated FETs. A FinFET is a form of a double gate transistor having surface conduction channels on two opposite vertical surfaces and having current flow in the horizontal direction. The channel length is given by the horizontal separation between source and drain and is usually determined by a

lithographic step combined with a side-wall spacer etch process. Many innovative structures, involving structural challenges such as fabrication on nanometer-scale fins and nanometer-scale planarization over an entire wafer, are currently under investigation. In conclusion, the semiconductor industry is approaching the end of an era of scaling gains by rote shrinkage of device dimensions, and entering a post-scaling era, a new phase of CMOS evolution in which innovation is demanded simply to compete. The trends in benefits to density, performance, and power will be continued through such innovations. Rather than coming to a close, a new era of CMOS technology is just beginning. Table 3.1[vi] summarizes the advantages and challenges of some of the above-mentioned device structures.

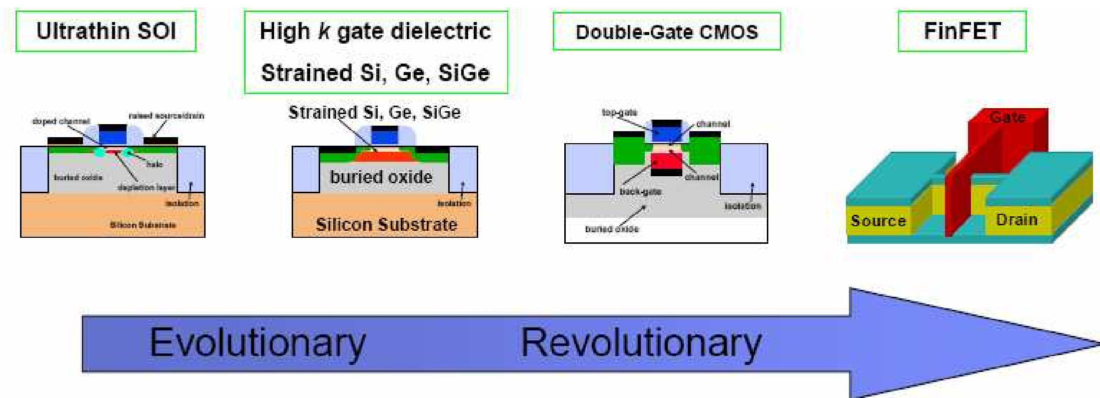


Figure 3.1 Method II for improving device performance – Introduction of new device structures.

Table 3.1 Properties of different transistor designs.

Device	**Ultrathin Body (UTB) SOI**	**Band-Engineered Transistor**	**Vertical Transistor**	**FinFET**	**Double-Gate**
Concept	Fully-depleted SOI	SiGe or Strained Si; bulk Si or SOI	Double-gate or surround-gate structure		

Application/ Driver	Higher performance, higher transistor density, lower power dissipation			
Advantages	Improved subthreshold slope; V_T controllability	Higher drive current; compatible with bulk Si and SOI	Higher drive current; lithography independent gate length	Higher drive current; Improved subthreshold slope; improved short-channel effect (SCE)
Scaling Issues	Si film thickness, gate stack; worse SCE than bulk CMOS	High mobility film thickness (SOI); gate stack; integratability	Si film thiness; gate stack; integratability; process complexity; accurate TCAD	Gate alignment; Si film thickness; gate stack; integratability; process complexity; accurate TCAD
Design Challenges	Device characterization; compact model and parameter extraction	Device characterization	Device characterization; PD versus FD; compact model and parameter extraction; applicability to mixed signal applications	

3.2 SCHRED Examples for Dual-Gate Capacitors

In this section several examples will be given to outline the operation of dual-gate capacitors that are integral part of dual-gate MOSFET devices, both vertical and in-plane. In Example 1 we examine the influence of the back-gate on the dual-gate capacitor electrostatics. In Example 2 we discuss volume inversion and threshold voltage shift is analyzed in Example 3.

3.2.1 Example 1: DG Capacitor – Influence of Back Gate

We consider a dual gate (DG) capacitor under equilibrium conditions. The gate is metal gate with default value of the metal workfunction, the thickness of the front and back SiO_2 layers is t_{ox}=10 nm and the doping of the p-type substrate is $N_A=10^{17}$ cm^{-3}. For this device structure, using classical charge model, we examine the influence of the back gate by plotting (a) The conduction band profile for V_{GF} = V_{GB}= 1.5 V, and (b) The electric field profile for V_{GF} = V_{GB}= 1.5 V. We then comment on the influence of the back gate when the body thickness equals 10nm, 25nm, 50nm, 100nm, 150nm, 200nm, 250 nm, and 500nm.

From the results presented in Figure 3.2 we may conclude that the electrostatic potential underneath the front gate is not influenced by the presence of the back gate (given the back gate bias) for body thickness larger than approximately 250 nm.

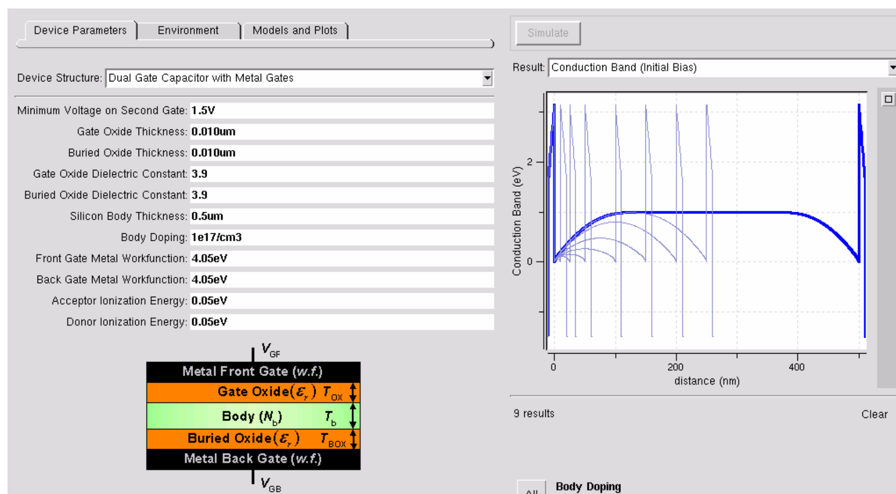


Figure 3.2. Conduction-band edge for dual-gate capacitors with different body thickness.

The same observation can be deduced from the simulation results for the electric-field profile in the dual-gate structure that are shown in Figure 3.3 for different body thickness. As in MOS capacitors, first observation is that the electric field is constant in the oxide regions and varies linearly in the semiconductor because of the constant body doping. Zero electric field denotes neutral region, which suggests that the front and back depletion regions are separated by a neutral region when the body thickness is larger than 250 nm. Thus, above this critical body thickness the back gate electrostatics does not influence the front gate electrostatics. The same observation can be drawn by looking at the total charge density (Not shown here).

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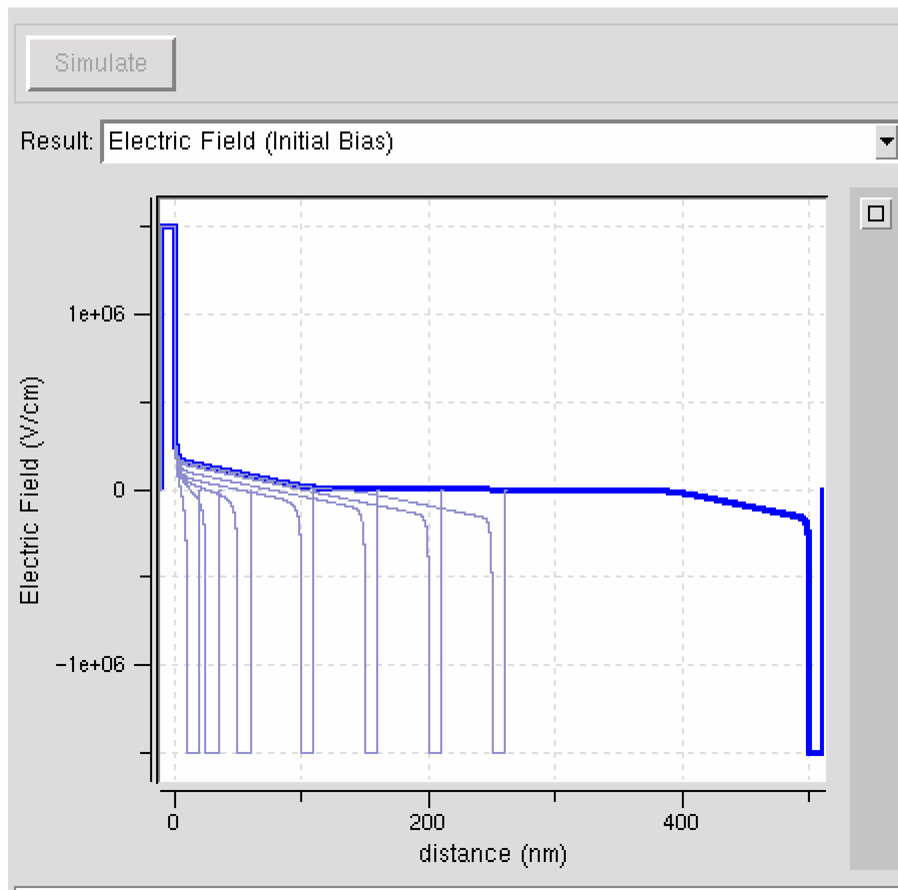

Figure 3.3. Electric field profiles for dual-gate capacitors with different body thickness.

3.2.2. Example 2: DG Capacitor – Quantum Charge Model and Volume Inversion

In this example we consider a dual gate (DG) capacitor under equilibrium conditions. The gate is metal gate with default value of the metal workfunction, the thickness of the front and back SiO_2 layers is t_{ox}=1 nm and the doping of the p-type substrate is $N_A=10^{18}$ cm^{-3}. For this device structure, using quantum-mechanical charge model, we examine the influence of the back gate and the charge distribution with body thickness by plotting:

(a) The conduction band profile for $V_{GF} = V_{GB}$= 1 V and body thickness of 40 nm.

(b) The spatial extent of the lowest-lying occupied states for body thickness of 40nm, 10nm and 4nm.

(c) The total charge density for body thickness of 40nm, 10nm and 4nm.

. From the simulation results for the conduction band presented in Figure 3.4 we find that even when we use quantum-mechanical model for the charge distribution in the channel, the electrostatic potential underneath the front gate is not influenced by the presence of the back gate for body thickness of 40 nm, front and gate bias of 1 V and body doping of 10^{18} cm^{-3}.. The same observation is seen from the simulation results for the wavefunctions from the unprimed and primed ladder of subbands that are given in Figure 3.5.

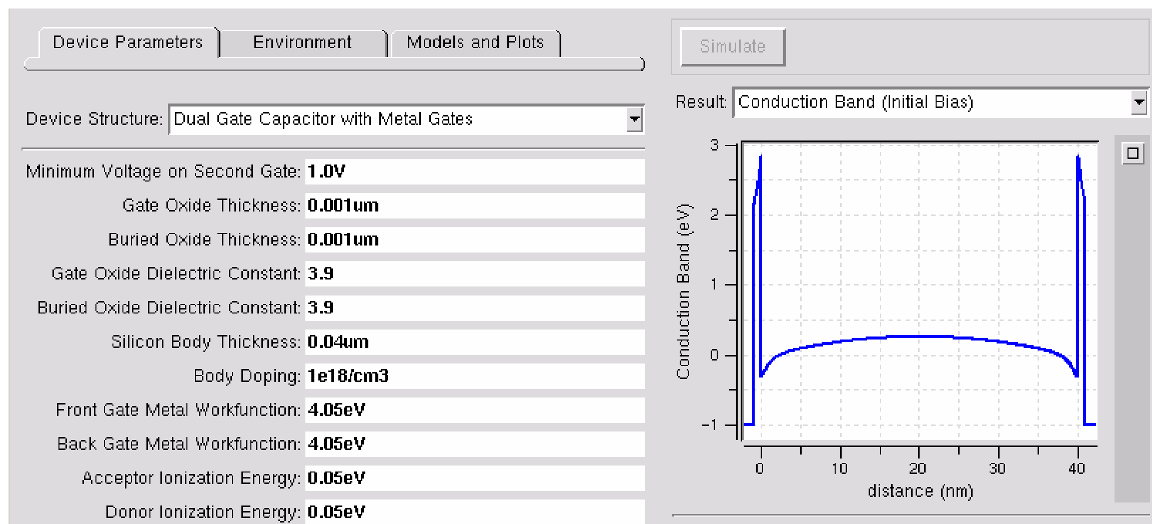

Figure 3.4 Conduction band profile for body thickness 40 nm.

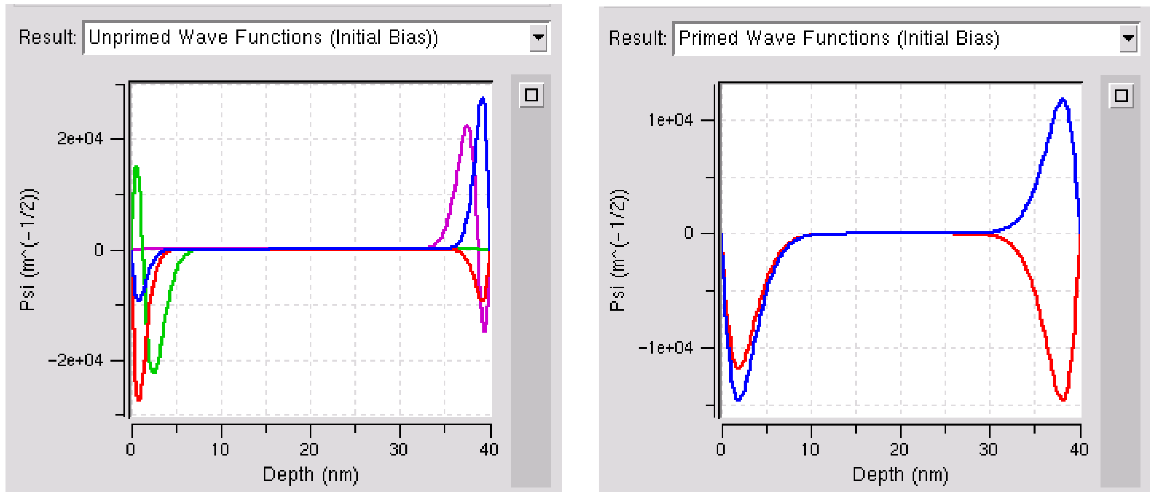

Figure 3.5 Spatial variation of the wavefunctions for body thickness 40 nm.

For 10 nm width of the body, the front and back channel begin to talk to each other, thus influencing the form of the wavefunctions. There is no quasi-neutral region in the middle portion of the body (see Figure 3.6).

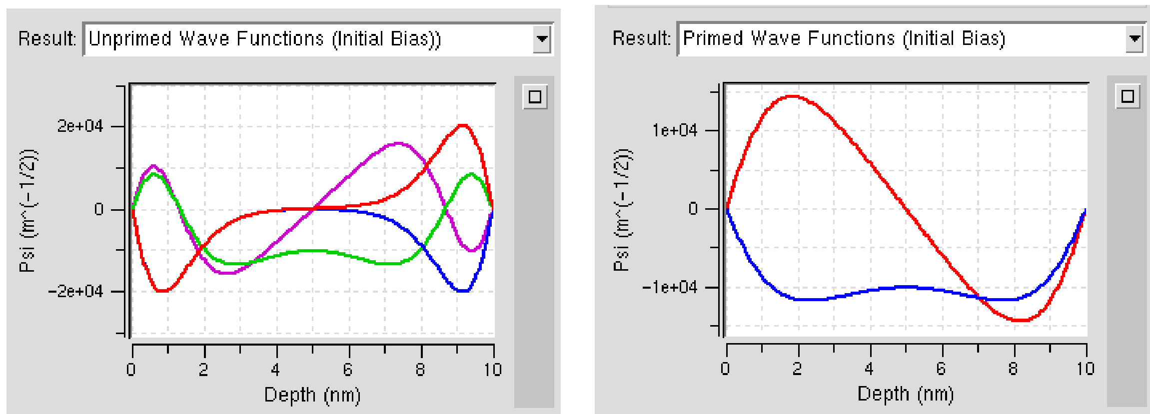

Figure 3.6 Spatial variation of the wavefunctions for body thickness 40 nm.

.For 4 nm body thickness, the quasi-neutral region in the middle completely disappears and due to the volume inversion there is smaller charge density in the vicinity of the front and back semiconductor/oxide interface (see Figure 3.7). We say that we have volume inversion in this system. When the system is in the volume inversion mode the importance of interface roughness could decrease if the body thickness is not too small.

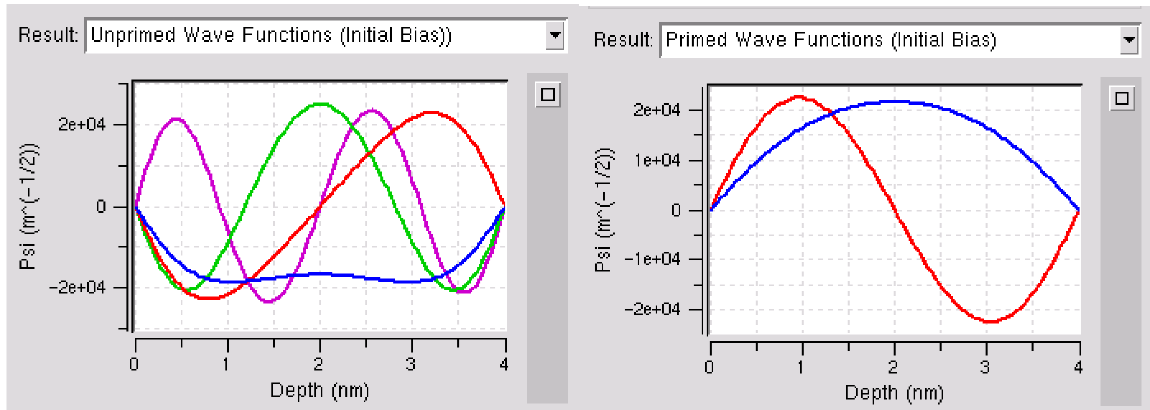

Figure 3.7 Spatial variation of the wavefunctions for body thickness 4 nm

The importance of interface-roughness scattering can also be seen on the total charge density plots that are given in Figure 3.8.

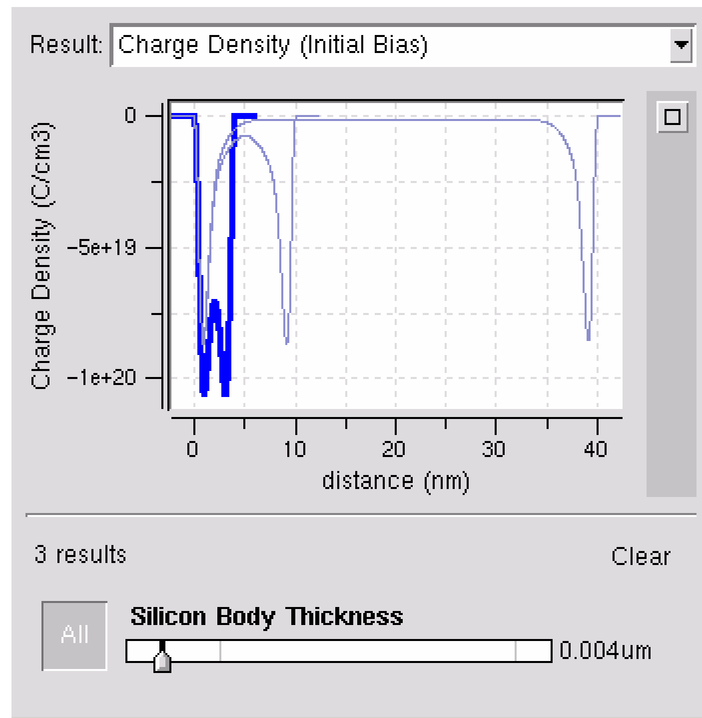

Figure 3.8 Spatial variation of the total charge density calculated using quantum-mechanical model for the charge description.

From the results presented in Figure 3.8 we see that, when decreasing the body thickness from 40 nm down to 4 nm there is a significant change in the charge distribution in the

body. For 40 nm body thickness two independent parallel channels are present. For body thickness of 10 nm and smaller, the quasi-neutral region in the middle portion of the body vanishes and the two channels begin to merge. This is more evident for body thickness of 4 nm in which case we practically have a single channel and more charge density in the middle portion of the body (volume inversion).

3.2.3 Example 3: DG Capacitor - Capacitance and Threshold Voltage

In this example too, we consider a dual gate (DG) capacitor. The gate is metal gate with default value of the metal workfunction, the thickness of the front and back SiO2 layers is t_{ox}=1 nm and the doping of the p-type substrate is $N_A=10^{18}$ cm^{-3}. For this device structure, using both semi-classical and quantum-mechanical charge model we examine:

(a) The variation of the total gate capacitance as a function of the charge model

(b) The shift in the threshold voltage with body thickness.

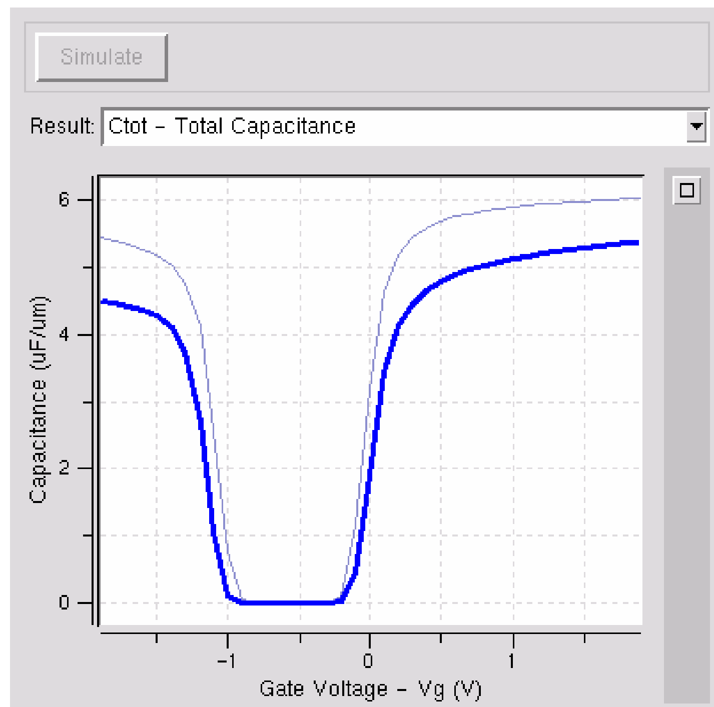

Figure 3.9 Total gate capacitance when using semi-classical charge model (thin line) and quantum-mechanical charge model (thick line).

As shown in Figure 3.9, similar to single-gate capacitors, the use of the quantum model leads to increase of the average distance of the carriers from the interface and degradation of the total gate capacitance for both positive and negative gate bias. The back gate voltage was set to -2 V in these simulations. The more pronounced quantum-mechanical nature of the charge transport in DG-capacitors with smaller body thickness leads to larger shift in the threshold voltage, which is in agreement with experimental findings (Figure 3.10).

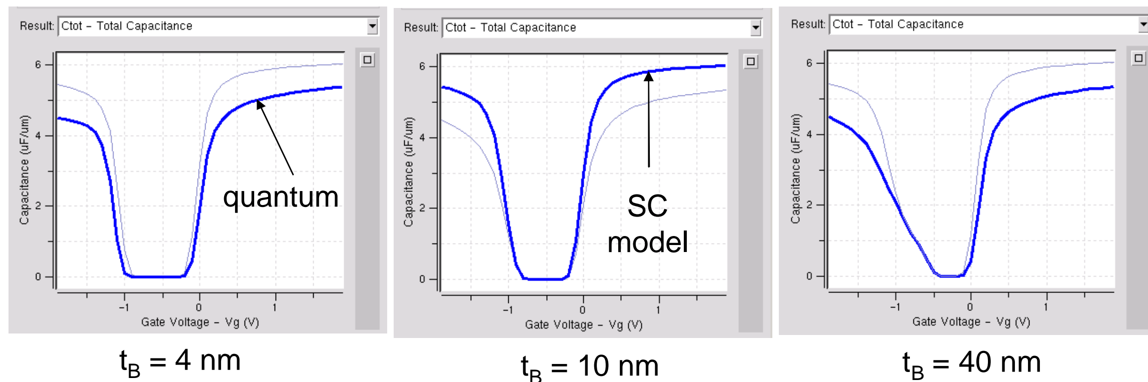

Figure 3.10 Inversion layer capacitances for different body thickness. As in Figure 3.9, semi-classical charge model is represented with thin line and quantum-mechanical charge model is represented with thick line.

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