SCHRED Exercises

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It is well known that the degradation of the total gate capacitance versus the in- version layer capacitance becomes more pronounced when scaling the device dimensions mainly due to increase in the substrate doping and the decrease of the oxide capacitance. This, in turn, leads to a degradation of the device transconductance, which determines the device on-state current. For simplicity we will assume that the doping does not change for different technology nodes (NA=1018 cm-3), but the oxide thickness changes. Follow these steps to arrive at a plot that describes capacitance degradation versus technology node:

(1) Calculate the low-frequency CV-curves for gate voltage between 0 and 3V using SCHRED simulator and both classical and quantum-mechanical model for the charge in the channel. Register the value of the low-frequency curve for applied bias VG=2.5 V. Calculate the ratio of C(quantum) versus C(classical).
(2) Plot this ratio versus oxide thickness that is varied between 1 and 10 nm. Comment on the results and compare with experimental data.