NCN@Purdue - Intel Summer School: July 14-25, 2008

Physics of *Nanoscale Transistors: Lecture 1:*

A Review of MOSFET Fundamentals

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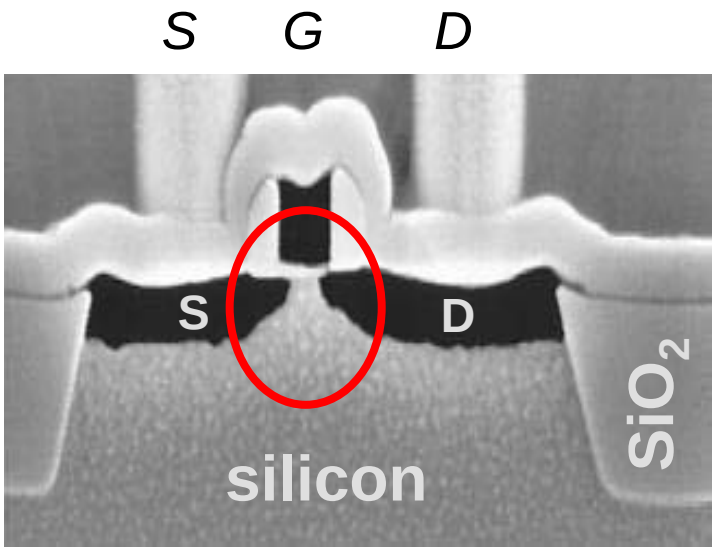
outline

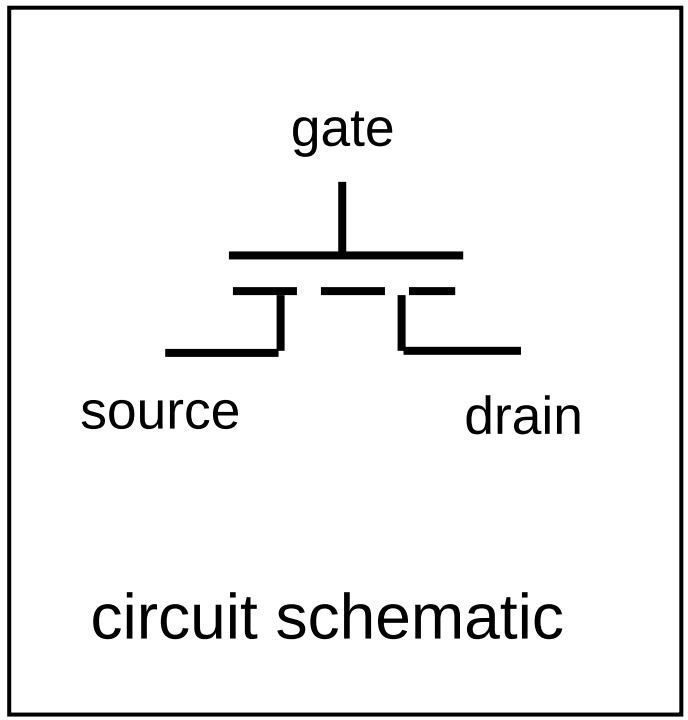
1) Introduction
2) MOSFET theory
3) Device performance metrics
4) The barrier model of a MOSFET
5) Carrier transport in MOSFETs
6) Summary

transistors

physical structure



(Texas Instruments, 1997)



"The transistor was probably the most important invention of the 20th century," Ira Flatow, Transistorized! www.pbs.org/transistor

MOSFETs

For representative dimensions and parameters of current and future MOSFETs, see:

International Technology Roadmap for Semiconductors (ITRS)

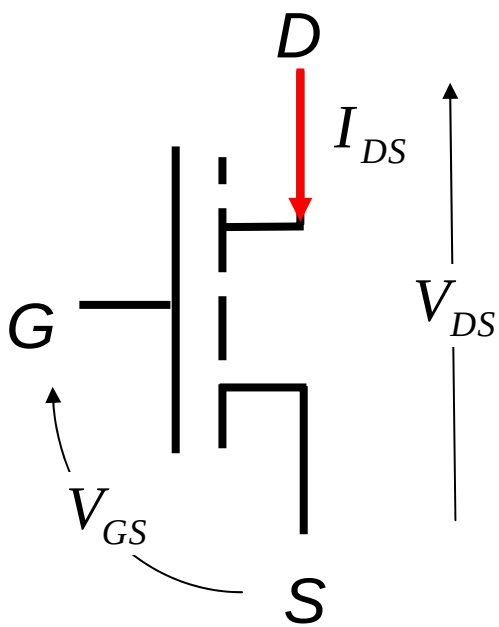
especially the chapter:

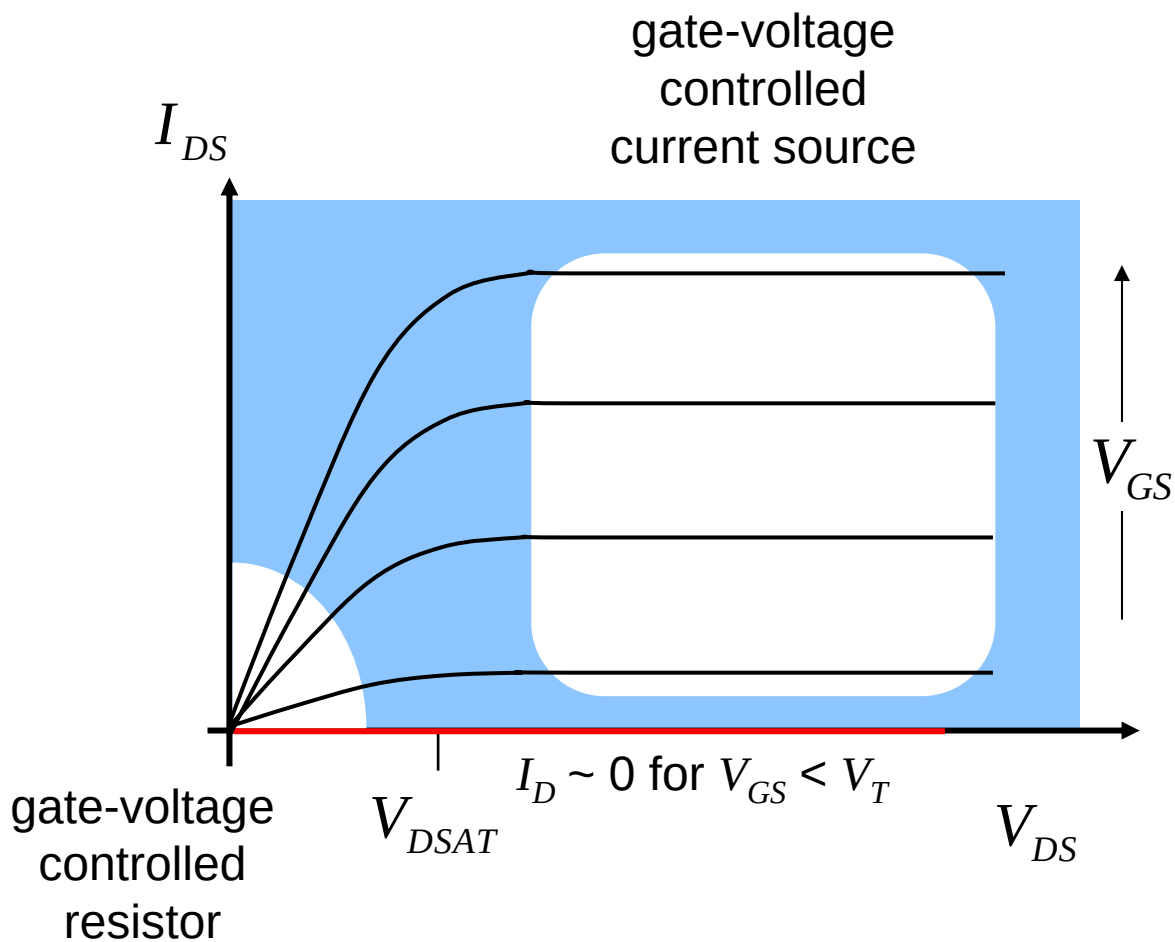
PIDS: Process Integration and Device Sciences.

http://public.itrs.net

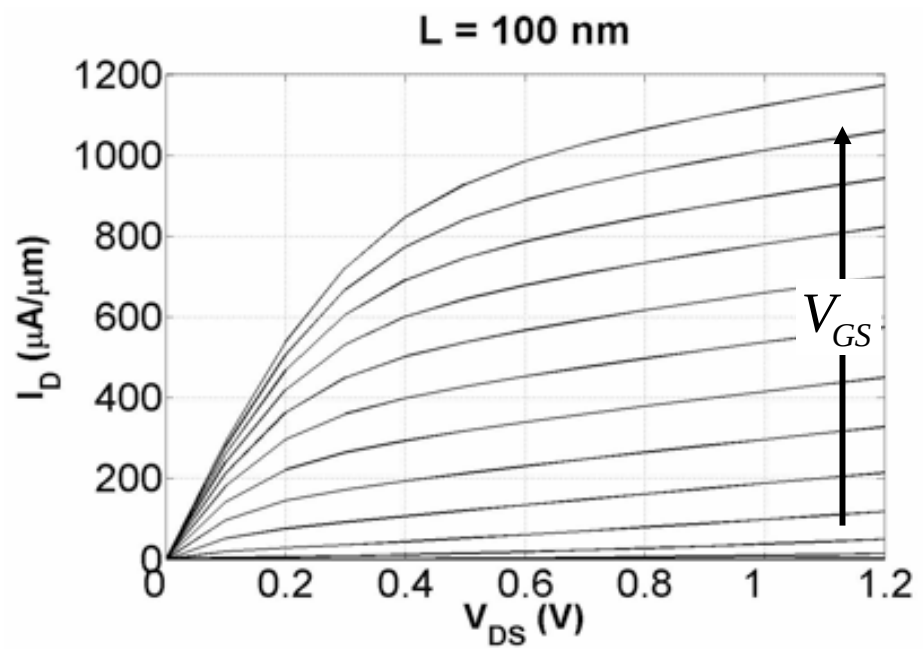
IV characteristics

circuit symbol

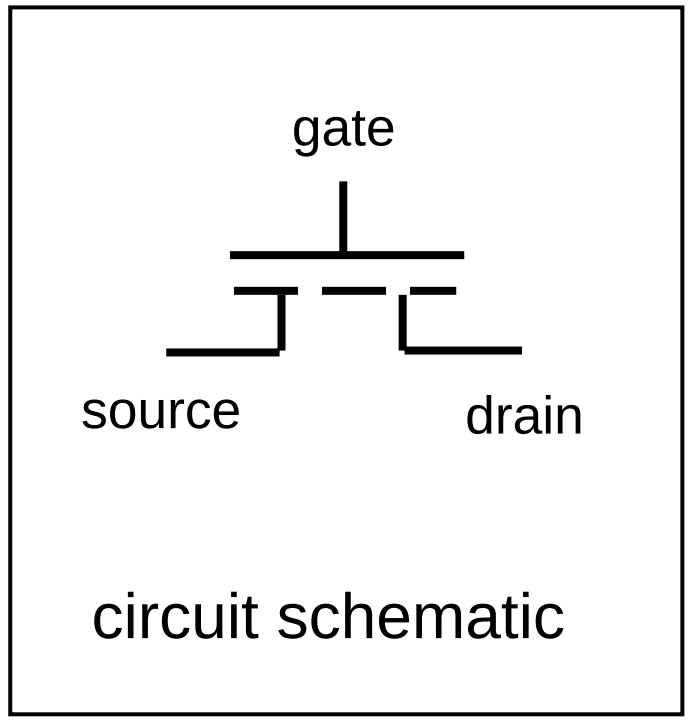




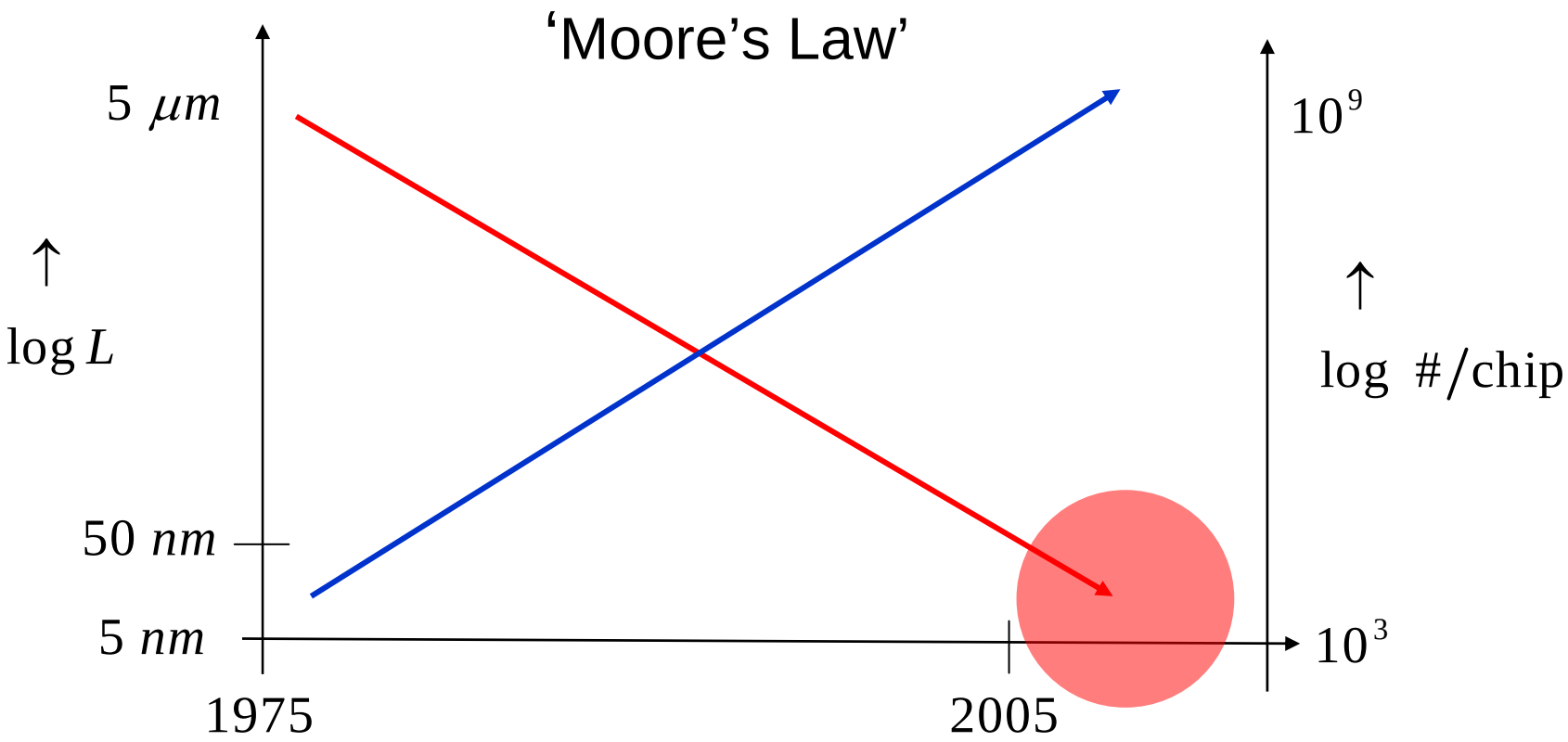
IV characteristic: real



(Courtesy, Shuji Ikeda, ATDF, Dec. 2007)



MOSFET technology evolution



see: http://www.intel.com/technology/mooreslaw/index.htm

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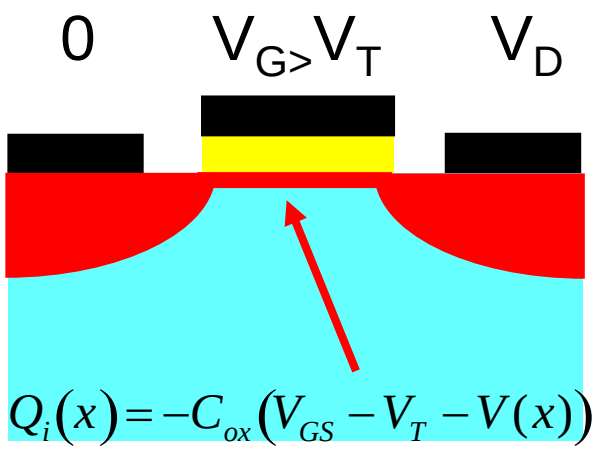
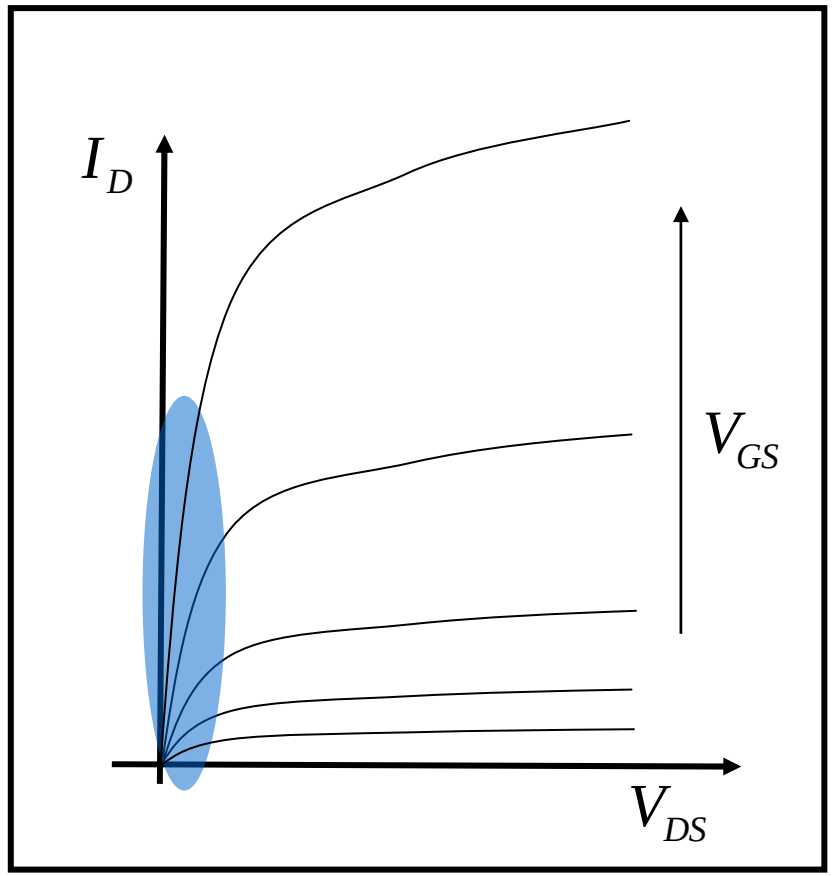
MOSFET IV: low V_{DS}





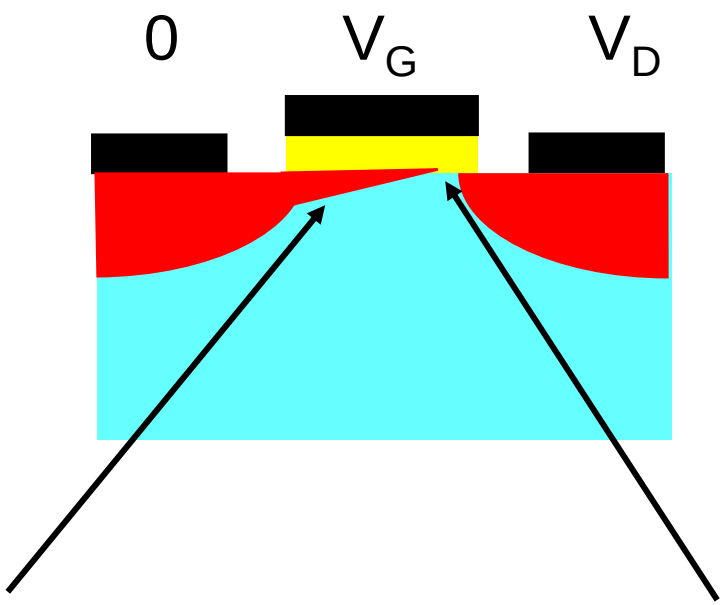
$$I_D = W\, Q_i(x)\, \upsilon_x(x)$$

$$I_D = W\, C_{ox}(V_{GS} - V_T)\mu_{eff}\mathcal{E}_x$$

$$\mathcal{E}_x = \frac{V_{DS}}{L}$$

$$I_D = \frac{W}{L}\mu_{eff} C_{ox}(V_{GS} - V_T)V_{DS}$$

MOSFET IV: 'pinch-off' at high V_{DS}

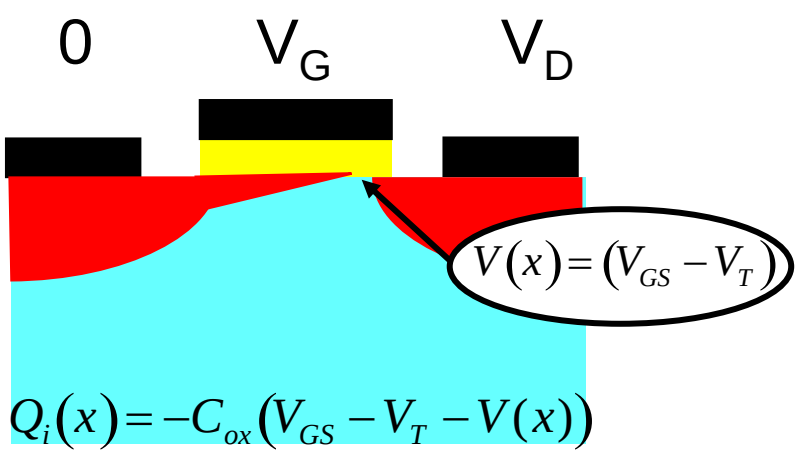


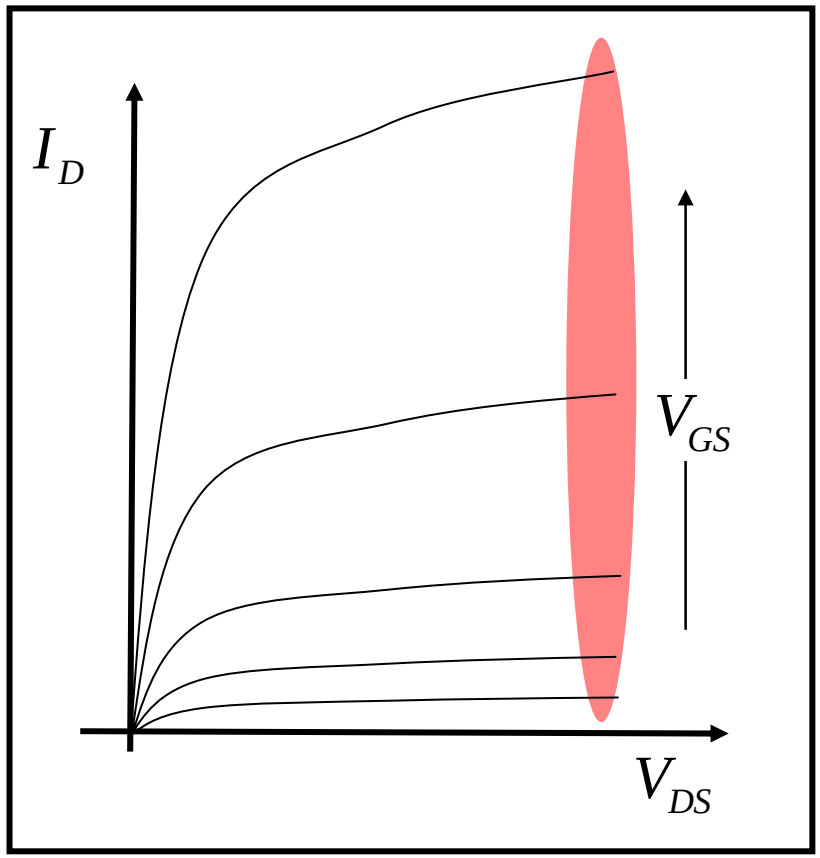
$$Q_i(x) = -C_{ox}\left(V_{GS} - V_T - V(x)\right)$$

$$V(x) = \left(V_{GS} - V_T\right)$$

$$Q_i(x) \approx 0$$

MOSFET IV: high V_{DS}





$$I_D = W\, Q_i(x)\upsilon_x(x) = W\, Q_i(0)\upsilon_x(0)$$

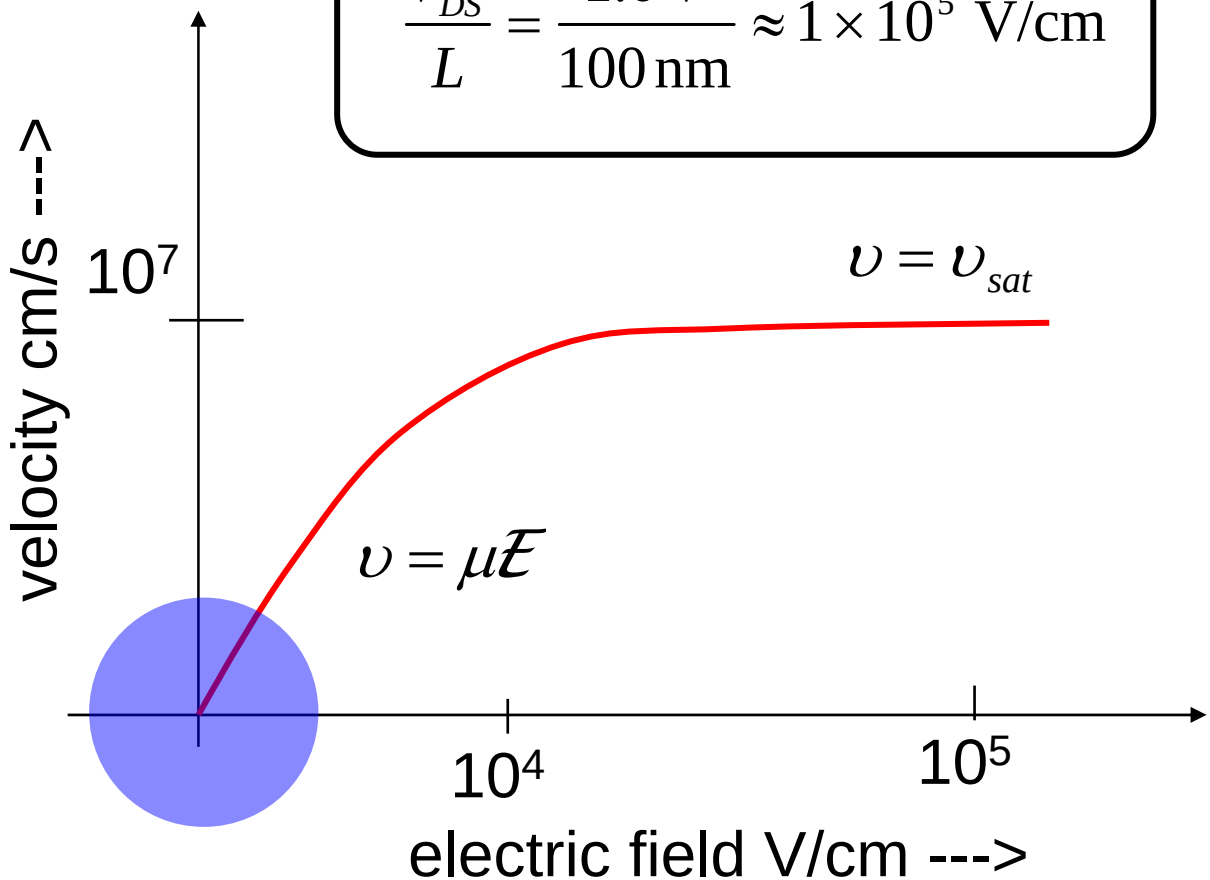
$$I_D = W\, C_{ox}\left(V_{GS} - V_T\right)\mu_{eff}\mathcal{E}_x(0)$$

$$\mathcal{E}_x(0) \approx \frac{V_{GS} - V_T}{L}$$

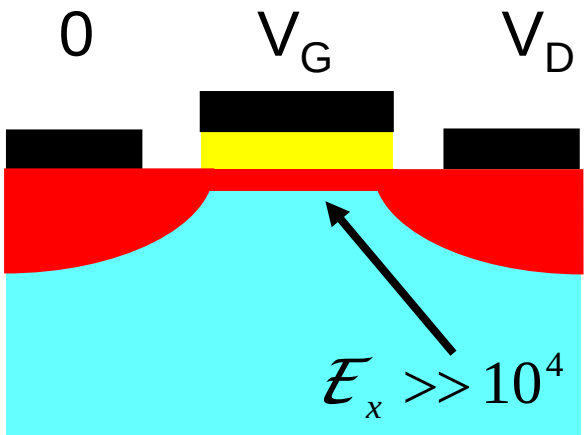
$$I_D = \frac{W}{2L}\mu_{eff} C_{ox}\left(V_{GS} - V_T\right)^2$$

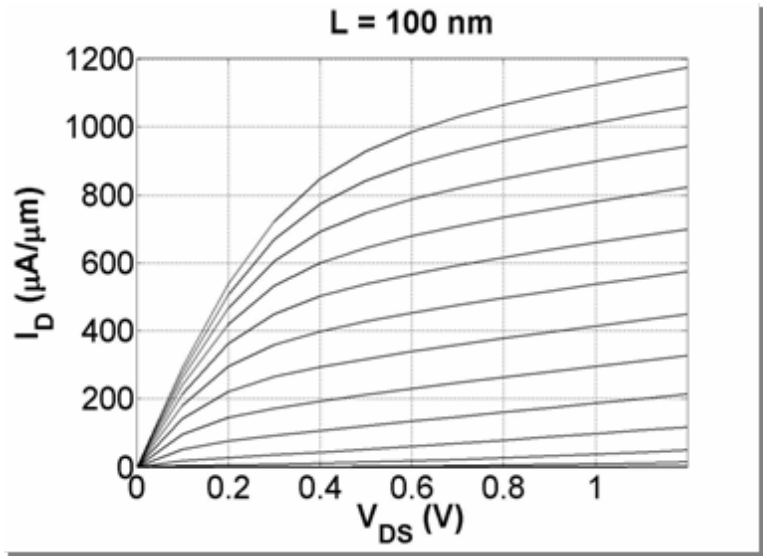
velocity saturation

$$\frac{V_{DS}}{L} = \frac{1.0\,\mathrm{V}}{100\,\mathrm{nm}} \approx 1 \times 10^5\ \mathrm{V/cm}$$



MOSFET IV: velocity saturation





(Courtesy, Shuji Ikeda, ATDF, Dec. 2007)

$$I_D = W\, Q_i(x)\, \upsilon_x(x)$$

$$I_D = W\, C_{ox}(V_{GS} - V_T)\, \upsilon_{sat}$$

$$I_D = W\, C_{ox}\, \upsilon_{sat}\,(V_{GS} - V_T)$$

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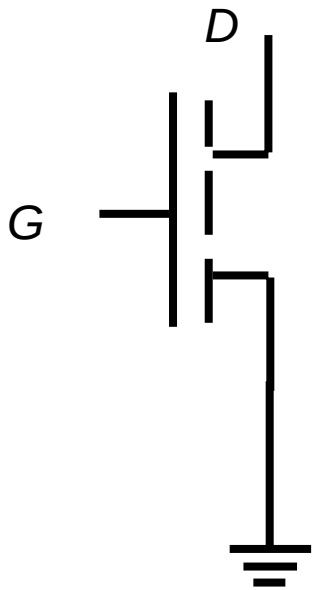
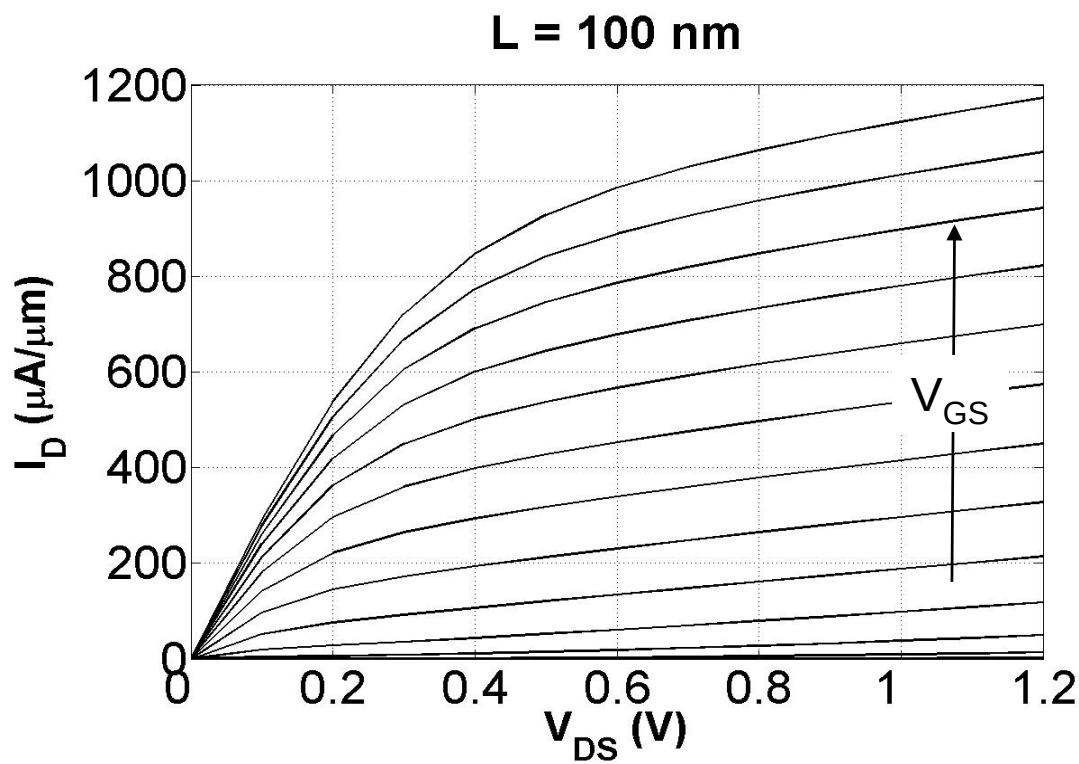
common source characteristics





1) ground source ($V_S = 0$)
2) set V_G
3) sweep V_D from 0 to V_{DD}
4) step V_G from 0 to V_{DD}

common source characteristics

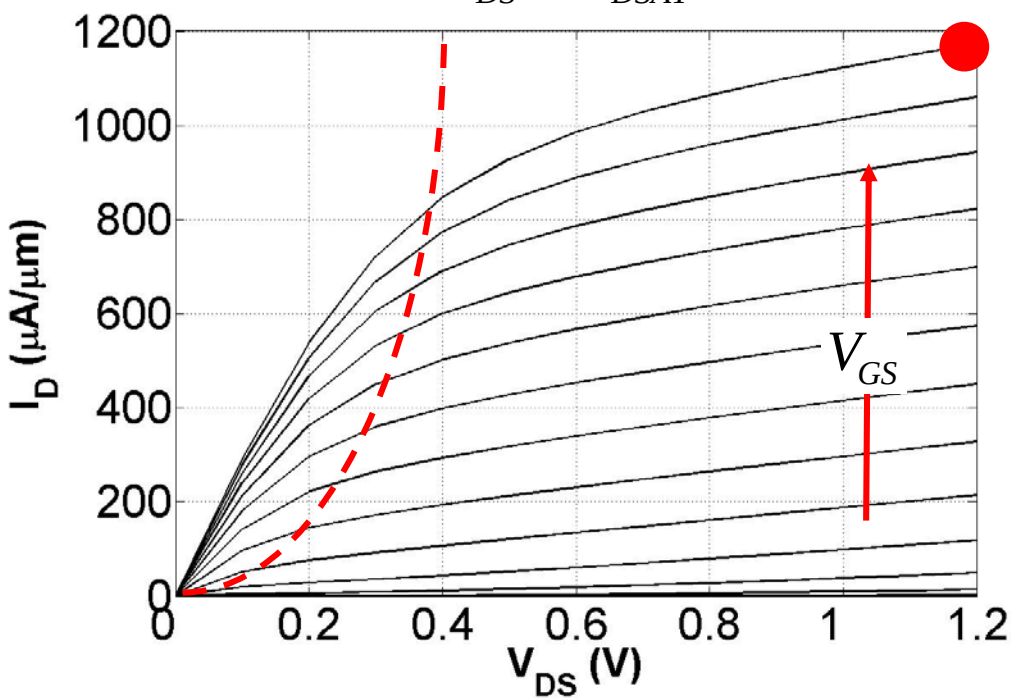
$V_{DS} << V_{DSAT}$

'linear region of operation'

'on-current'

$I_{DS}\left(V_{GS} = V_{DD}, V_{DS} = V_{DD}\right)$

$V_{DS} = V_{DSAT}$



I_{DSAT} : $\left(V_{GS} - V_T\right)^{\alpha}$

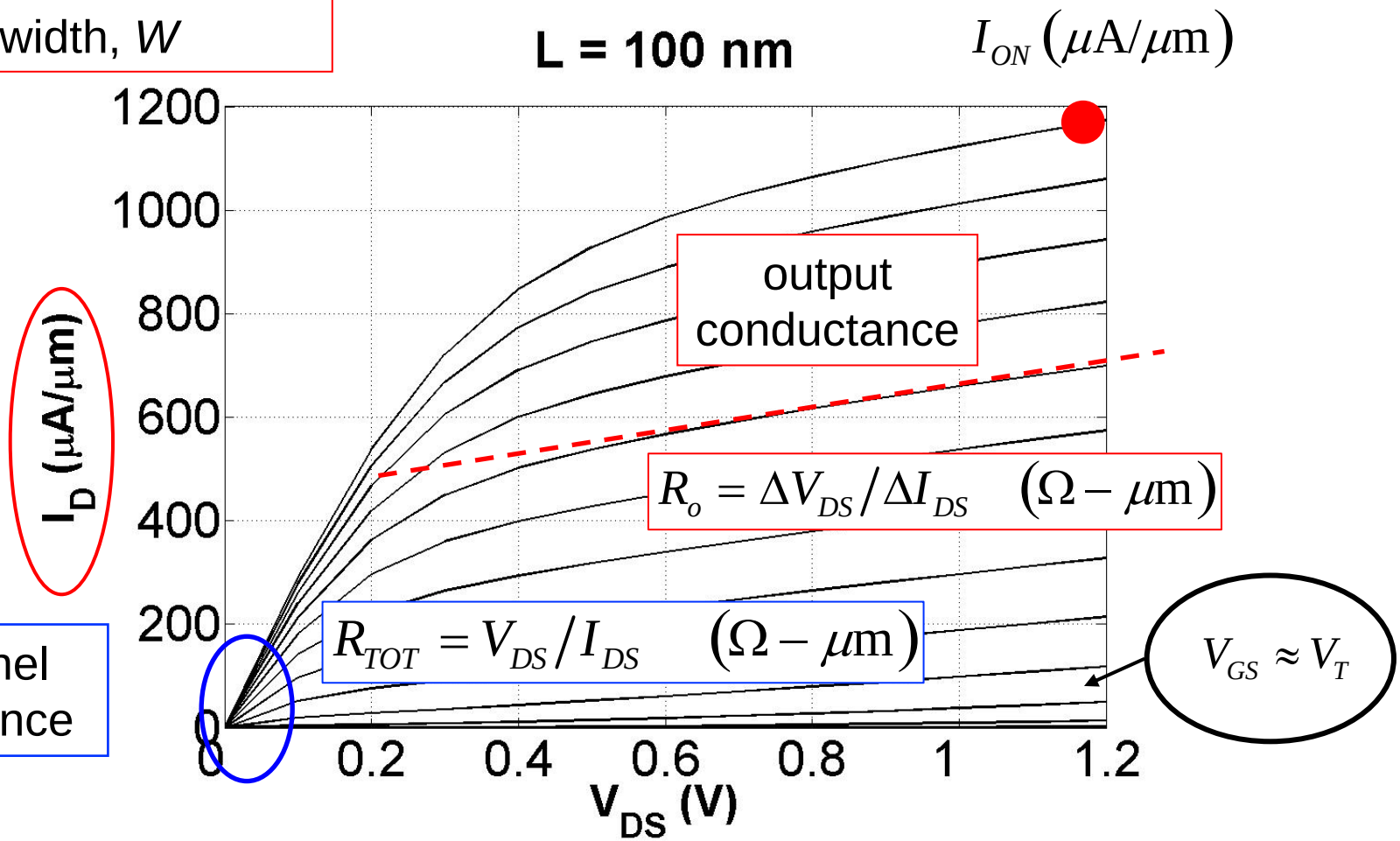
α = 2 ('square law')
α = 1 ('velocity saturated')

$V_{DS} >> V_{DSAT}$

'saturation region' ('beyond pinch-off')

common source characteristics

currents typically quoted per micrometer of MOSFET width, *W*



channel resistance

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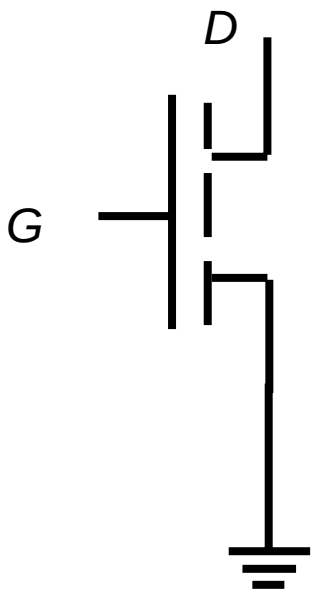
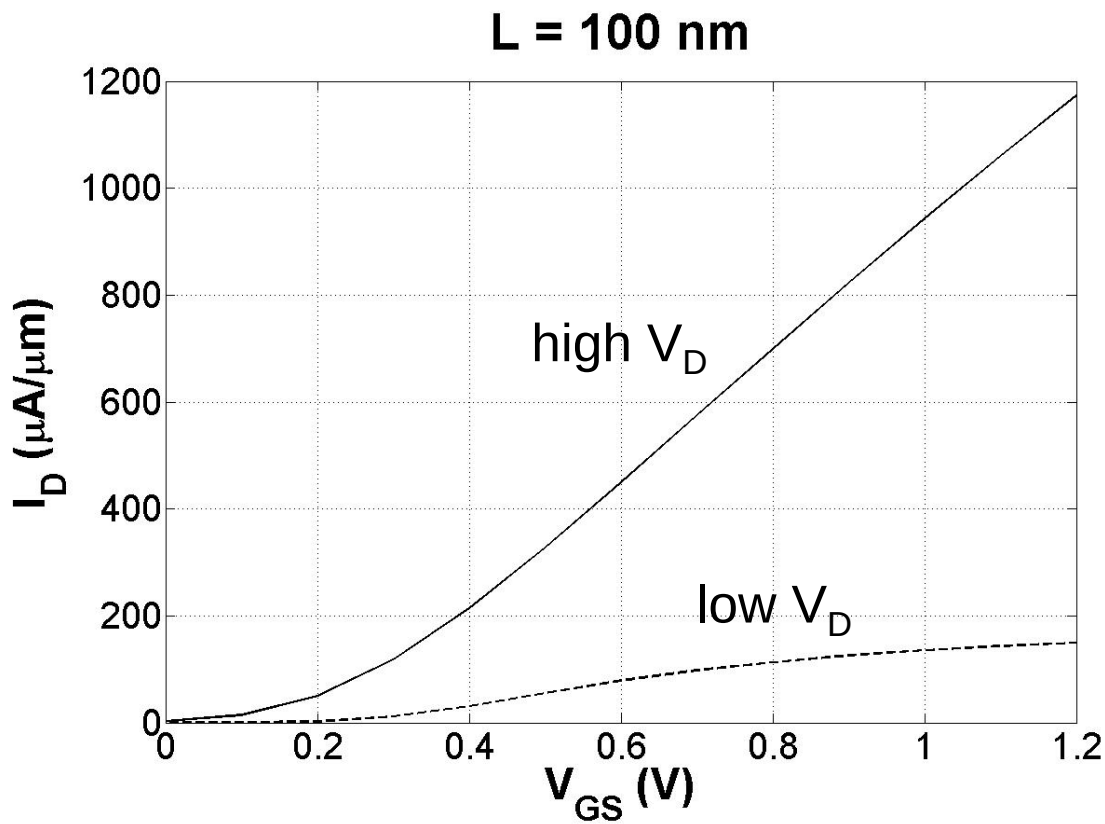
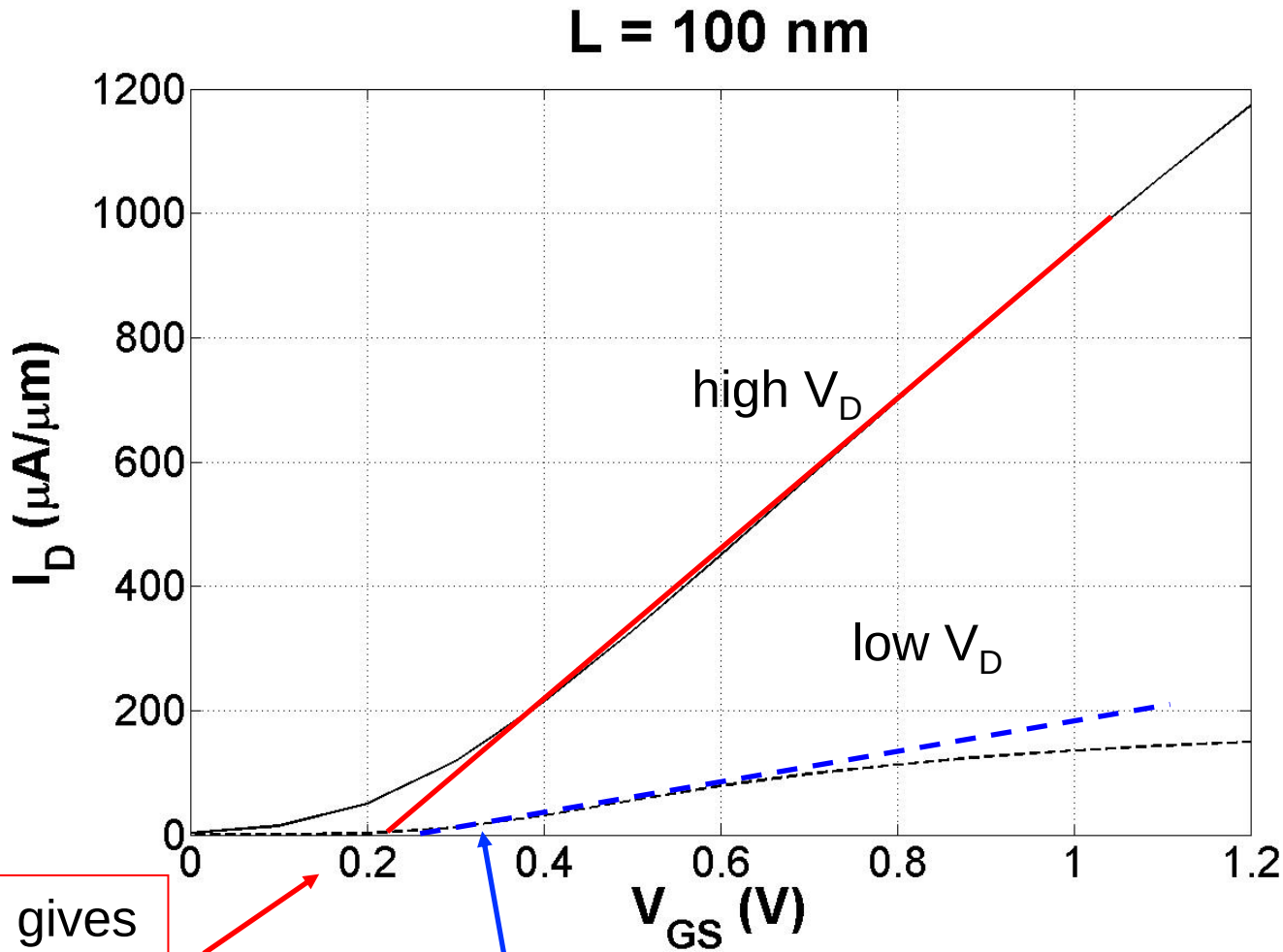
transfer characteristics





1) ground source
2) set V_D
3) sweep V_G from 0 to V_{DD}

measuring V_T



intercept gives
$V_T(sat) < V_T(lin)$

intercept gives $V_T(lin)$
slope is related to the effective mobility

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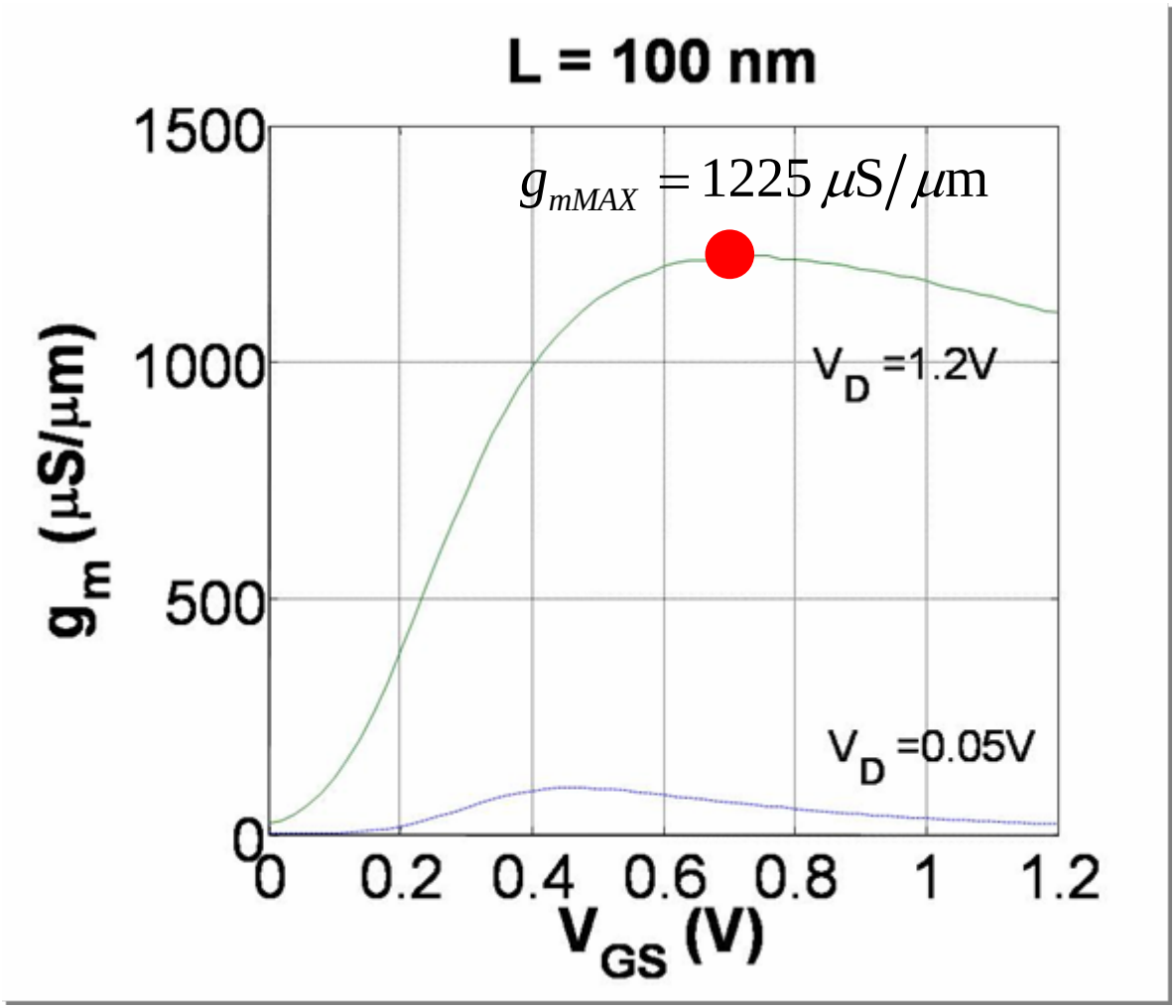
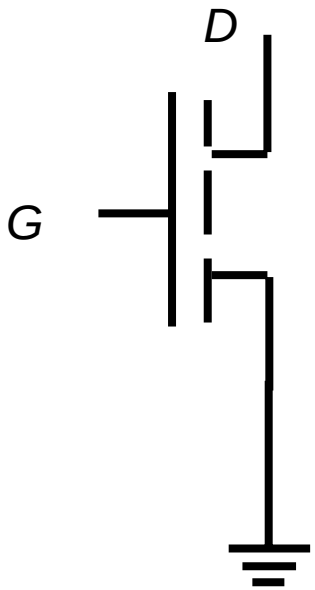
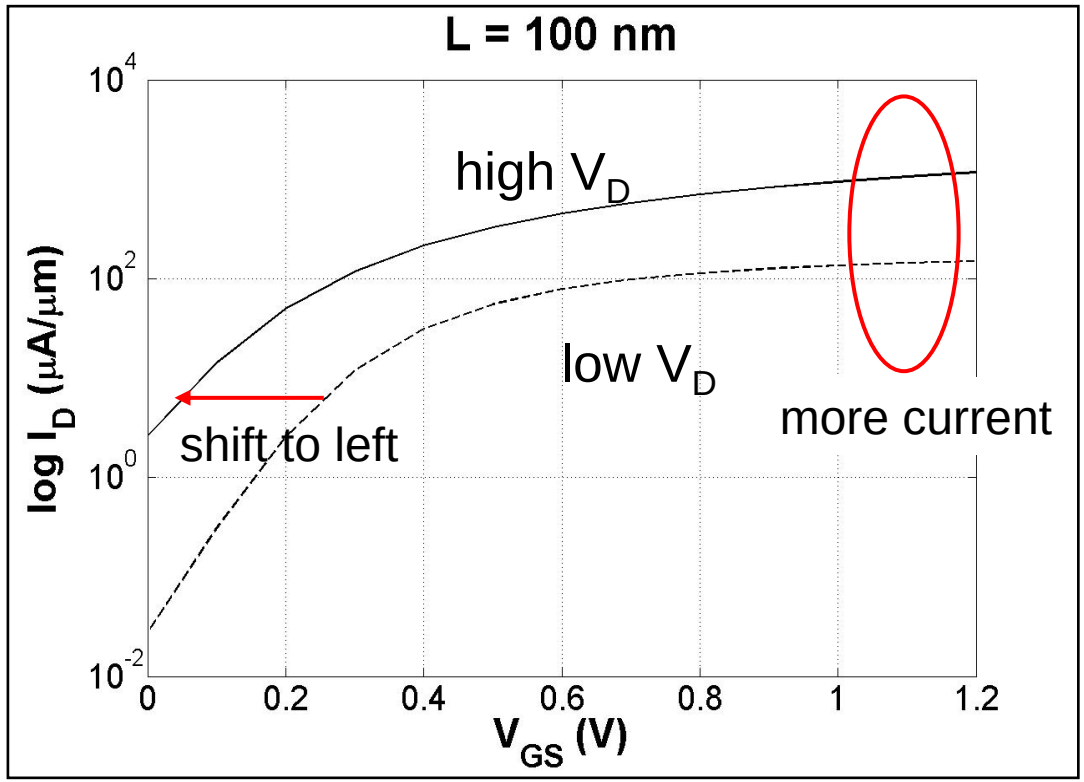
transconductance



$$g_m \equiv \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}}$$

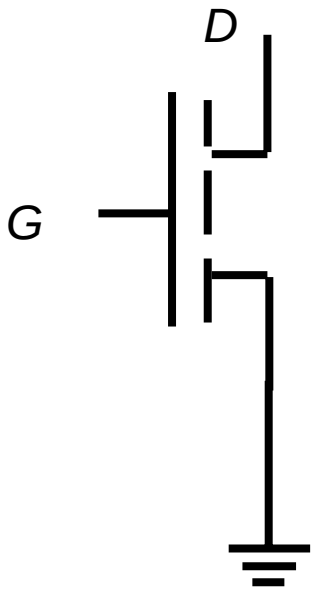
$\log_{10} I_D$ vs. V_{GS}

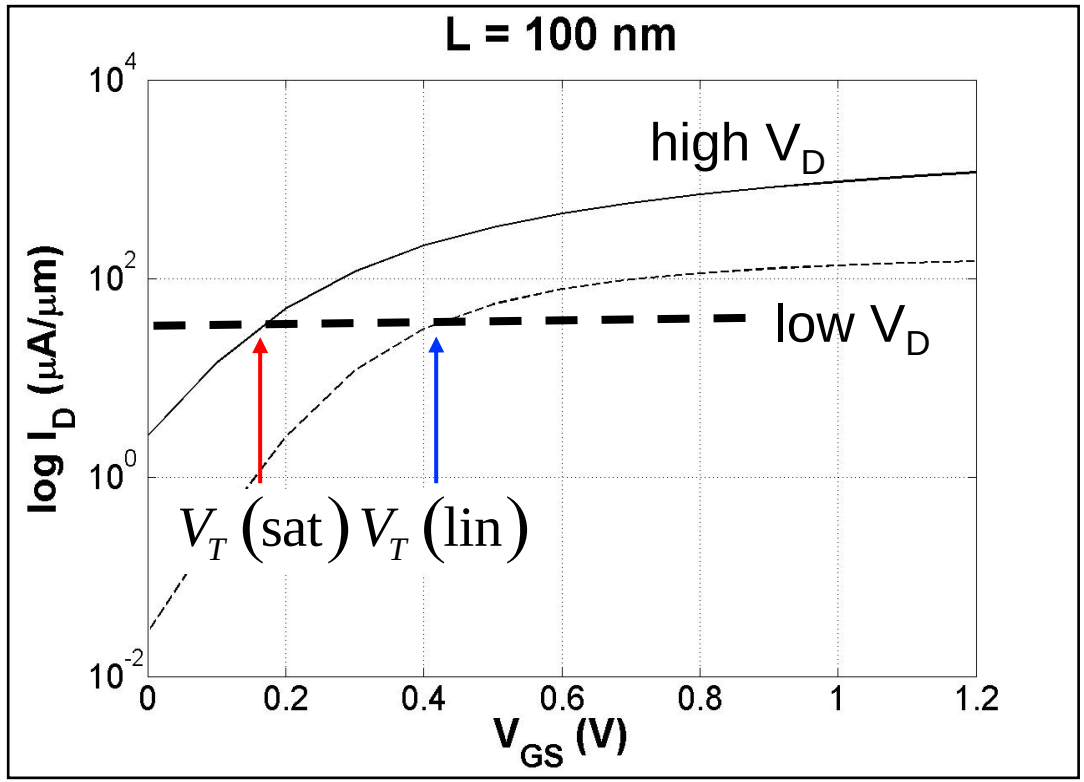




1) ground source
2) set $V_D = V_{DD}$
3) sweep V_G from 0 to V_{DD}

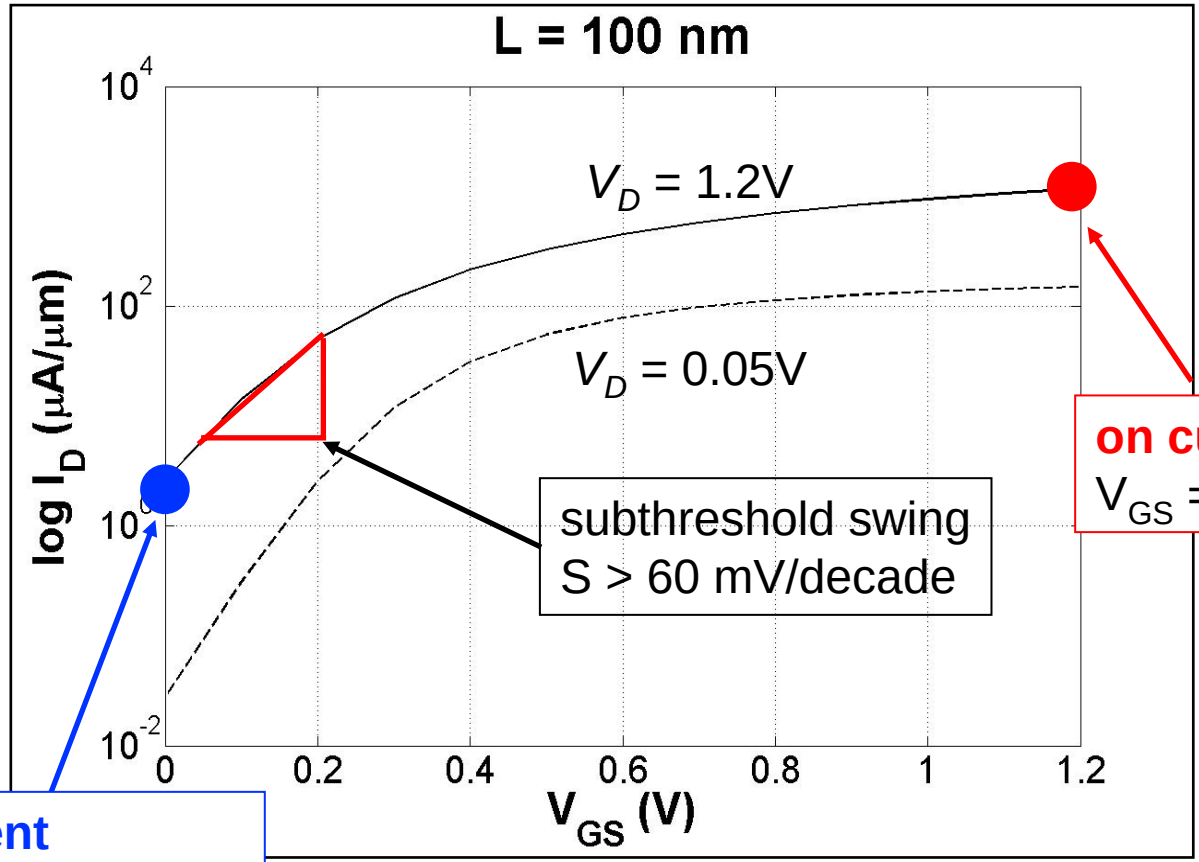
another way to 'measure' V_T





1) ground source
2) set $V_D = V_{DD}$
3) sweep V_G from 0 to V_{DD}

$\log_{10} I_D$ vs. V_{GS}



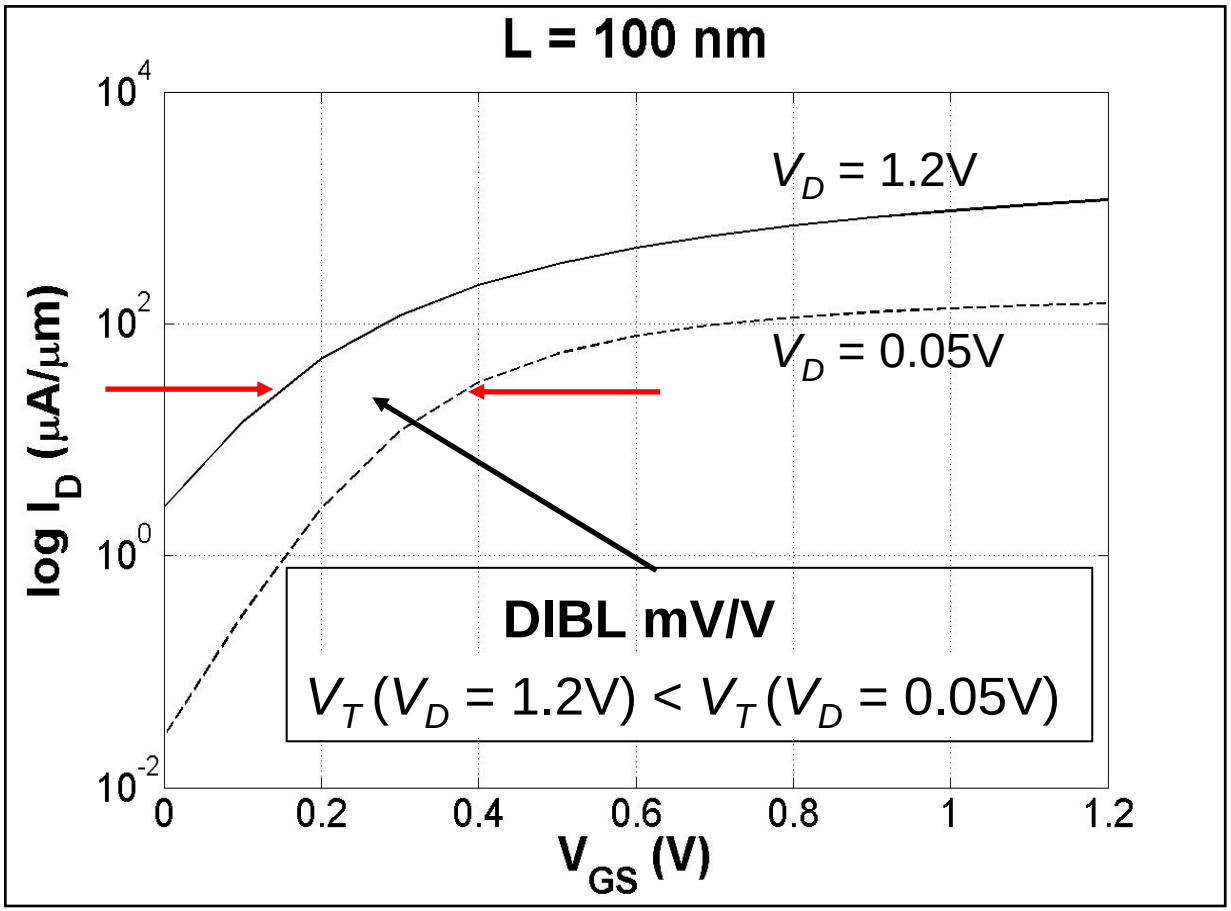
subthreshold swing
S > 60 mV/decade

on current
$V_{GS} = V_{DS} = V_{DD}$

off current
$V_{GS} = 0$ $V_{DS} = V_{DD}$

S is the number of millivolts required to increase V_G to produce a factor of 10 increase in I_D (in the sub-threshold region).

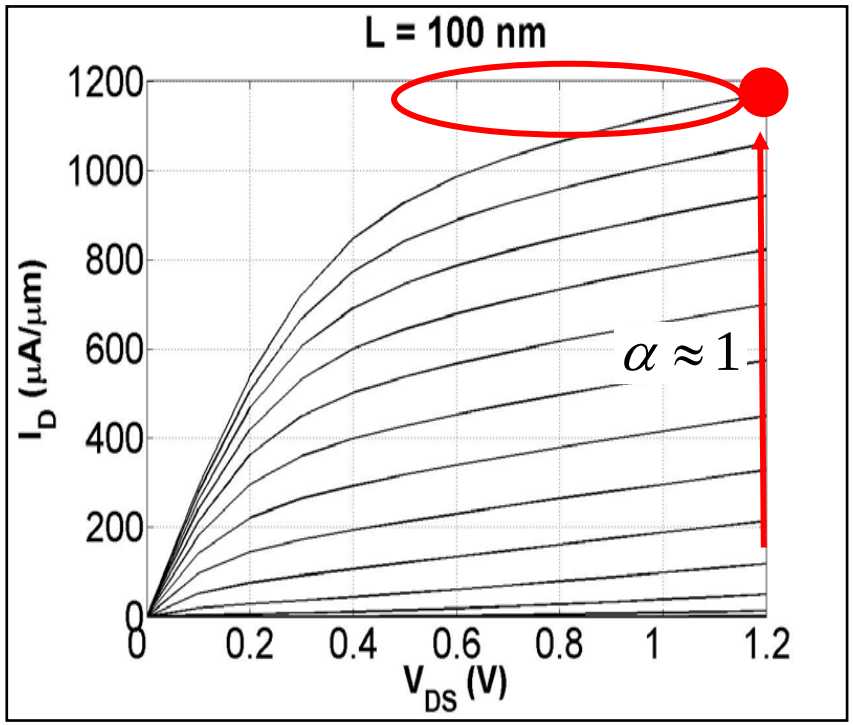
DIBL (drain-induced barrier lowering)



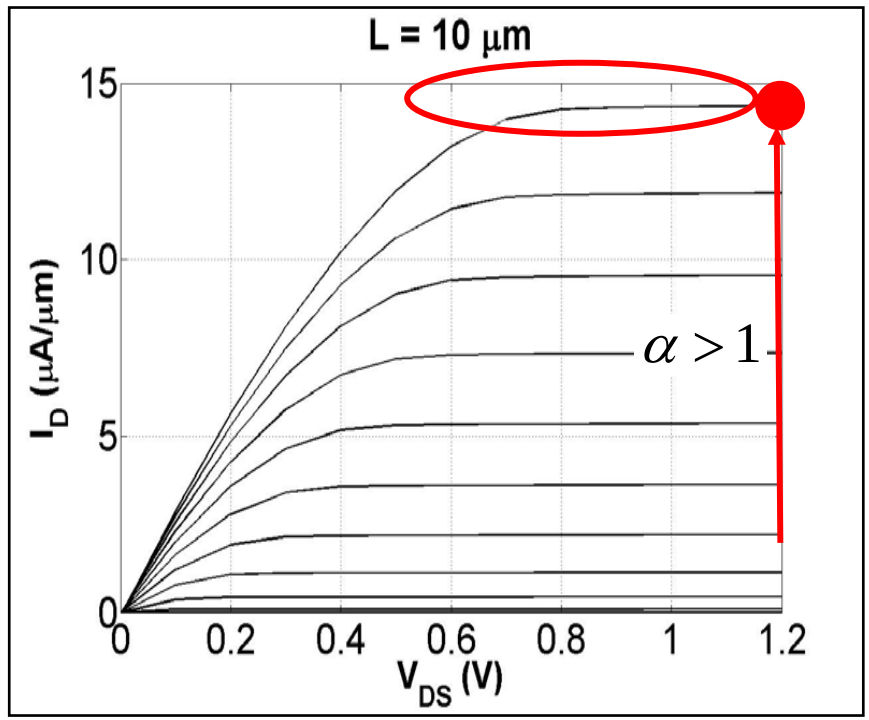
DIBL is the horizontal shift in the subthreshold characteristic (in millivolts) divided by the change in V_D (in volts).

long channel vs. short channel

L = 100nm



L = 10 μm (10,000 nm)



$$I_{DSAT} : (V_{GS} - V_T)^{\alpha}$$

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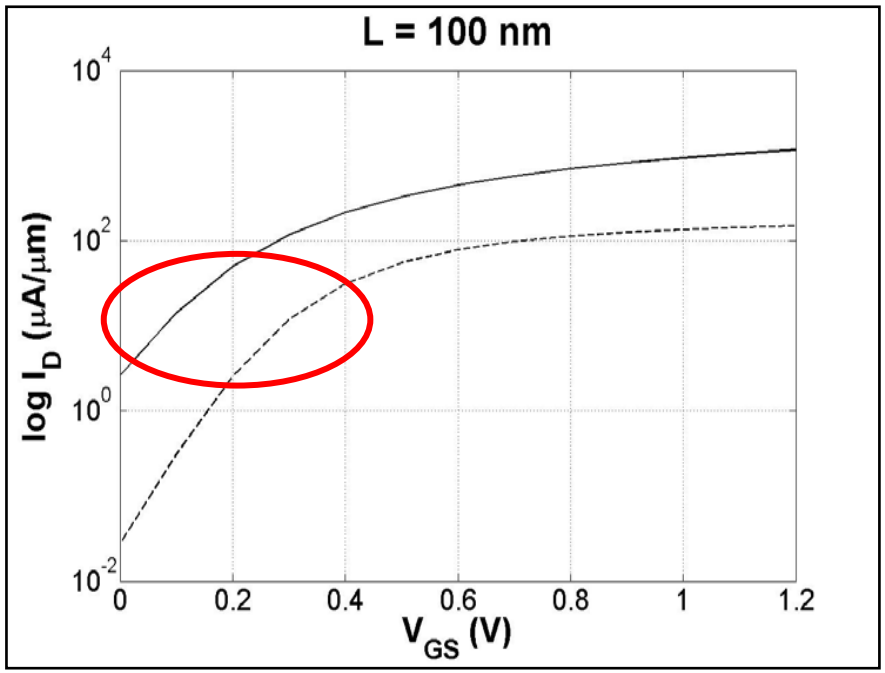
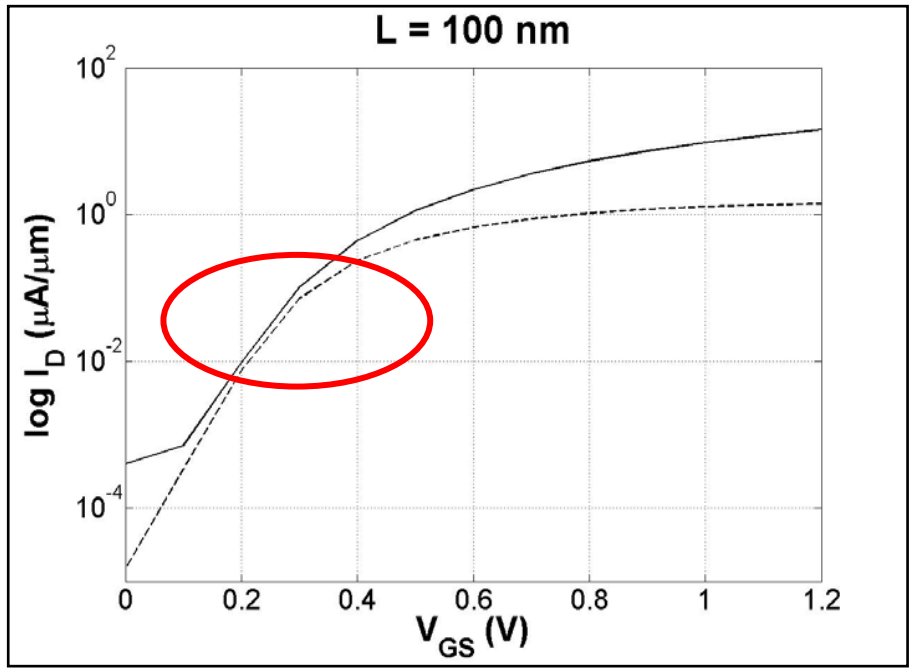
long channel vs. short channel

L = 100nm



L = 10 μm (10000 nm)



device performance metrics summary

You should now be familiar with the following terms:

1) On-current
2) Off-current
3) Channel resistance
4) Output resistance
5) Threshold voltage
6) Drain saturation voltage
7) Subthreshold swing *S* (mV/dec)
8) Drain Induced Barrier Lowering DIBL (mV/V)

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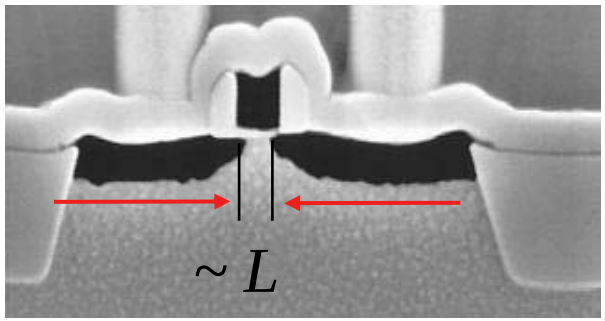
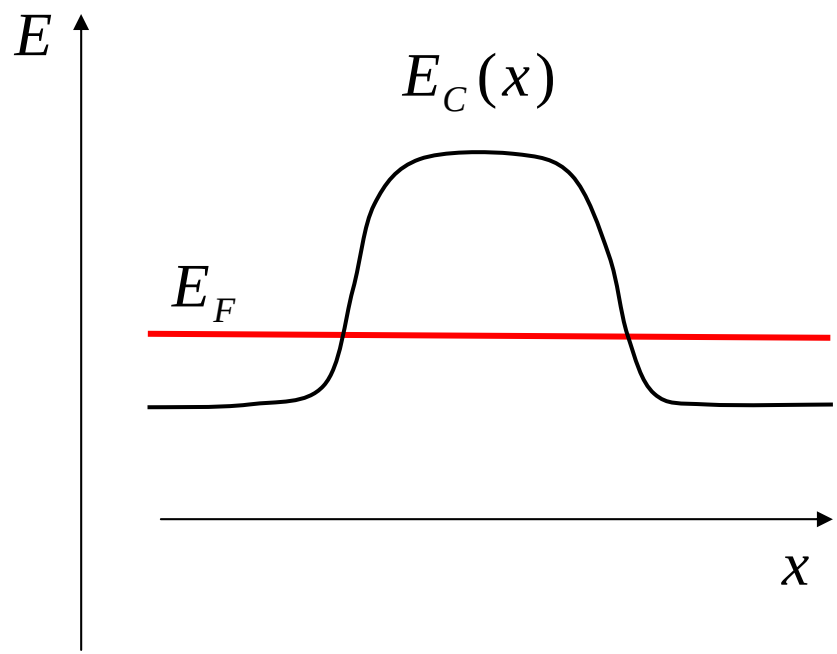
energy vs. position

source gate drain

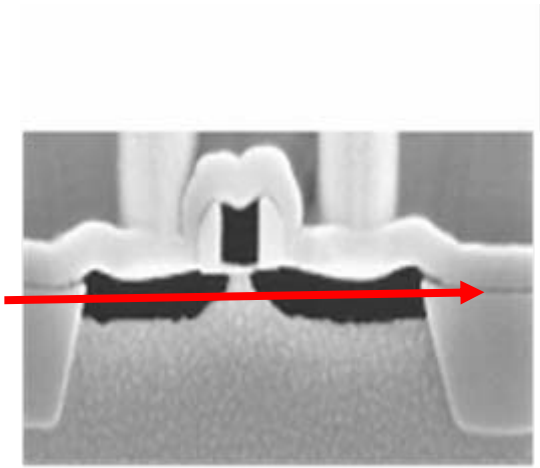


physical structure



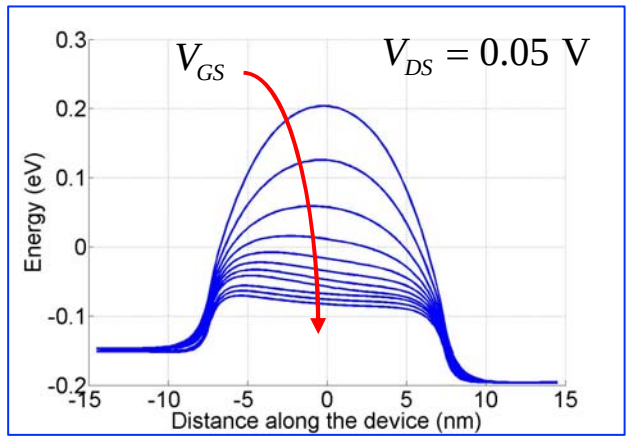
equilibrium E-band diagram

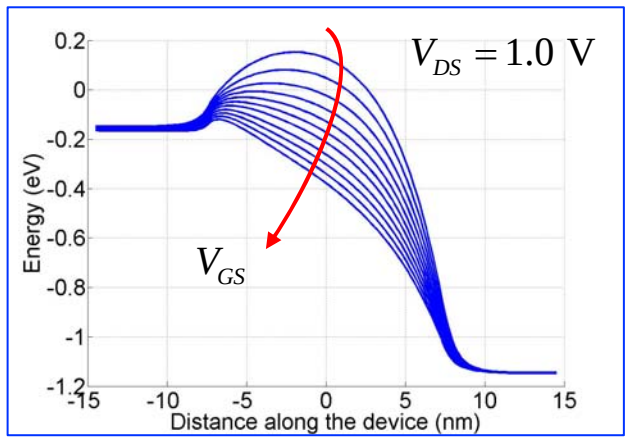
controlling current with energy barriers



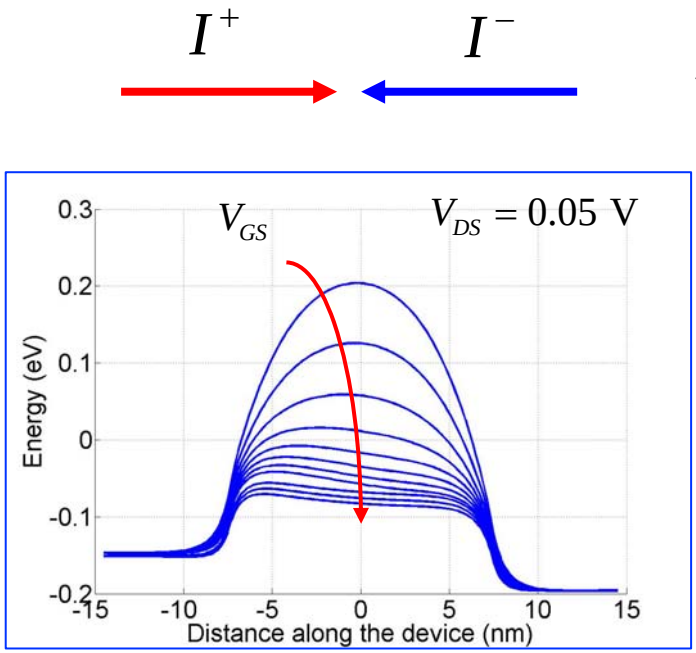
$$E = -qV$$

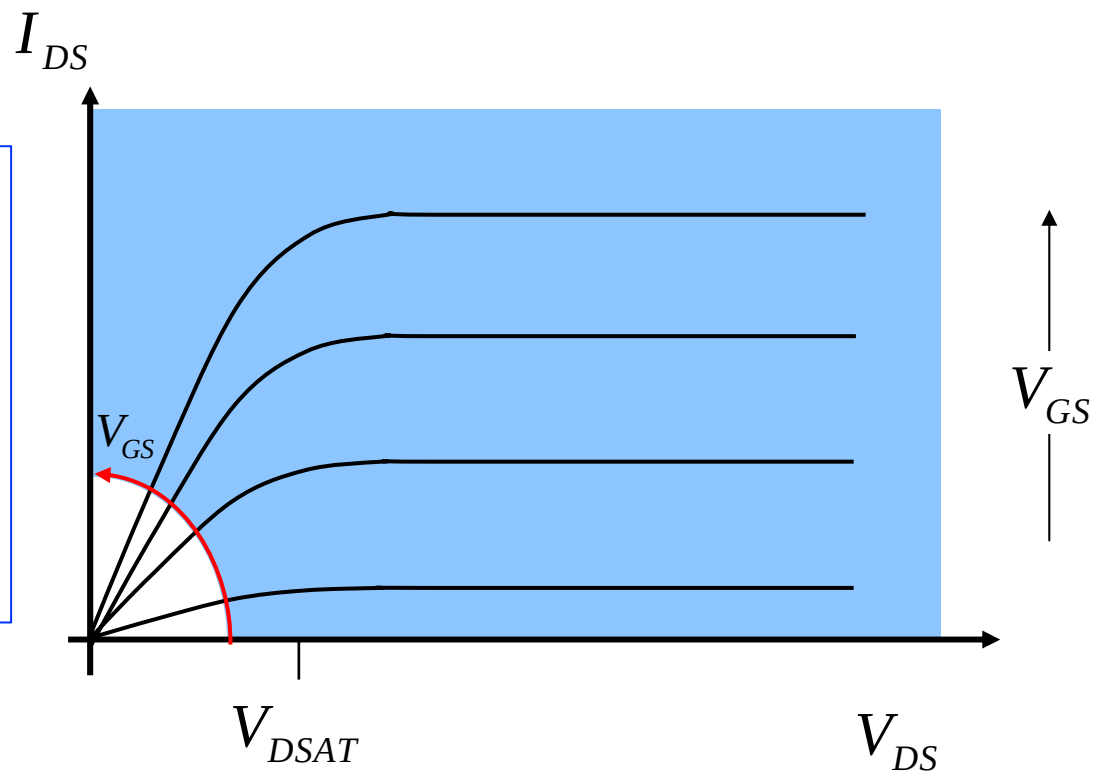
electron energy vs. position





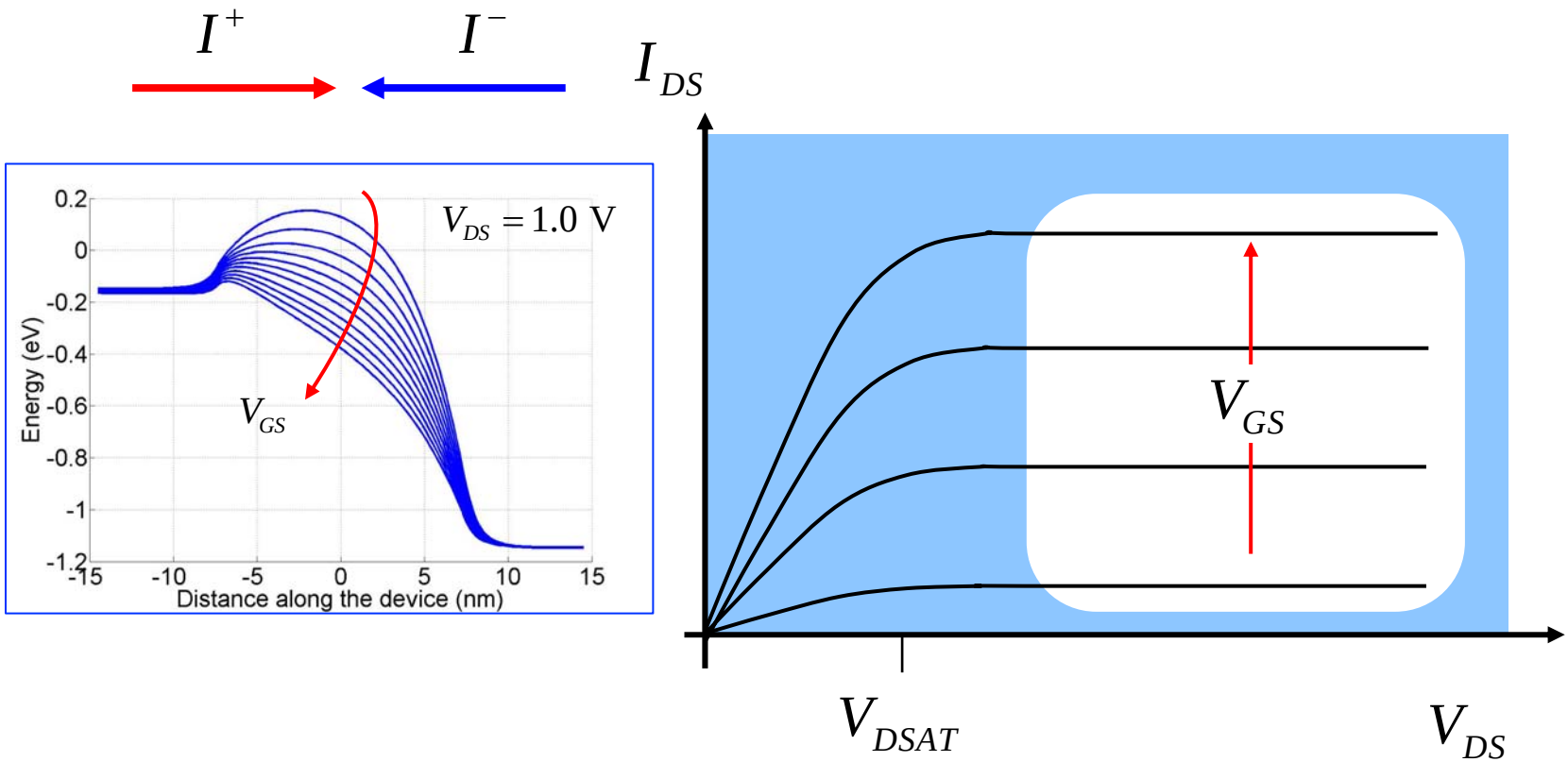
low V_{DS}





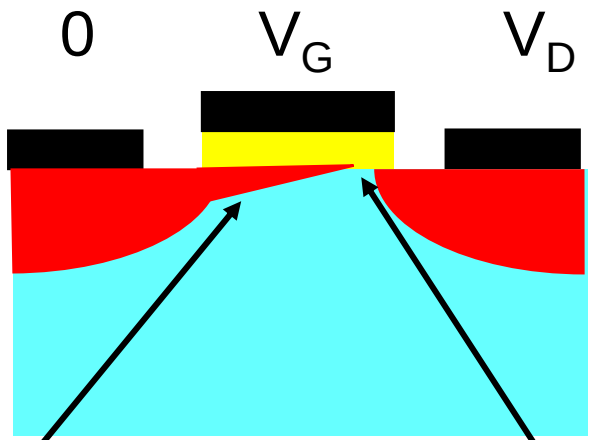
$$I^+ - I^- \propto V_{DS}$$

high V_{DS}



$$I_{DS} \propto I^+$$

MOSFET IV: pinch-off at high V_{DS}



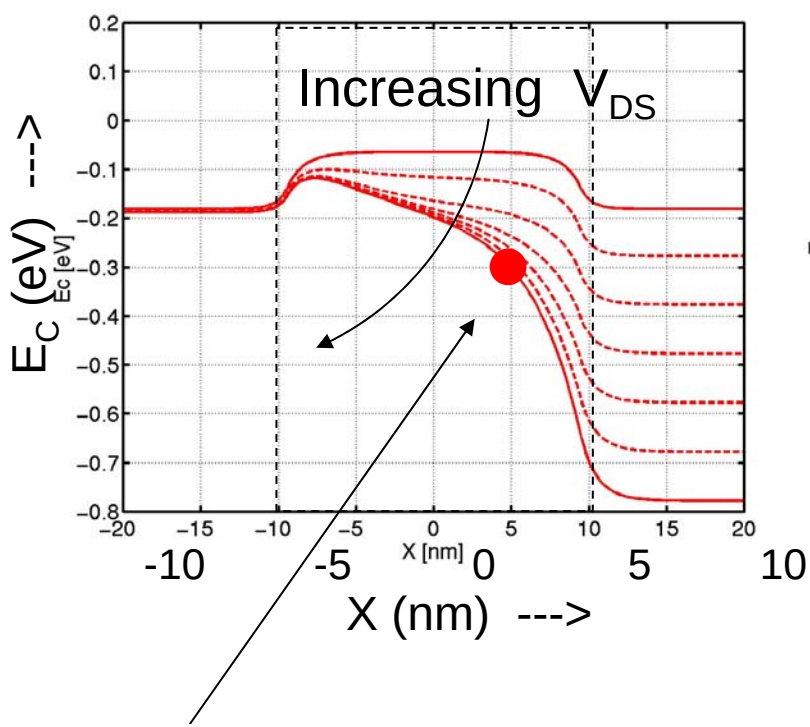
$$Q_i(x) = -C_{ox}\left(V_{GS} - V_T - V(x)\right)$$

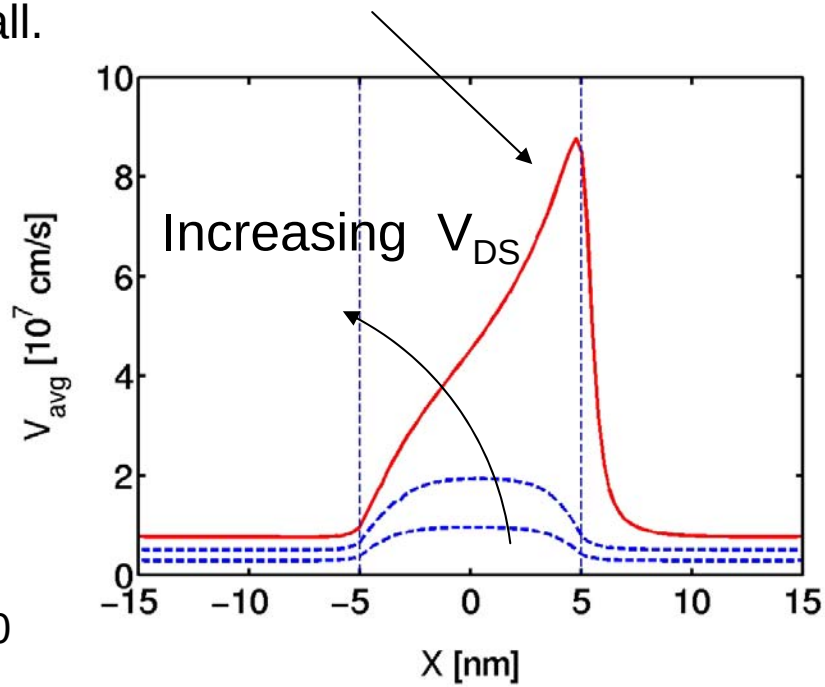
$$V(x) = \left(V_{GS} - V_T\right)$$

$$Q_i(x) \approx 0$$

pinch off in a MOSFET

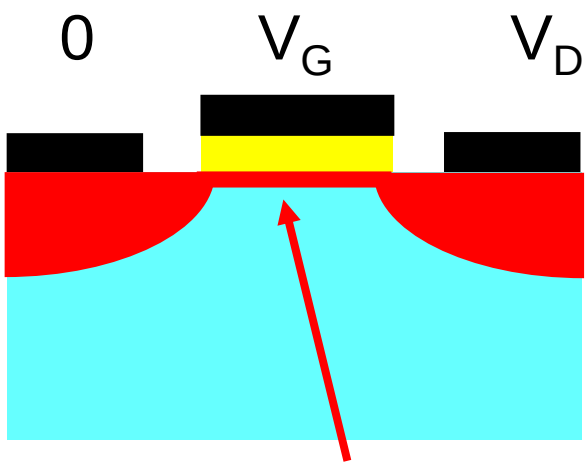
The electron velocity is very high in the pinch-off region. High velocity implies low inversion layer density (because I_D is constant). In the textbook model, we say $Q_i \approx 0$, but it is not really zero - just very small.



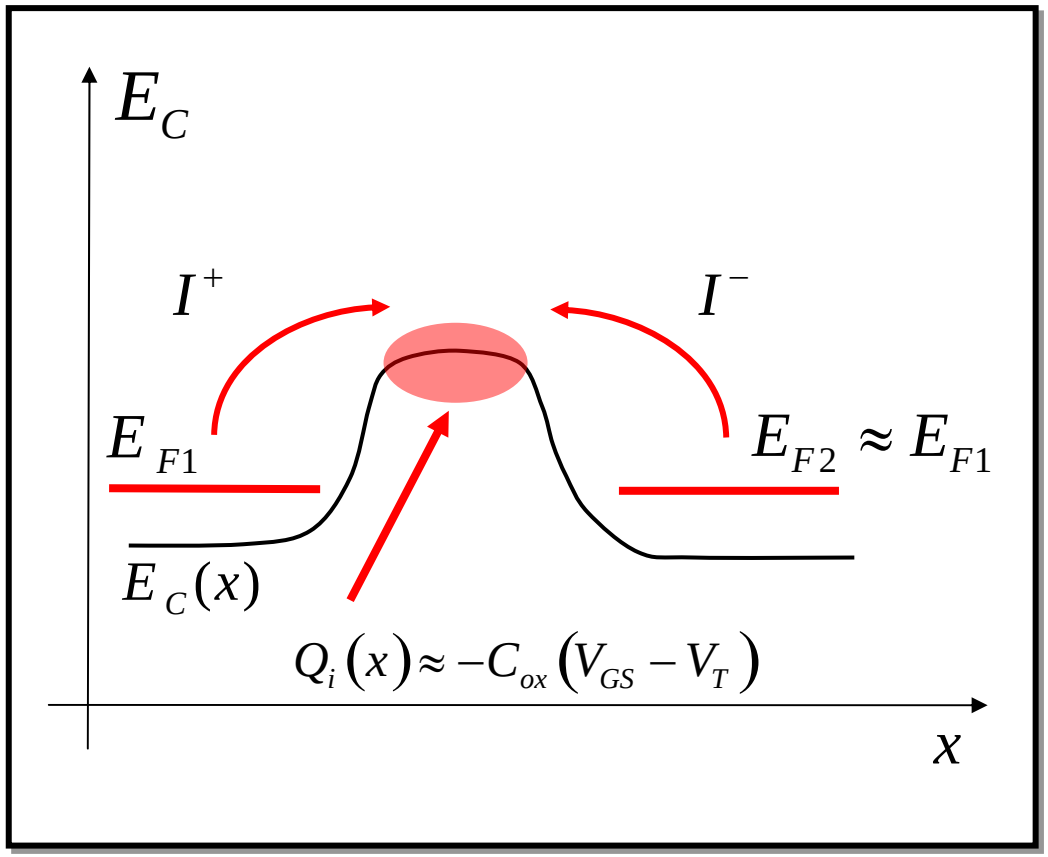


pinch-off point: where the electric field along the channel becomes very large. Note that electrons are simply swept across the high-field (pinched-off) portion at very high velocity.

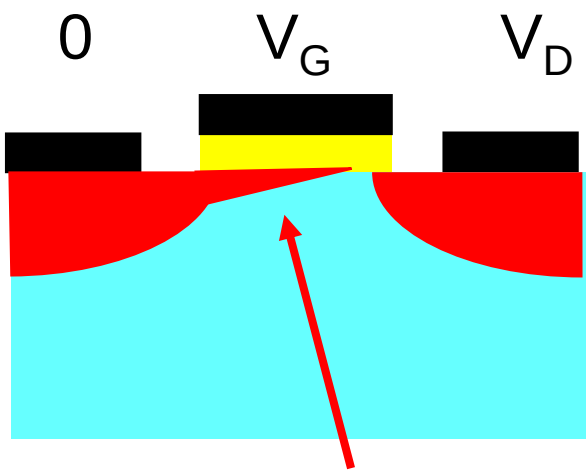
barrier-controlled vs. charge controlled view



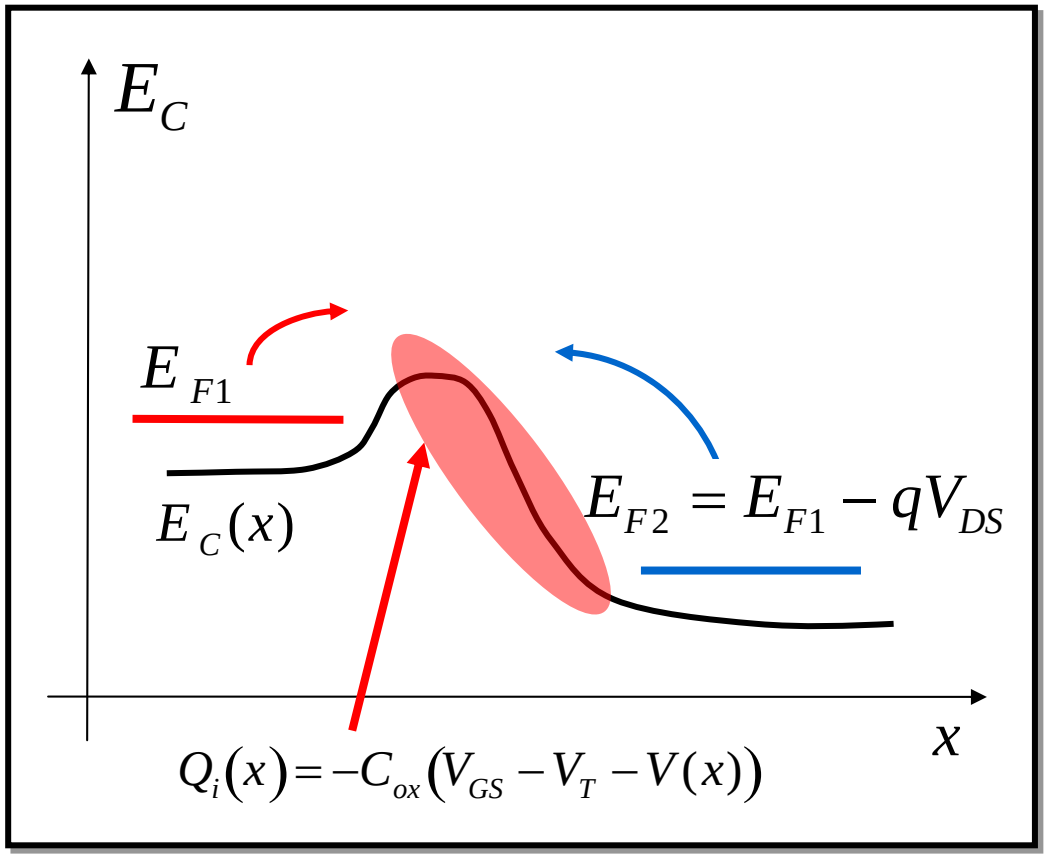
$$Q_i(x) = -C_{ox}(V_{GS} - V_T - V(x))$$



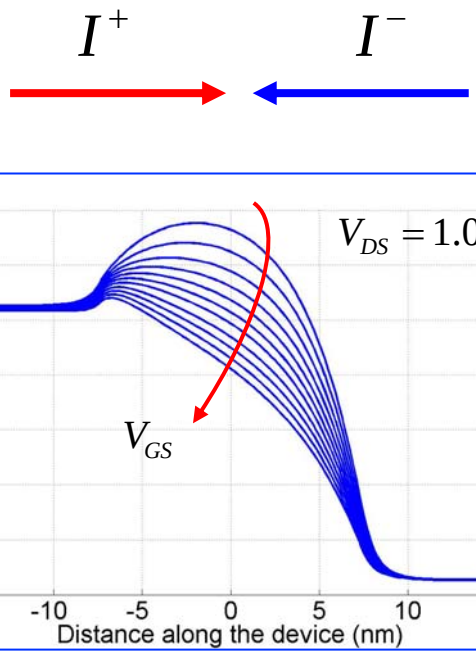
barrier-controlled vs. charge controlled view



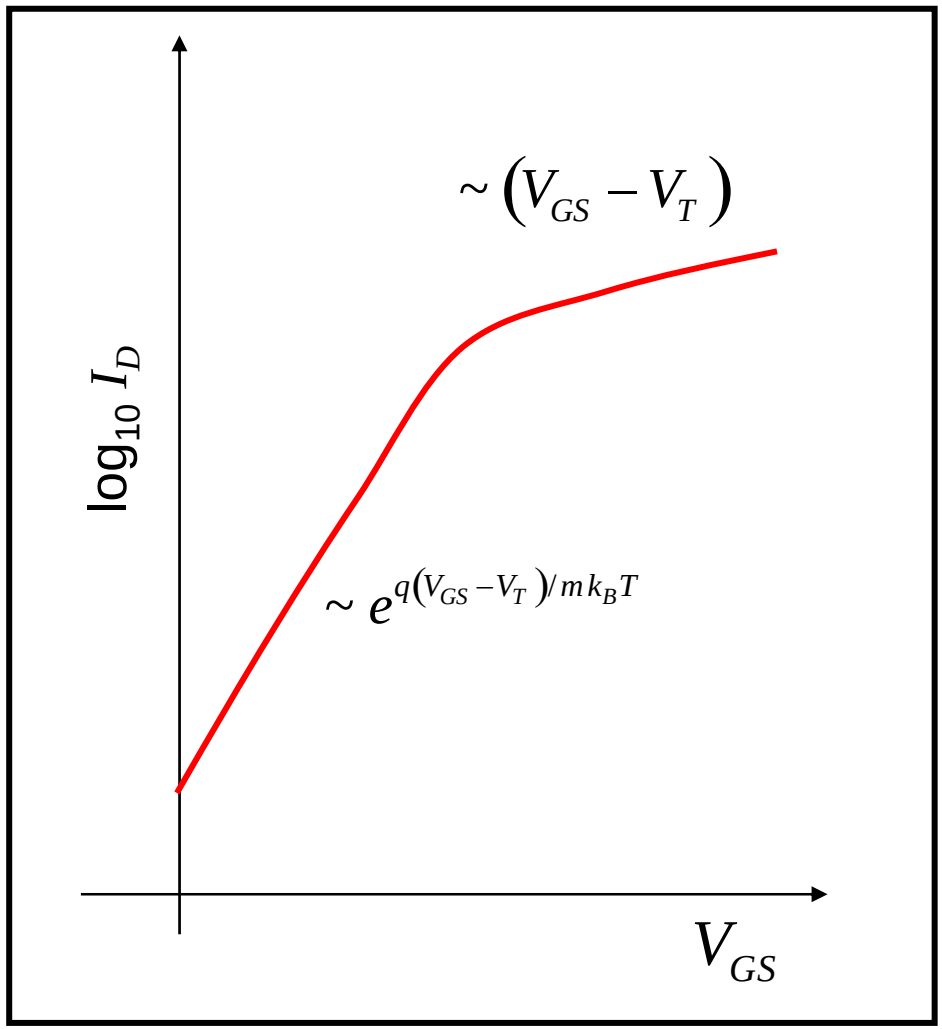
$$Q_i(x) = -C_{ox}(V_{GS} - V_T - V(x))$$



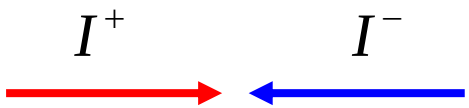
IV characteristic for high V_{DS}

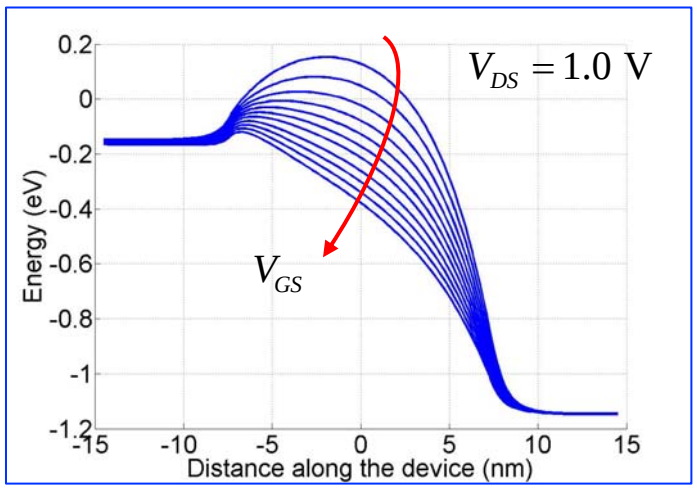


$$I_D \approx I^+$$



IV characteristic for high V_{DS} (below threshold)





$$I_D \approx I^+$$

$$I_D \approx I^+ \sim e^{-\Delta E/k_B T}$$

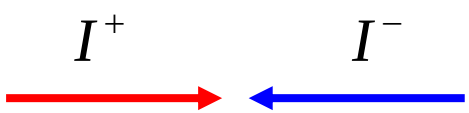
$$\Delta E = \Delta E_{FB} - q\psi_S$$

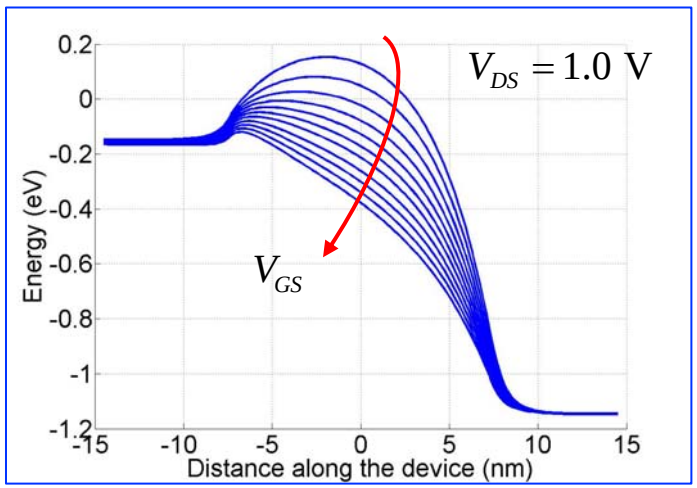
$$I_D \sim e^{q\psi_S/k_B T}$$

$$\psi_S = V_{GS}/m$$

$$I_D \sim e^{qV_{GS}/mk_B T}$$

IV characteristic for high V_{DS} (above threshold)





$$I_D \propto I^+$$

E.O. Johnson, *RCA Review*, 1971

$$I_D \approx I^+ \sim e^{-\Delta E/k_B T}$$

$$\Delta E = \Delta E_{FB} - q\psi_S$$

$$I_D \sim e^{q\psi_S/k_B T}$$

$$|Q_I| \sim e^{q\psi_S/k_B T}$$

$$|Q_I| = C_{ox}(V_{GS} - V_T)$$

$$\psi_S \sim \ln(V_{GS} - V_T)$$

$$I_D \sim (V_{GS} - V_T)$$

outline

1) Introduction
2) MOSFET theory
3) Device performance metrics
4) The barrier model of a MOSFET
5) **Carrier transport in MOSFETs**
6) Summary

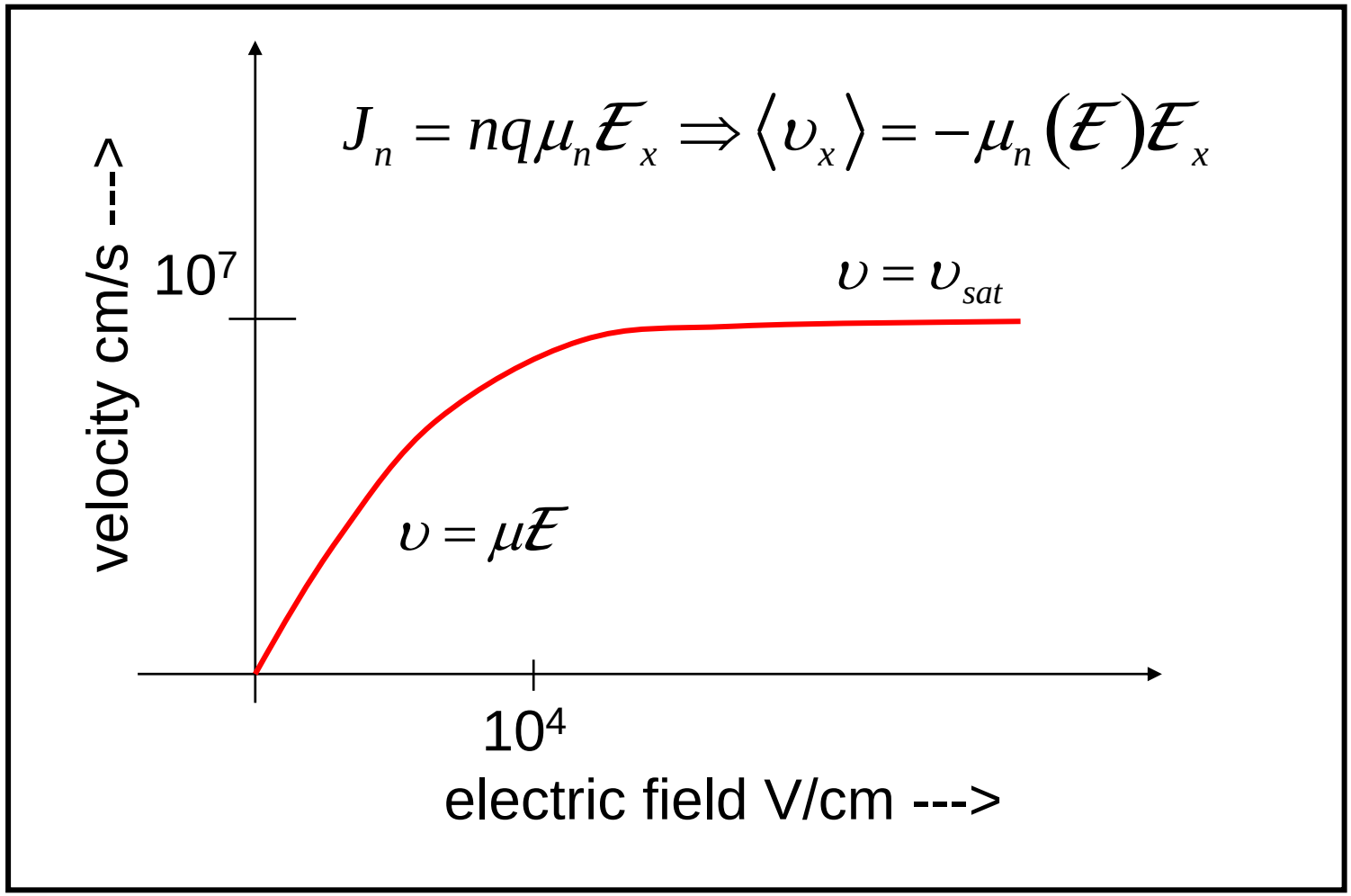
drift-diffusion transport

$$J_n = nq\mu_n \mathcal{E}_x + qD_n \frac{dn}{dx}$$

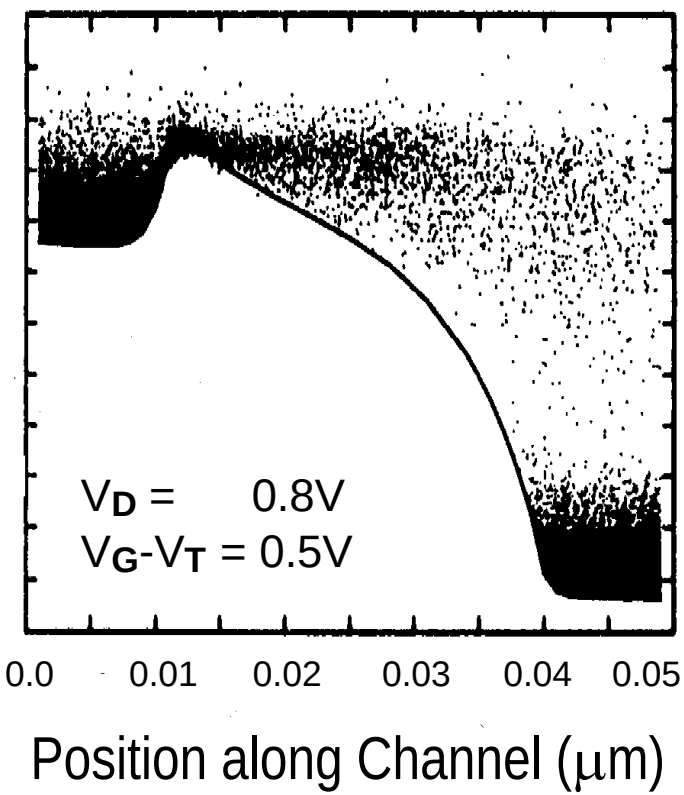
above threshold, drift dominates

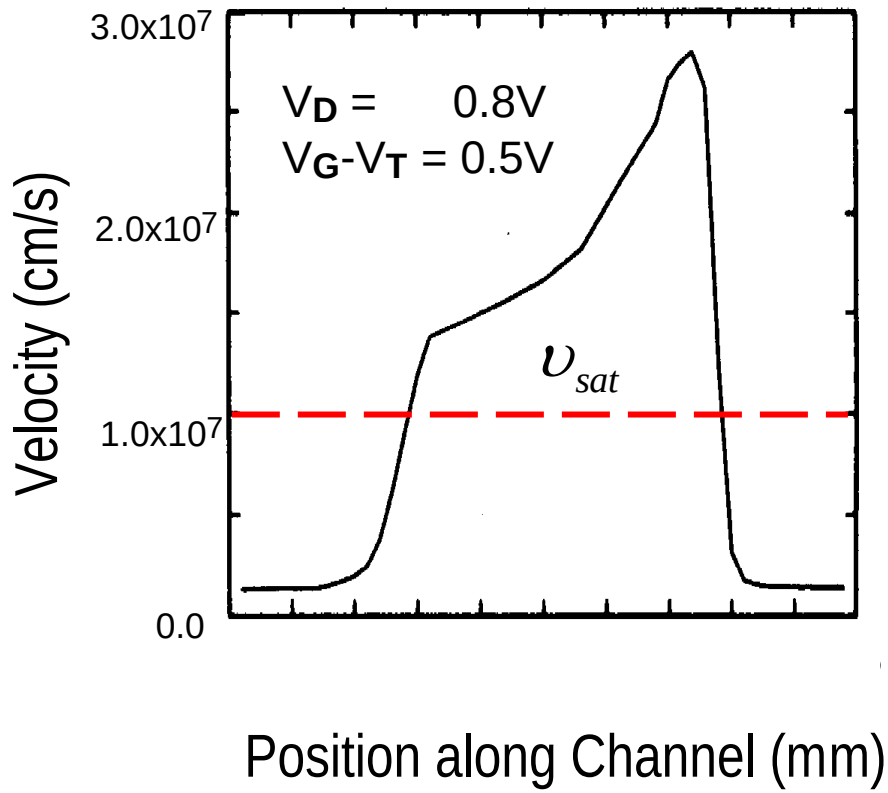
below threshold, diffusion dominates

velocity saturation



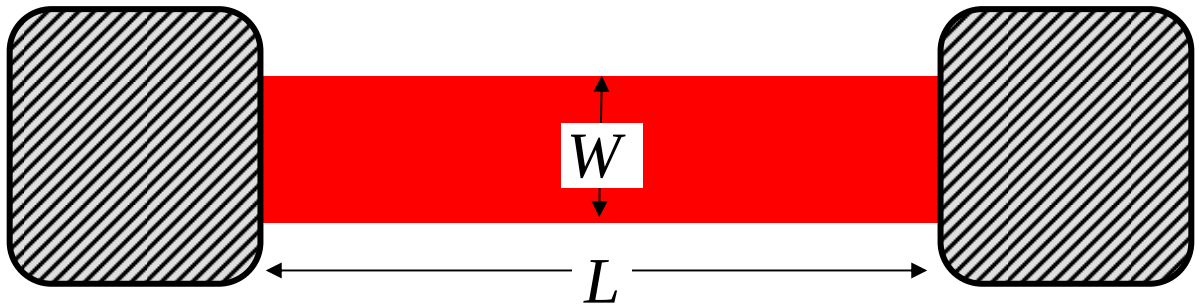
velocity overshoot in sub-micron MOSFETs





Frank, Laux, and Fischetti, IEDM Tech. Dig., p. 553, 1992

diffusive vs. ballistic transport



1) diffusive:

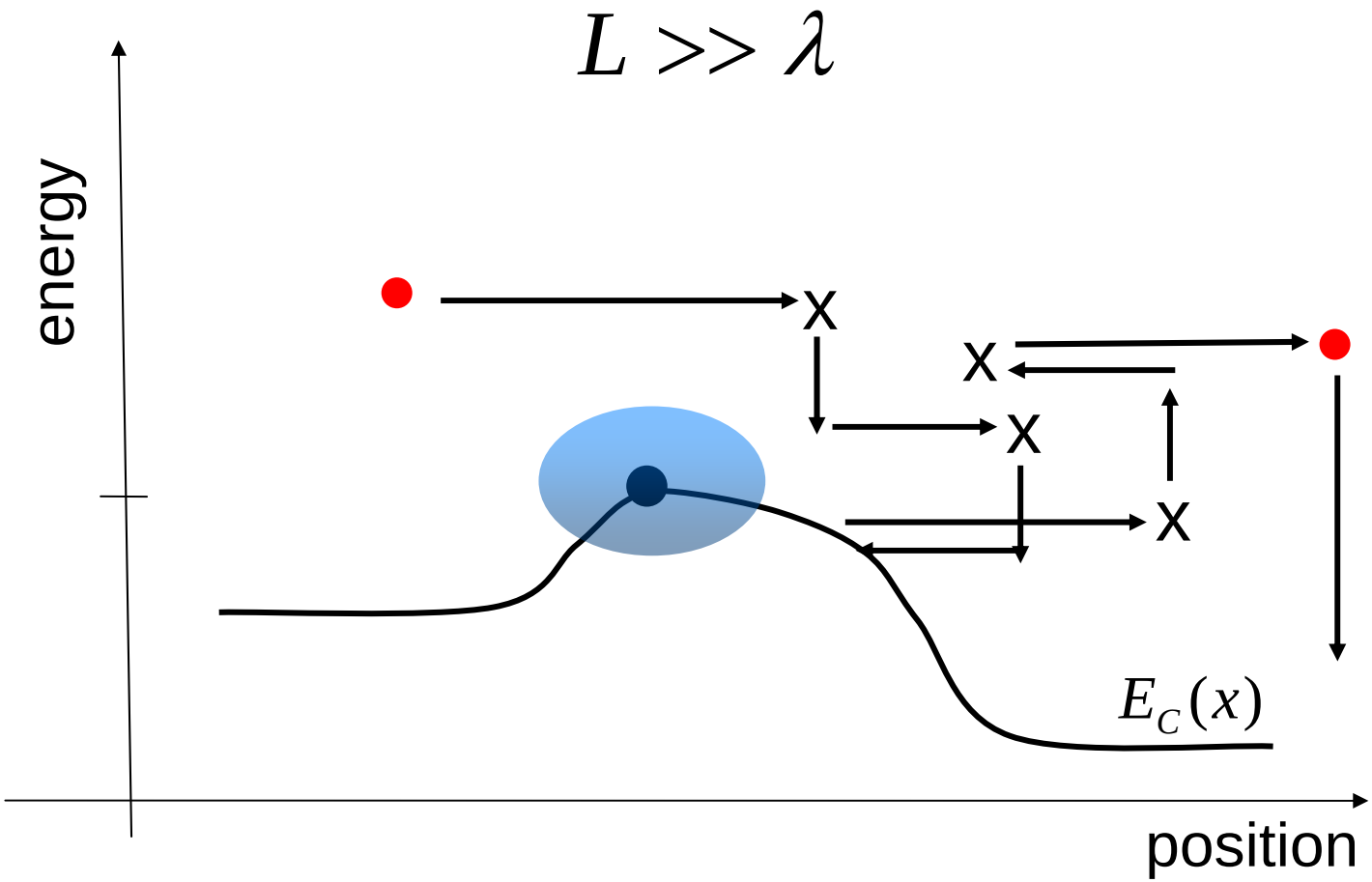
$$R = \rho_S \left(L/W \right) \quad \rho_S = 1/n_S q \mu_n \quad \langle \upsilon_x \rangle = -\mu_n \mathcal{E}_x = \mu_n \left(V/L \right)$$

2) ballistic:

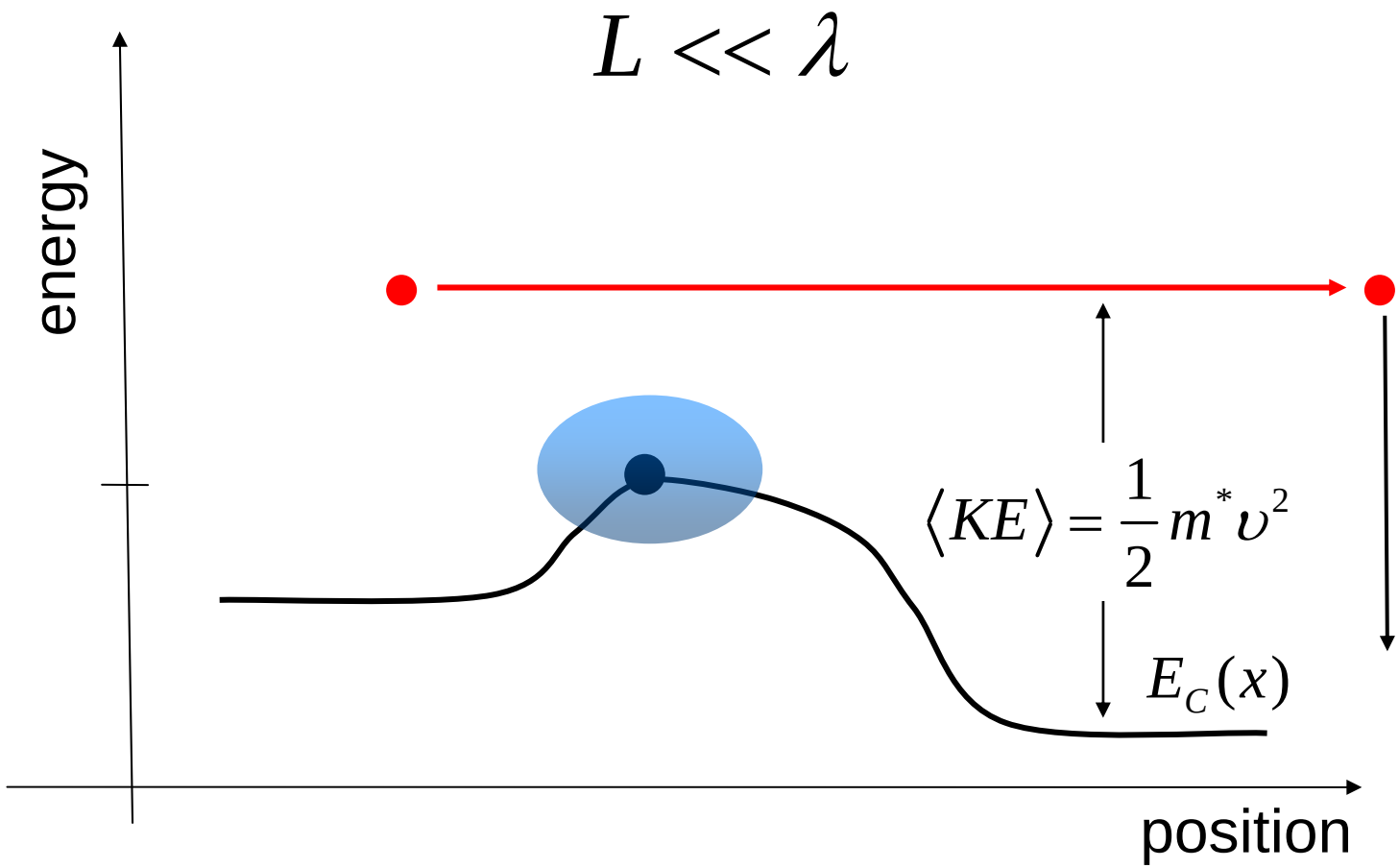
$$R = \left(M\, 2q^2/h \right)^{-1}$$

("quantum contact resistance" T = 0 K)

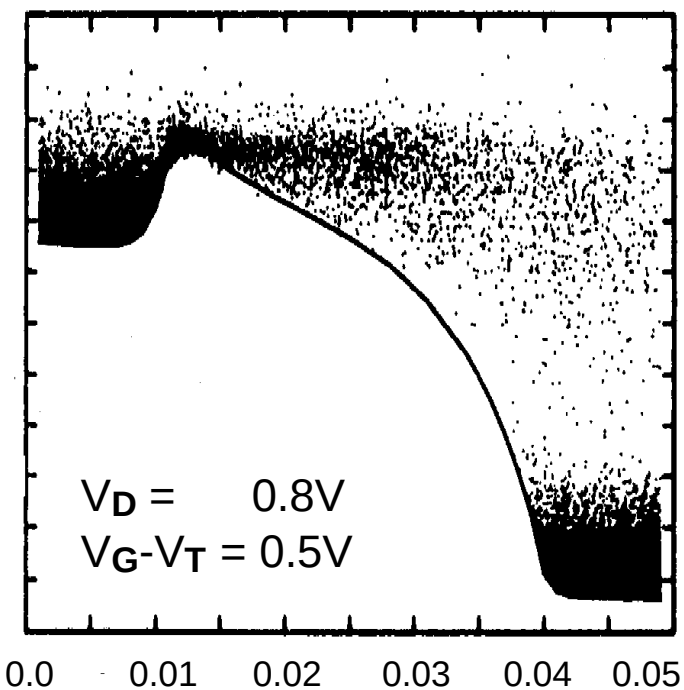
diffusive transport in a MOSFET



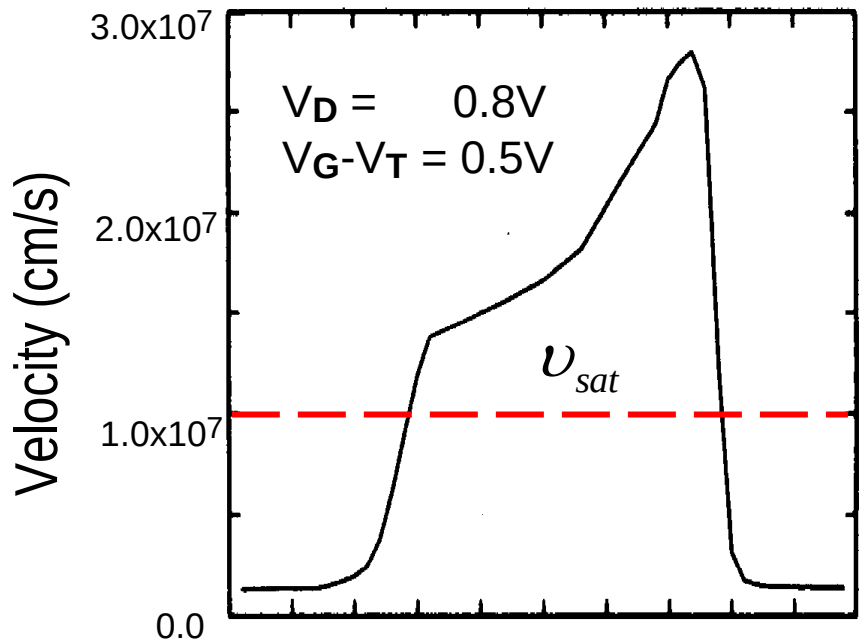
ballistic transport in a MOSFET



velocity overshoot in sub-micron MOSFETs



Position along Channel (μm)

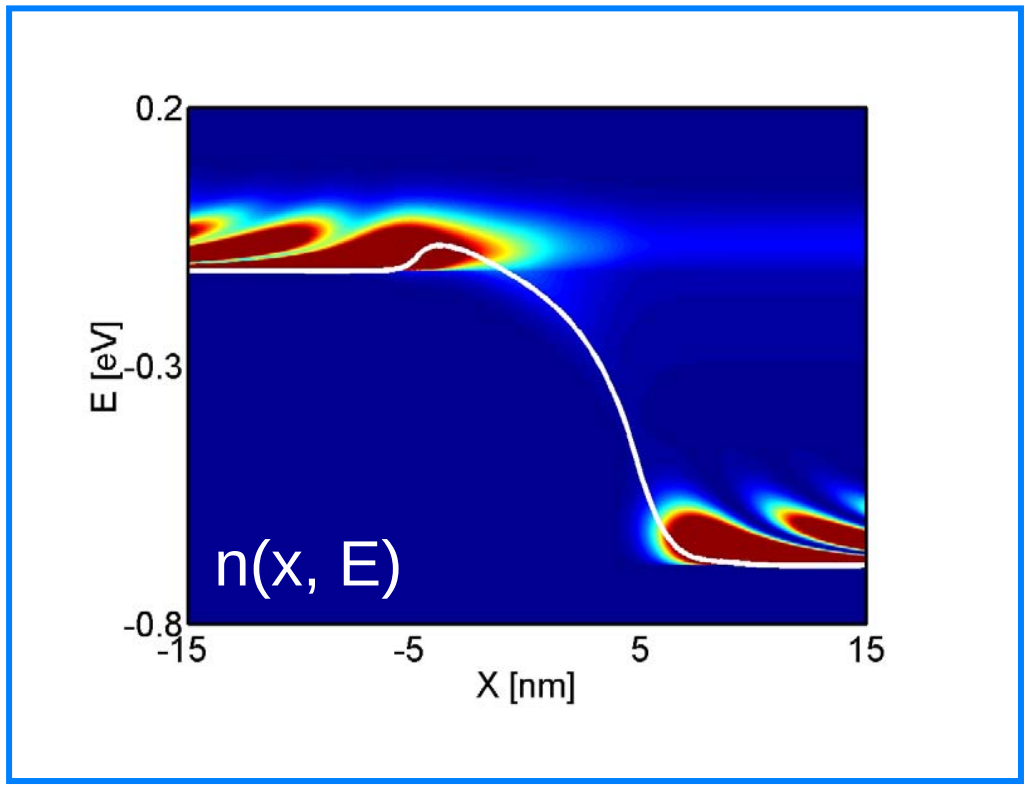


Position along Channel (mm)

Frank, Laux, and Fischetti, IEDM Tech. Dig., p. 553, 1992

quantum transport in a nano MOSFET

L = 10 nm



nanoMOS (www.nanoHUB.org)

outline

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summary

1) Traditional MOSFET theory is based on drift-diffusion and MOS electrostatics.

2) MOSFETs are ‘barrier controlled devices.’

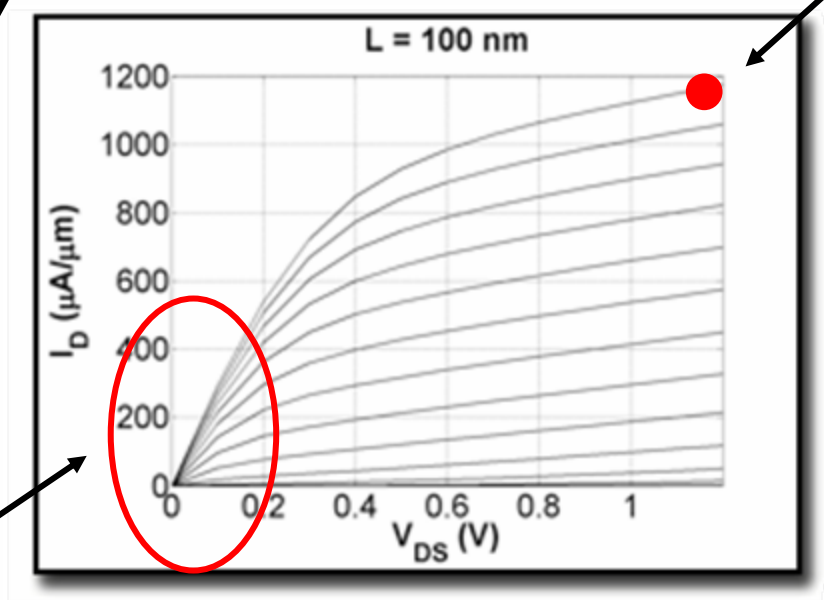
3) A few key device metrics characterize performance.

4) Modern MOSFETs operate between the diffusive and ballistic limits.

summary

'Barrier controlled transport' is responsible for the shape of the MOSFET IV characteristic.

$$I_D = W C_{ox} \upsilon_{sat} \left(V_{GS} - V_T\right)$$



~linear steps

(Courtesy, Shuji Ikeda, ATDF, Dec. 2007)

$$I_D = \frac{W}{L} \mu_{eff} C_{ox} \left(V_{GS} - V_T\right) V_{DS}$$

The specific transport model determines the magnitude of the current.

NCN nanoHUB.org

references

A good reference for this lecture is:

Fundamentals of Modern VLSI Devices, by Taur and Ning, Cambridge Univ. Press, 1998.

You may also wish to consult the online lectures:

Nanoscale Transistors, by Mark Lundstrom, https://www.nanohub.org/courses/nanoscale_transistors

These references discuss the physics of DIBL, subthreshold swing, etc.