EE-612:
Lecture 12:
2D Electrostatics

Mark Lundstrom
Electrical and Computer Engineering
Purdue University
West Lafayette, IN USA
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NCN

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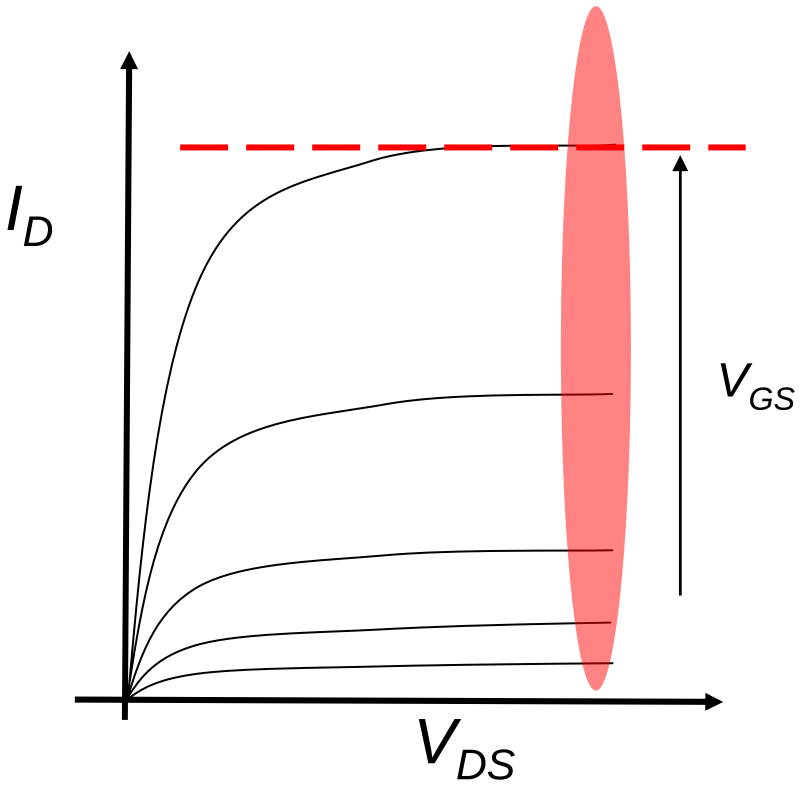
outline

1) **Consequences of 2D electrostatics**
2) 2D Poisson equation
3) Charge sharing model
4) Barrier lowering
5) 2D capacitor model
6) Geometric screening length
7) Discussion
8) Summary

I_D vs. V_{DS} (long channel)



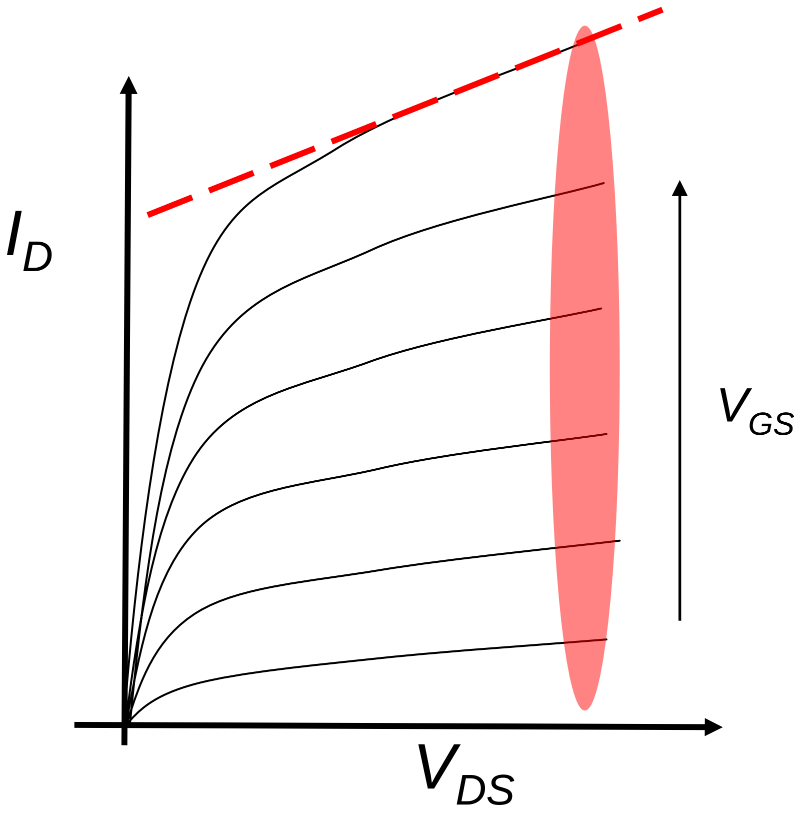
1) square law

$$I_D = \frac{W}{2L}\mu_{eff}C_{ox}\frac{\left(V_{GS}-V_T\right)^2}{m}$$

2) low output conductance

$$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}}$$

I_D vs. V_{DS} (short channel)



1) linear with V_{GS}

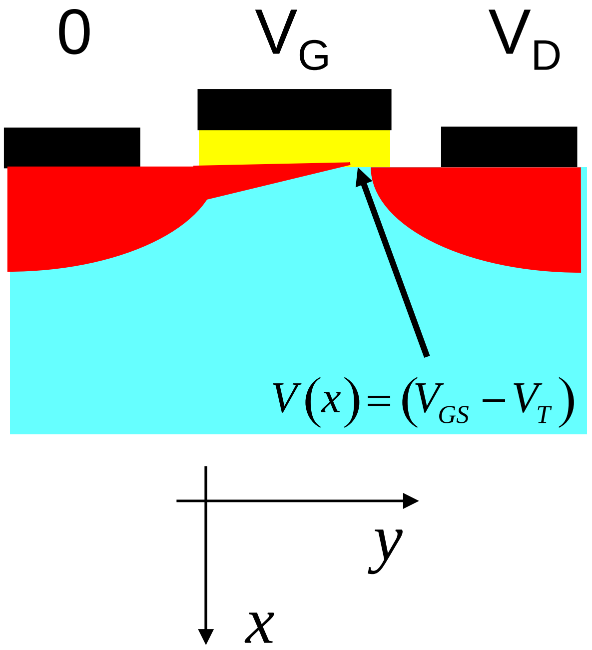
$$I_D = W \upsilon_{sat} C_{ox} \left(V_{GS} - V_T\right)$$

2) high output conductance

$$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}}$$

see Taur and Ning, pp. 154-158

channel length modulation



$$I_D = \mu_{eff} C_{ox} \frac{W}{2L'} (V_{GS} - V_T)^2$$

$$V_{GS} > V_T$$

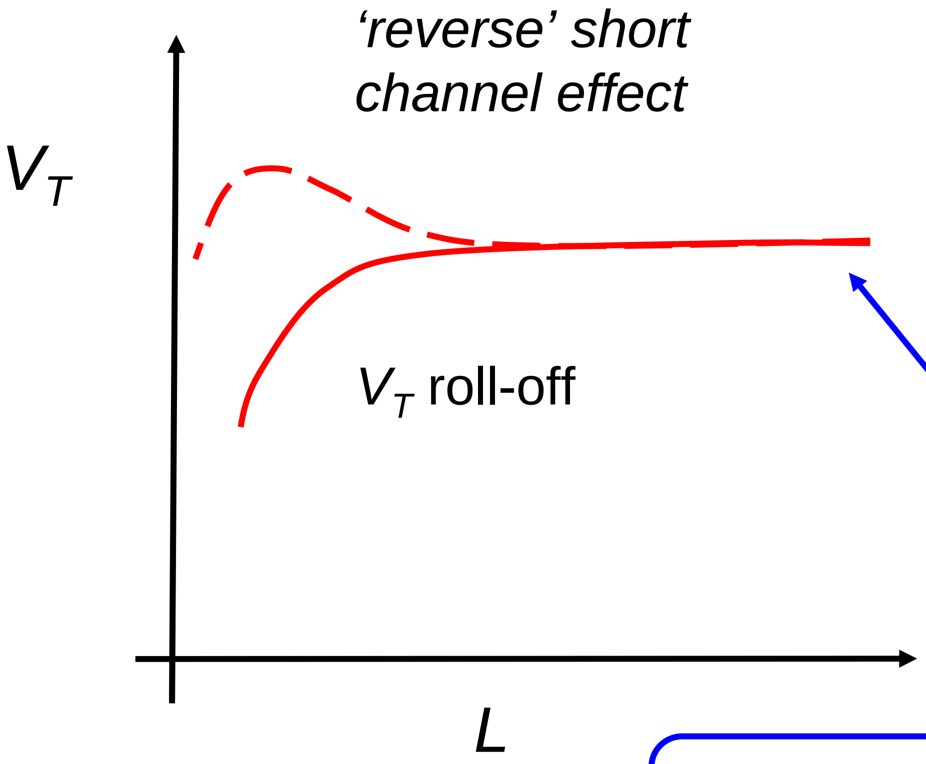
$$V_{DS} > V_{GS} - V_T$$

$$L' = L - \Delta L < L$$

pinch-off region:

1) high lateral electric field $E_y >> E_x$
2) small carrier density
3) under control of drain, not gate (GCA does not apply)

V_T roll-off



'reverse' short channel effect

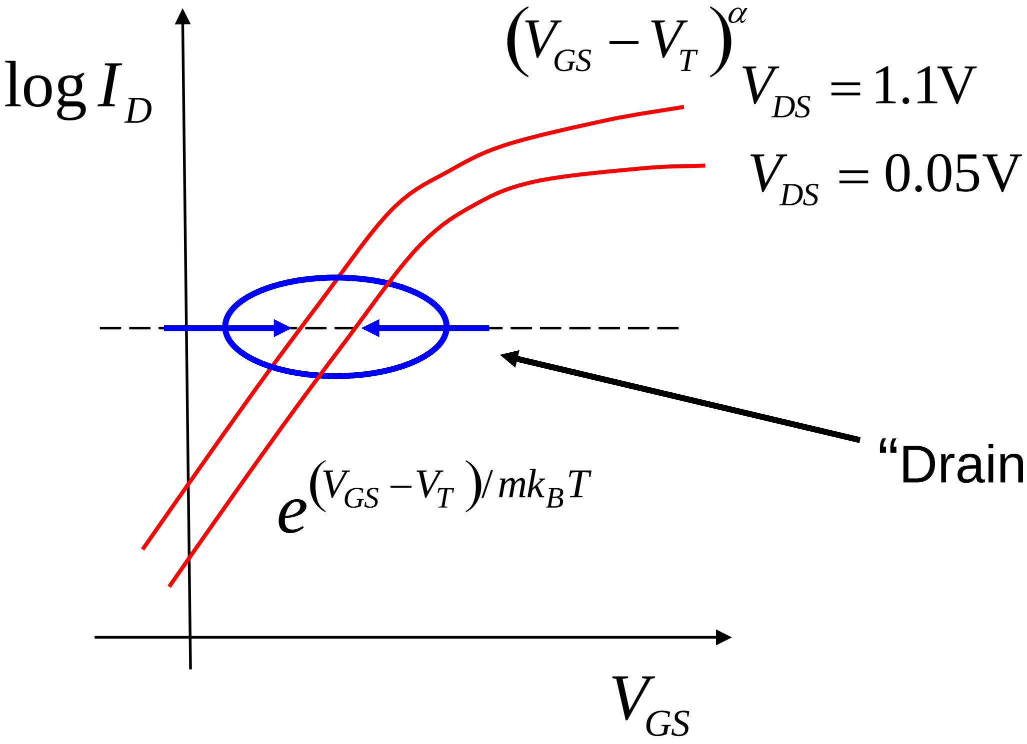
V_T

V_T roll-off

L

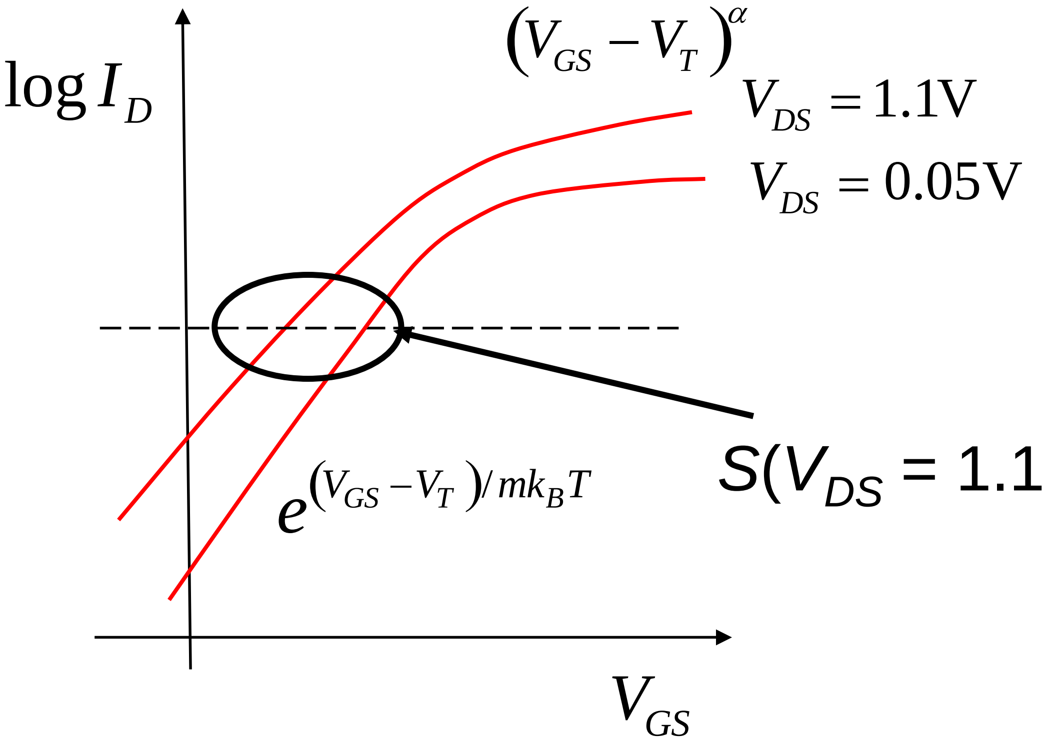
$$V_T = V_{FB} + 2\psi_B + \sqrt{2q\varepsilon_{Si} N_A (2\psi_B)} \big/ C_{ox}$$

DIBL



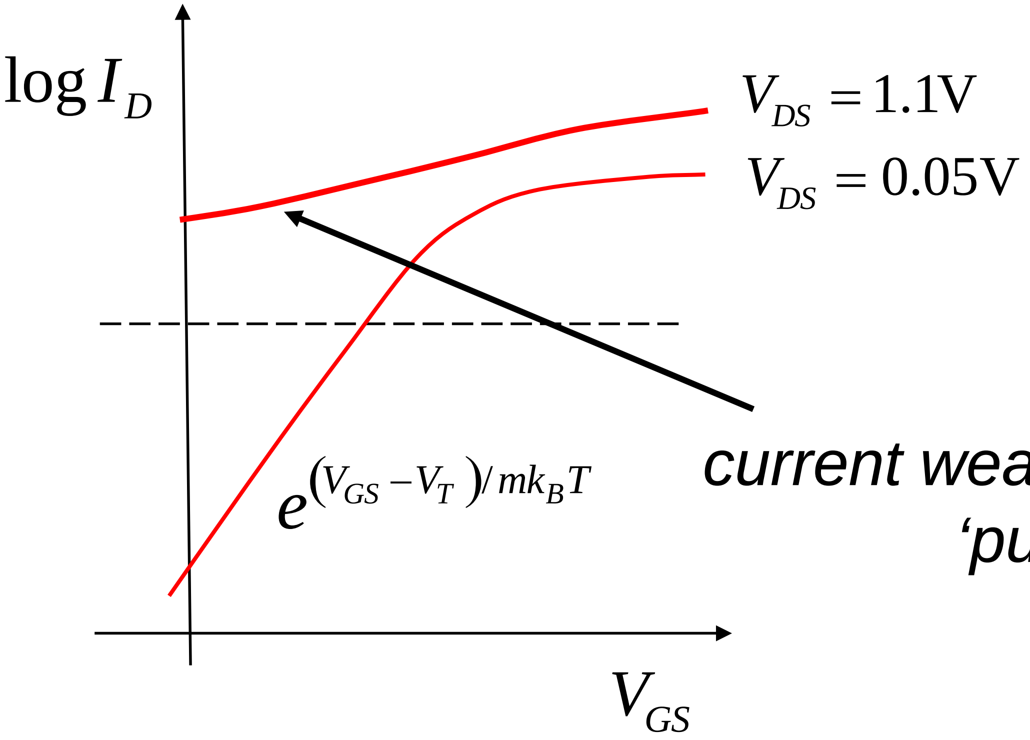
"Drain-Induced Barrier Lowering"
(DIBL) mV/V

stronger short channel effects



$S(V_{DS} = 1.1\mathrm{V}) > S(V_{DS} = 0.05\mathrm{V})$

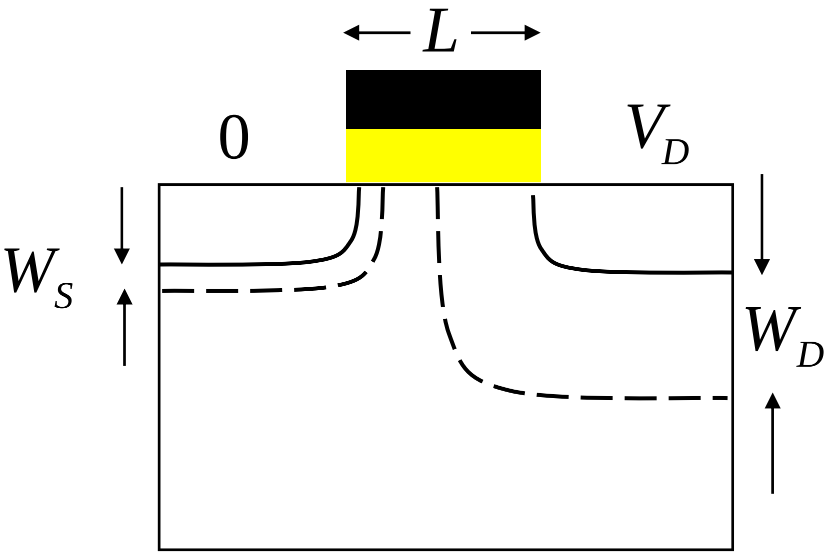
severe short channel effects



current weakly dependent on V_{GS}

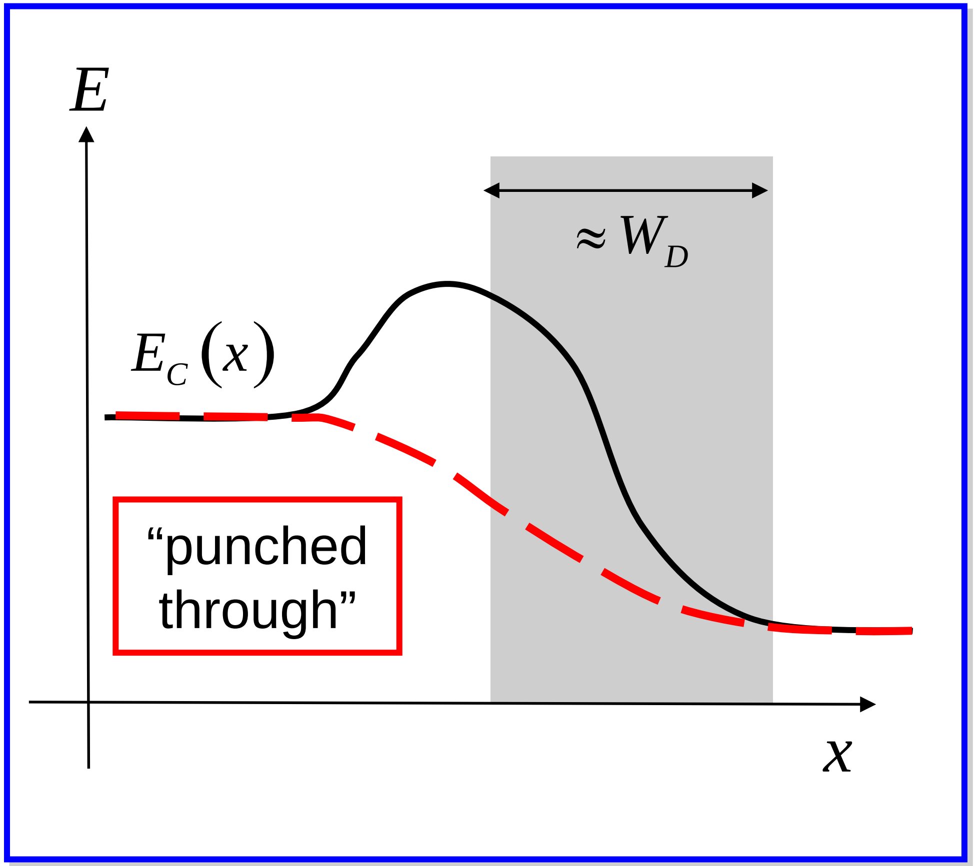
'punch through'

punchthrough



$$N_A(\min): \text{punch through}$$

$$W_S + W_D < L$$



short channel effects

1) I_D linear not quadratic with gate voltage
2) high output conductance
3) threshold voltage roll-off
4) increased DIBL
5) increased S
6) punchthrough

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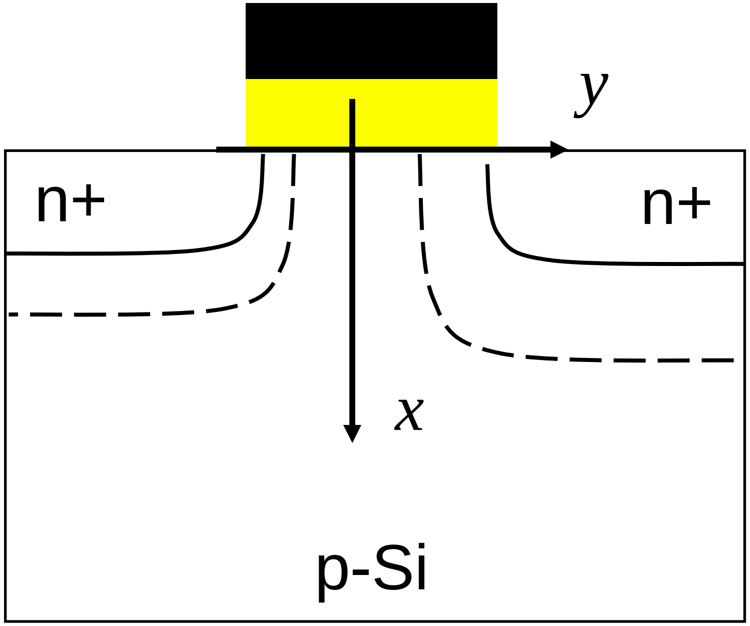
2D Poisson equation



1) MOS Capacitor:

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho}{\varepsilon_{Si}} = \frac{qN_A}{\varepsilon_{Si}} \quad (\text{below} V_T)$$

2) MOSFET:

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}} \quad (\text{below} V_T)$$

2D Poisson equation (ii)

1) Long channel MOSFET below threshold:

$$\frac{\partial^2 \psi}{\partial x^2} >> \frac{\partial^2 \psi}{\partial y^2}$$

gradual channel approximation (GCA):

$$Q_I(y) = -C_G\left[V_G - V_T - mV(y)\right]$$

2D Poisson equation (iii)

1) Short channel MOSFET below threshold:

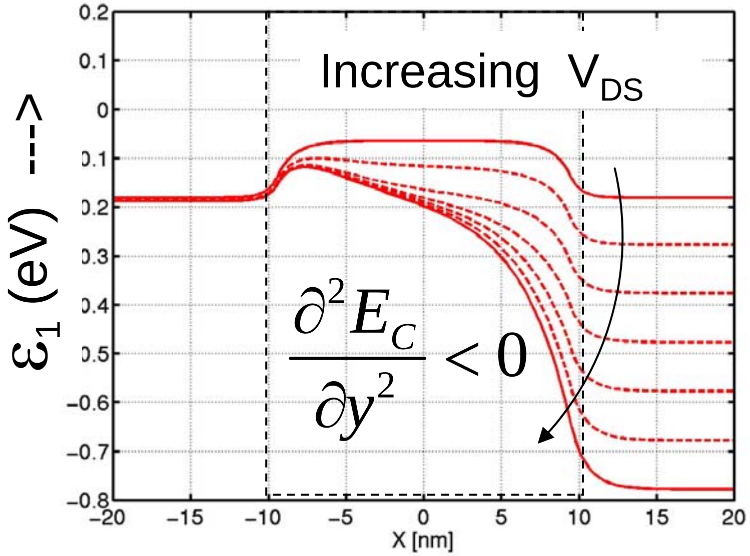
$$\frac{\partial^2 \psi}{\partial x^2} = \frac{qN_A}{\varepsilon_{Si}} - \frac{\partial^2 \psi}{\partial y^2}$$

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{q\,N_A\big|_{eff}}{\varepsilon_{Si}}$$

$$N_A\big|_{eff} < N_A$$

$$V_T < V_T(\text{long channel})$$

explains V_T roll-off



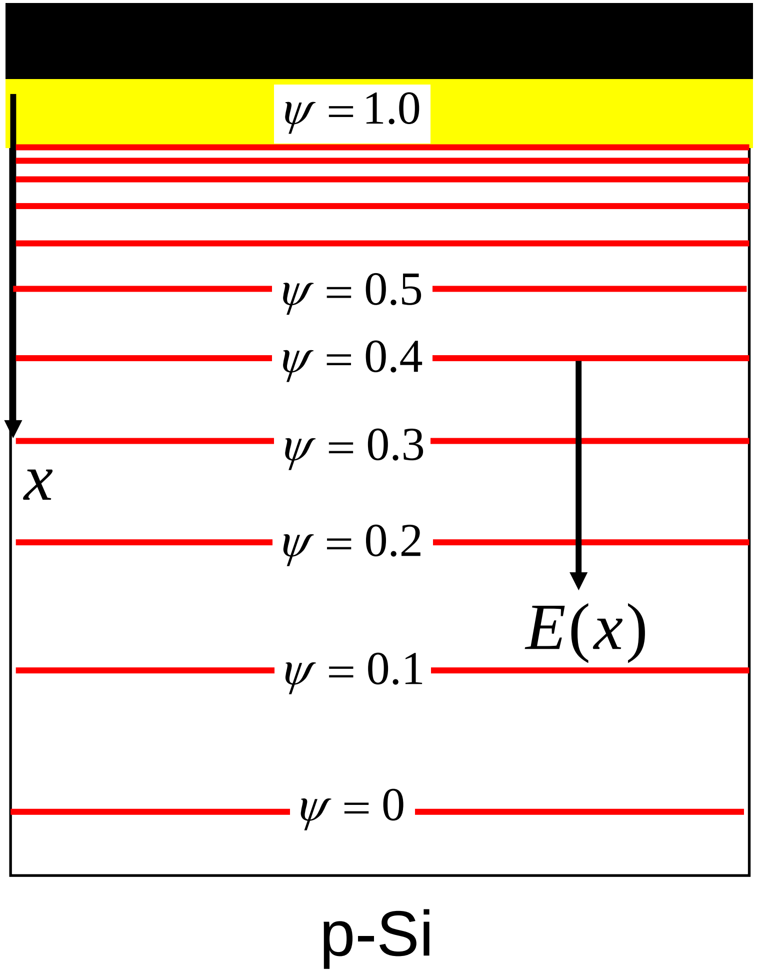
ε_1 (eV) --->

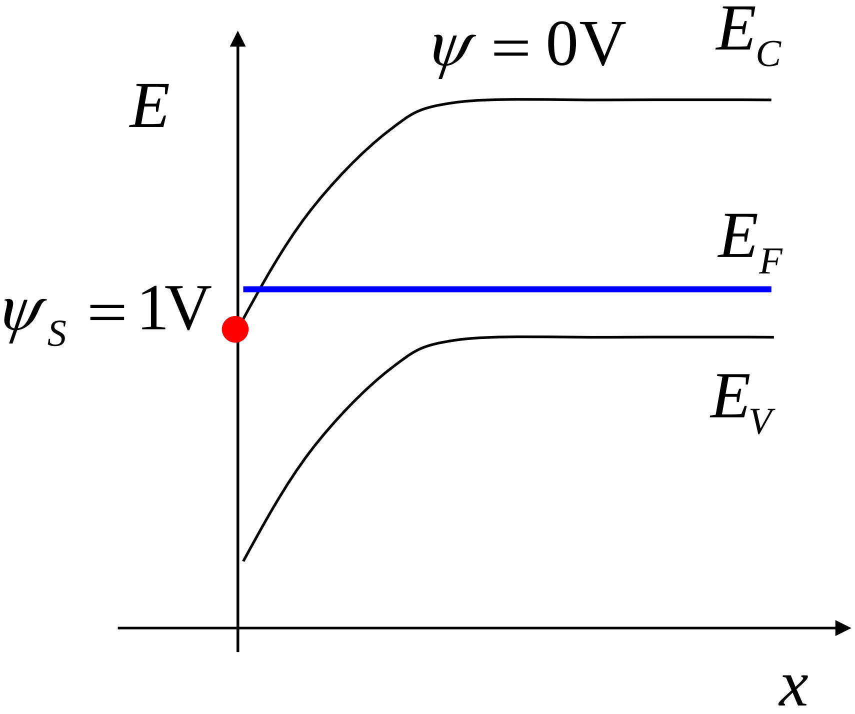
Increasing V_{DS}

$$\frac{\partial^2 E_C}{\partial y^2} < 0$$

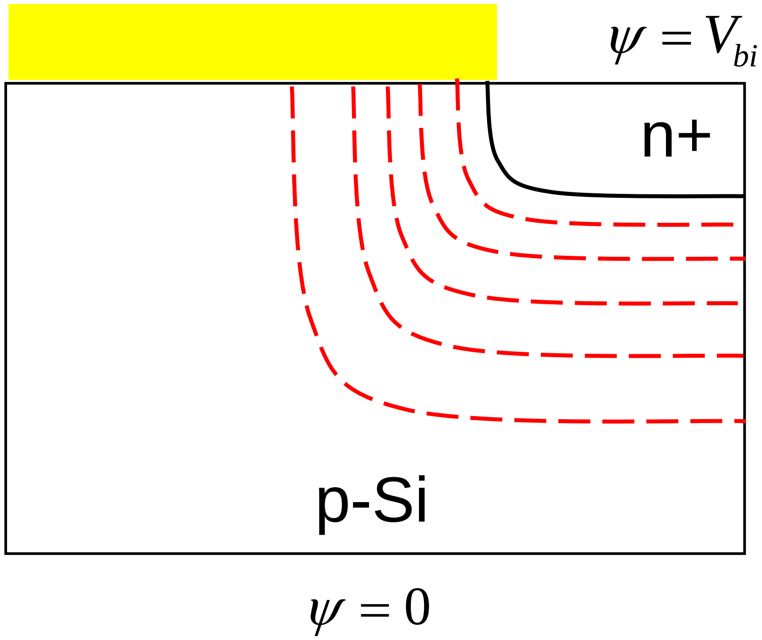
y (nm) --->

2D potential contours

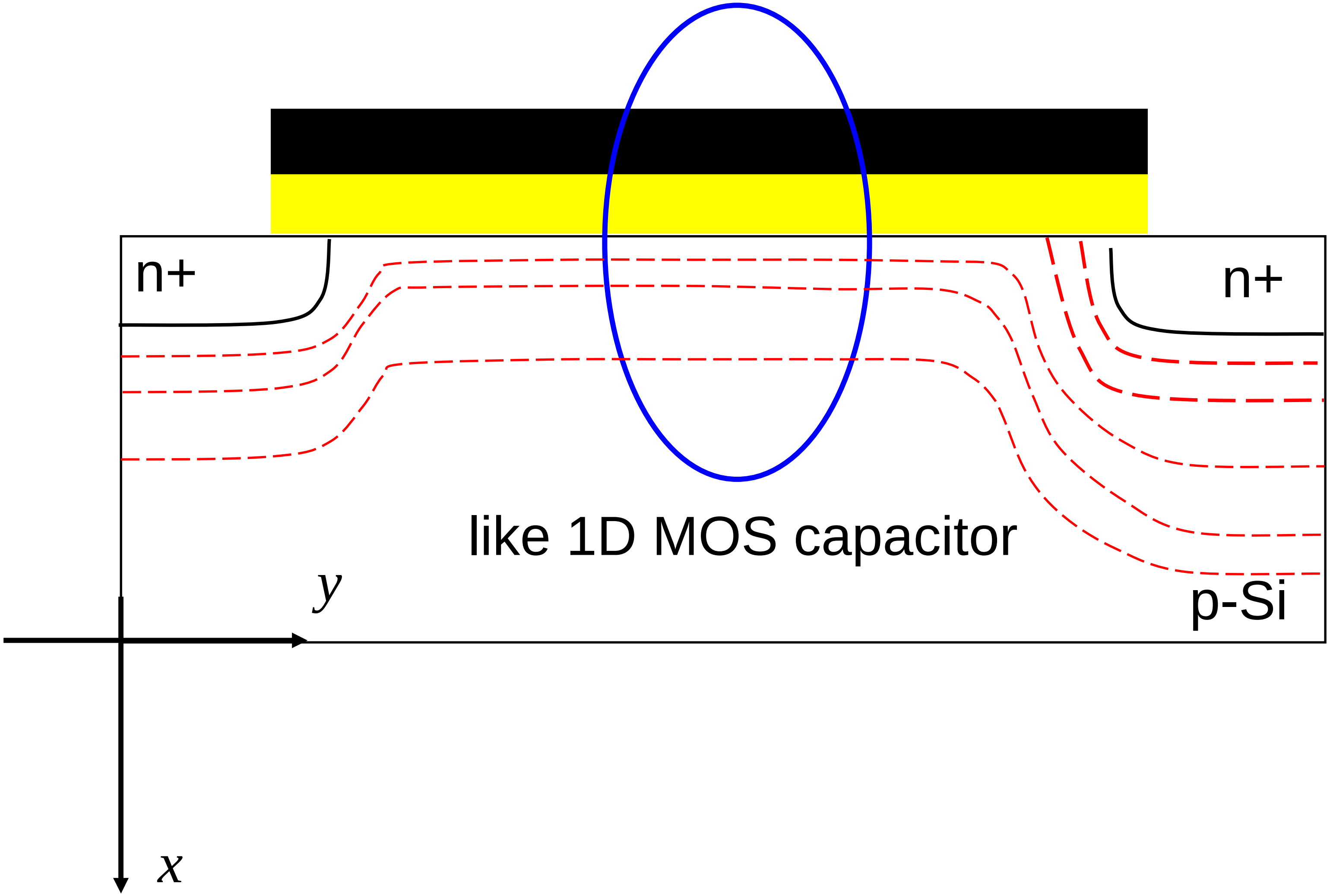




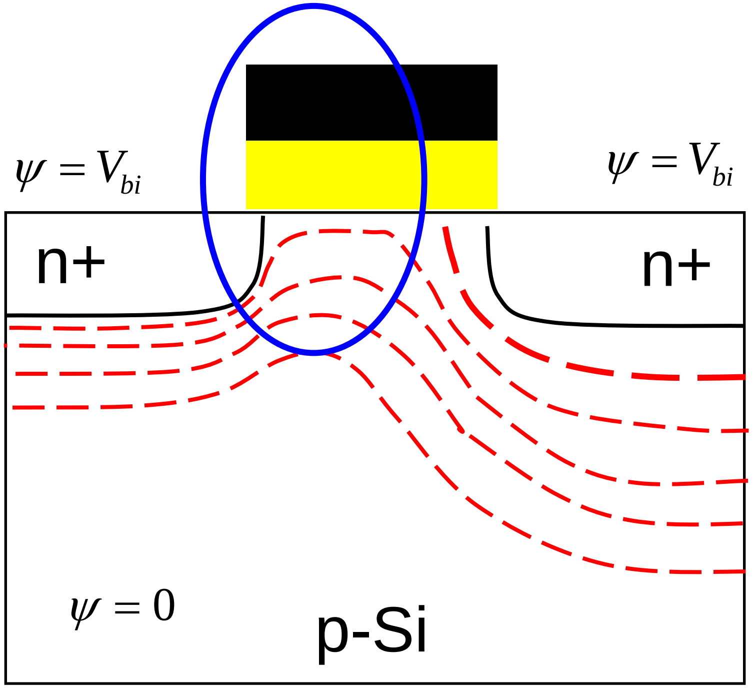
2D potential contours



2D potential contours (long channel)

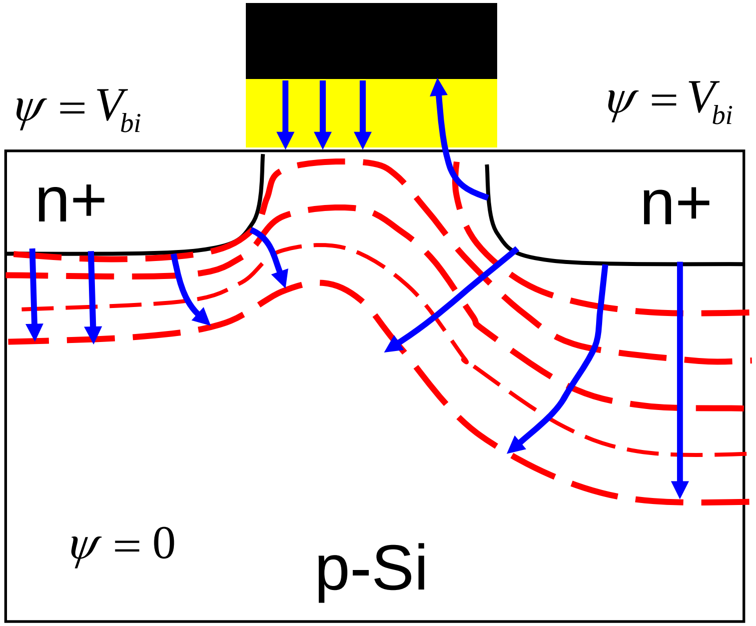


2D potential contours (short channel)

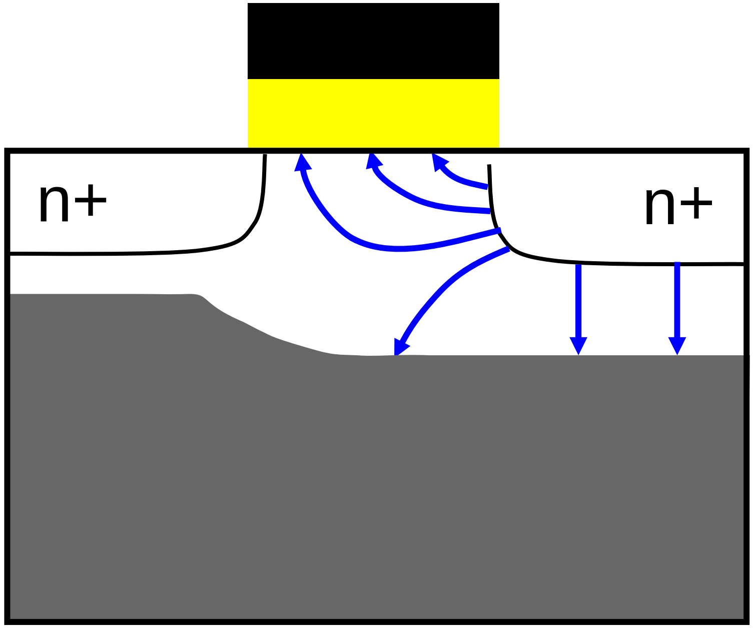


(See Fig. 3.18 of Taur and Ning)

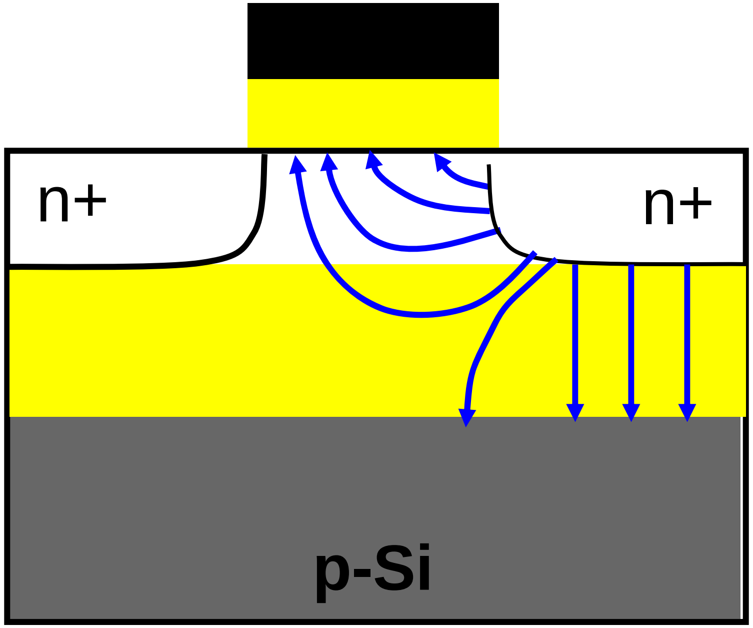
field lines



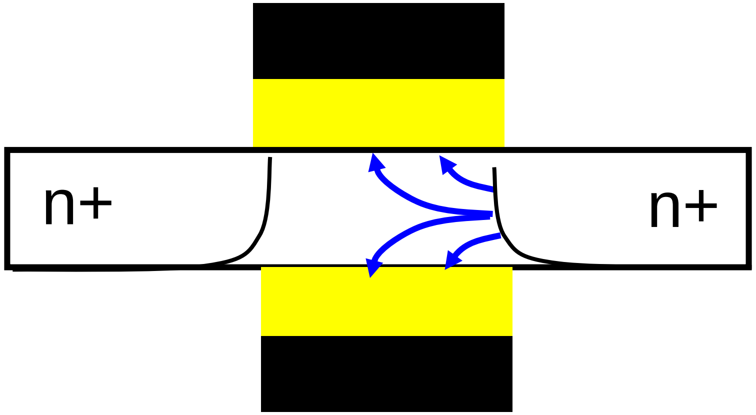
field lines (bulk)



field lines (SOI)



field lines (SOI)



‘gate all around’

FINFET

tri-gate

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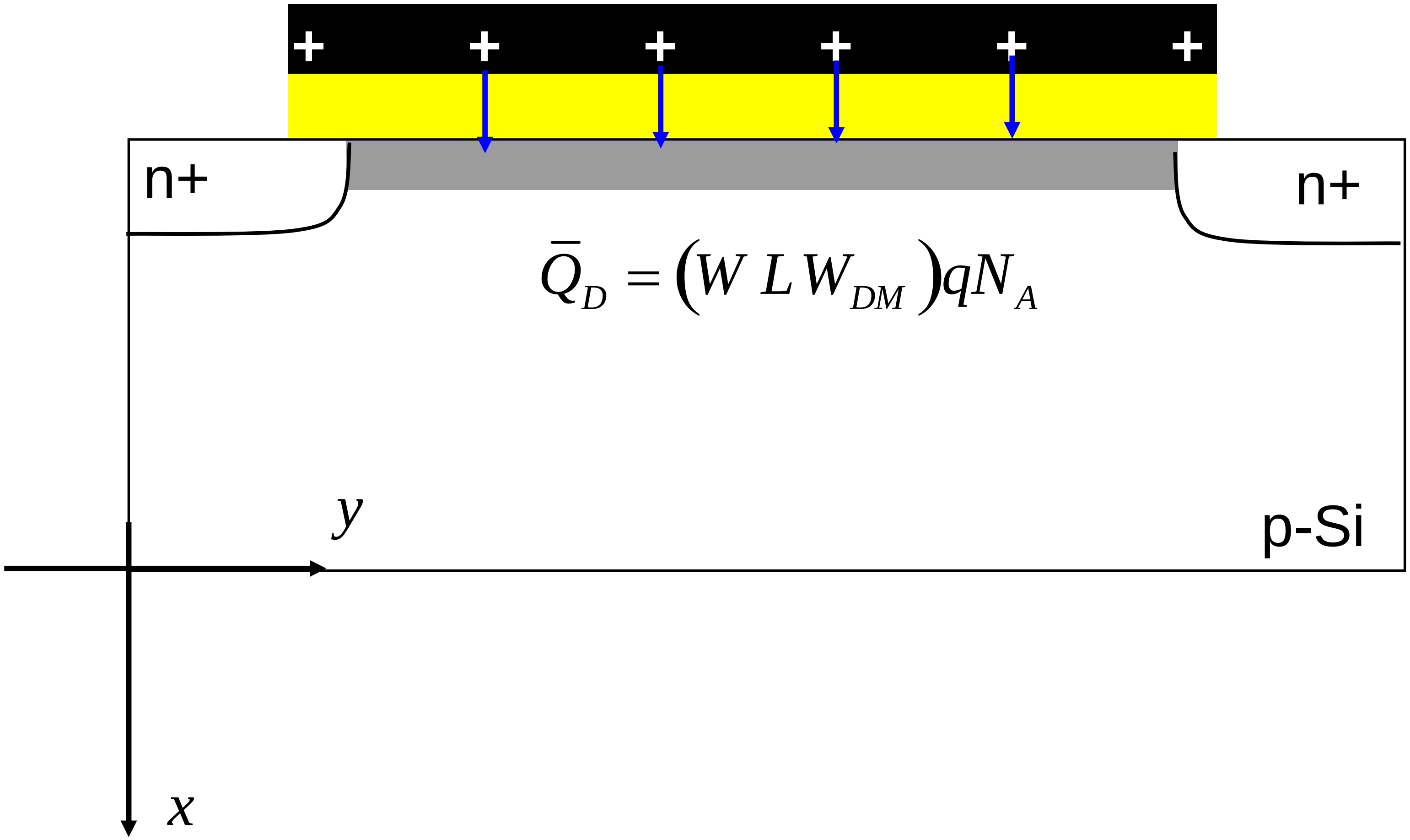
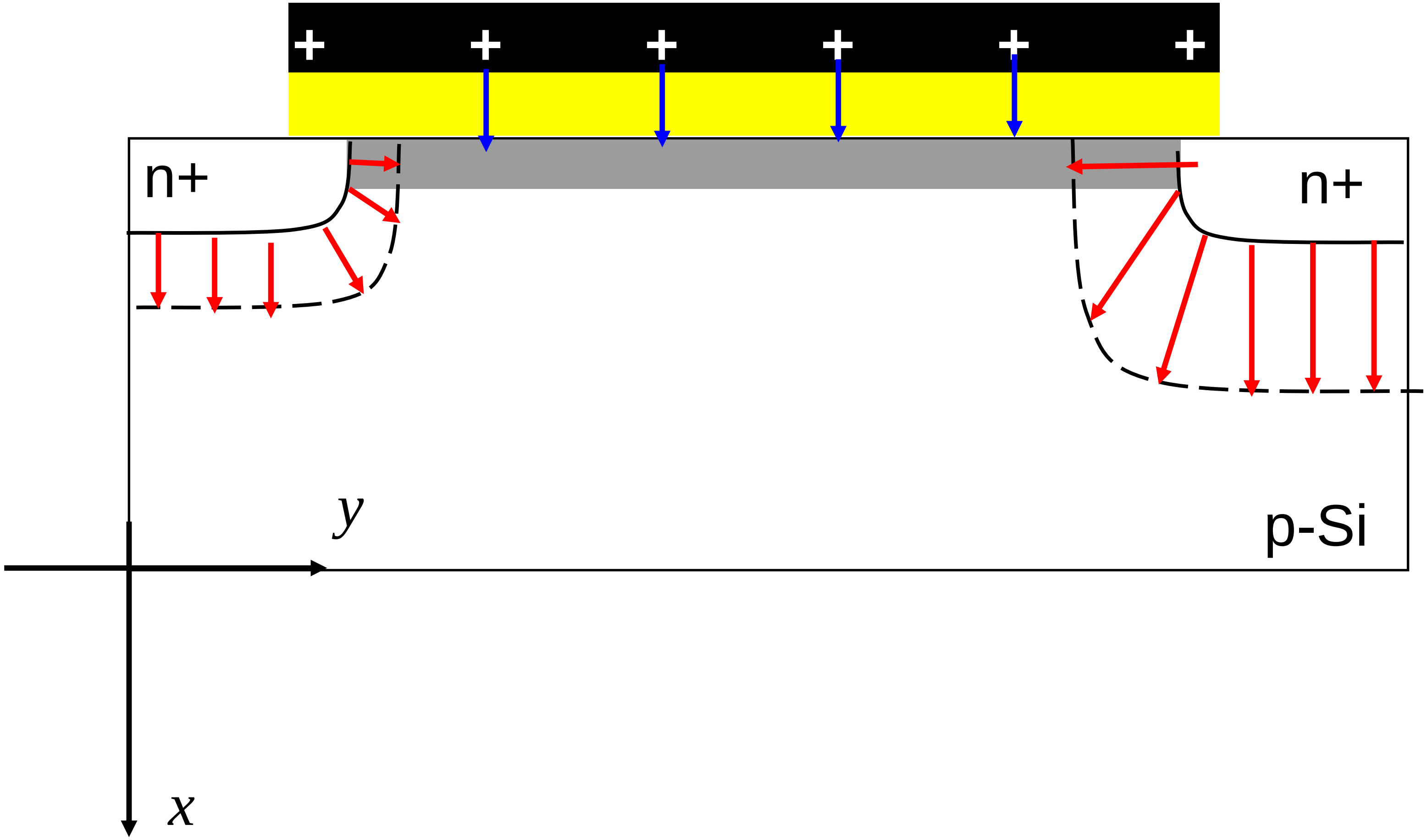
charge sharing model

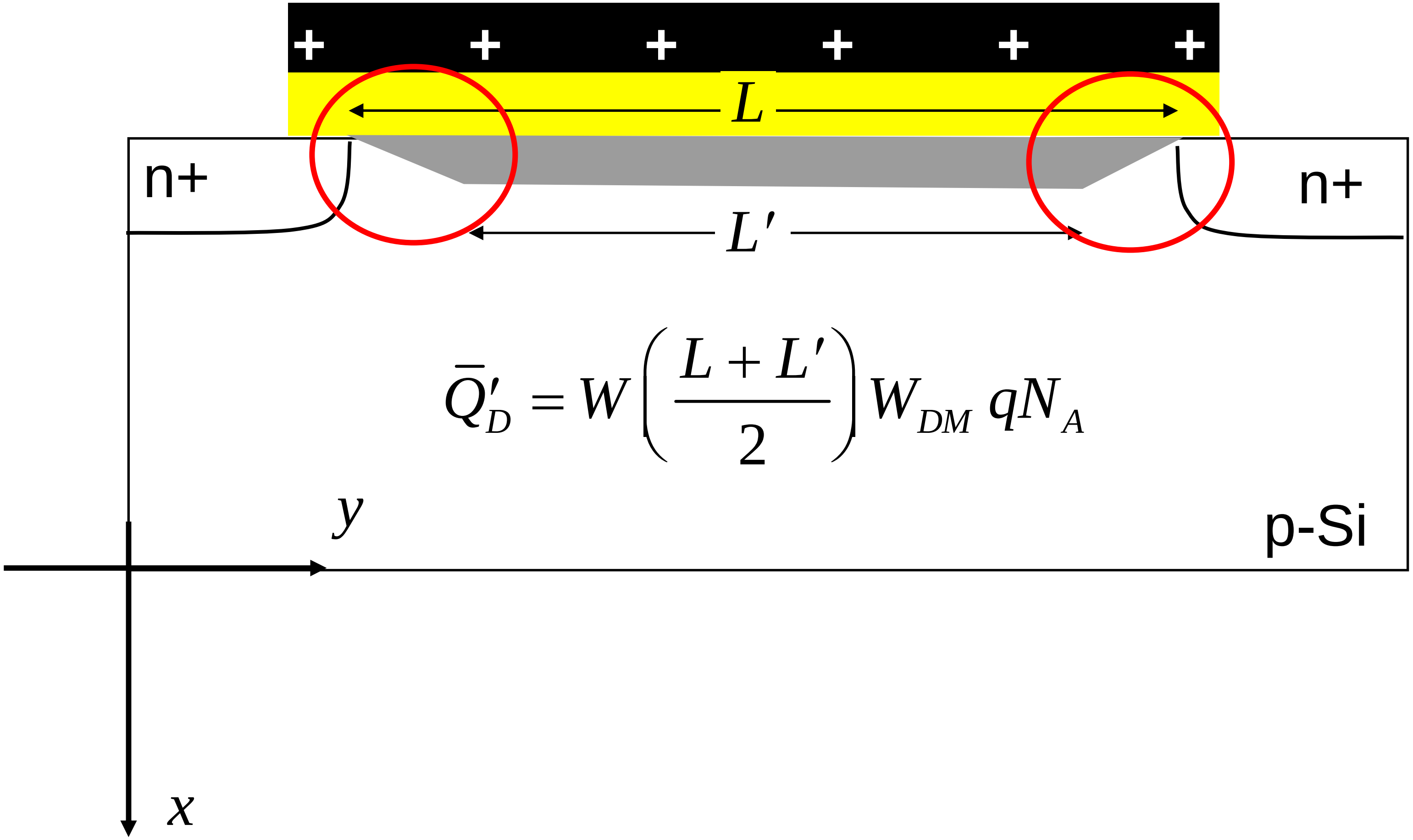


$$\bar{Q}_D = \left(W\,L\,W_{DM}\right) q N_A$$

charge sharing model (ii)



charge sharing model (ii)



$$\bar{Q}_D' = W\left(\frac{L+L'}{2}\right)W_{DM}\,qN_A$$

charge sharing model (iii)

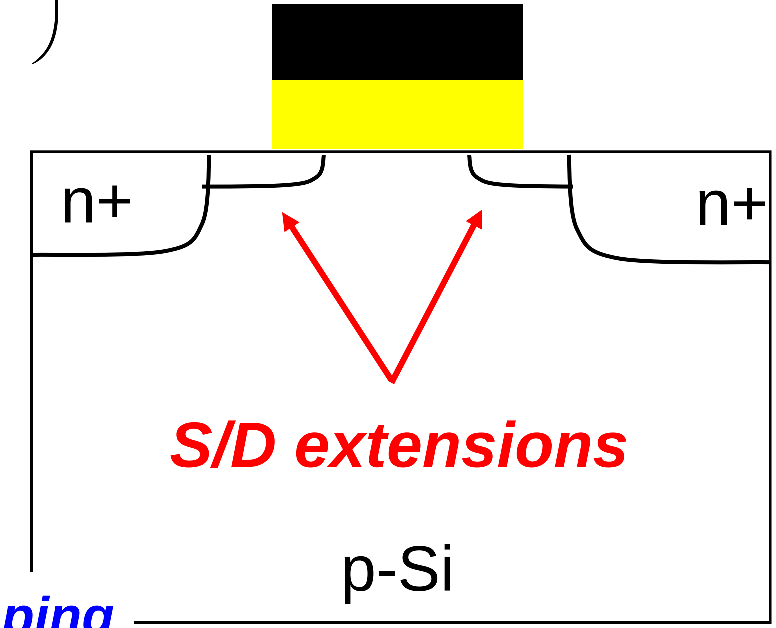
$$V_T = V_{FB} + 2\psi_B - \gamma \frac{Q_D}{C_{OX}} < V_T\left(\text{long channel}\right)$$

$$\gamma = \frac{L + L'}{2L} = 1 - \frac{x_j}{L}\left(\sqrt{1 + \frac{2W_{DM}}{x_j}} - 1\right)$$

(prob. 3.6, Taur and Ning)

for $\gamma \sim 1$, need: $\begin{cases} x_j << L \\ W_{DM} << x_j \end{cases}$

increase channel doping



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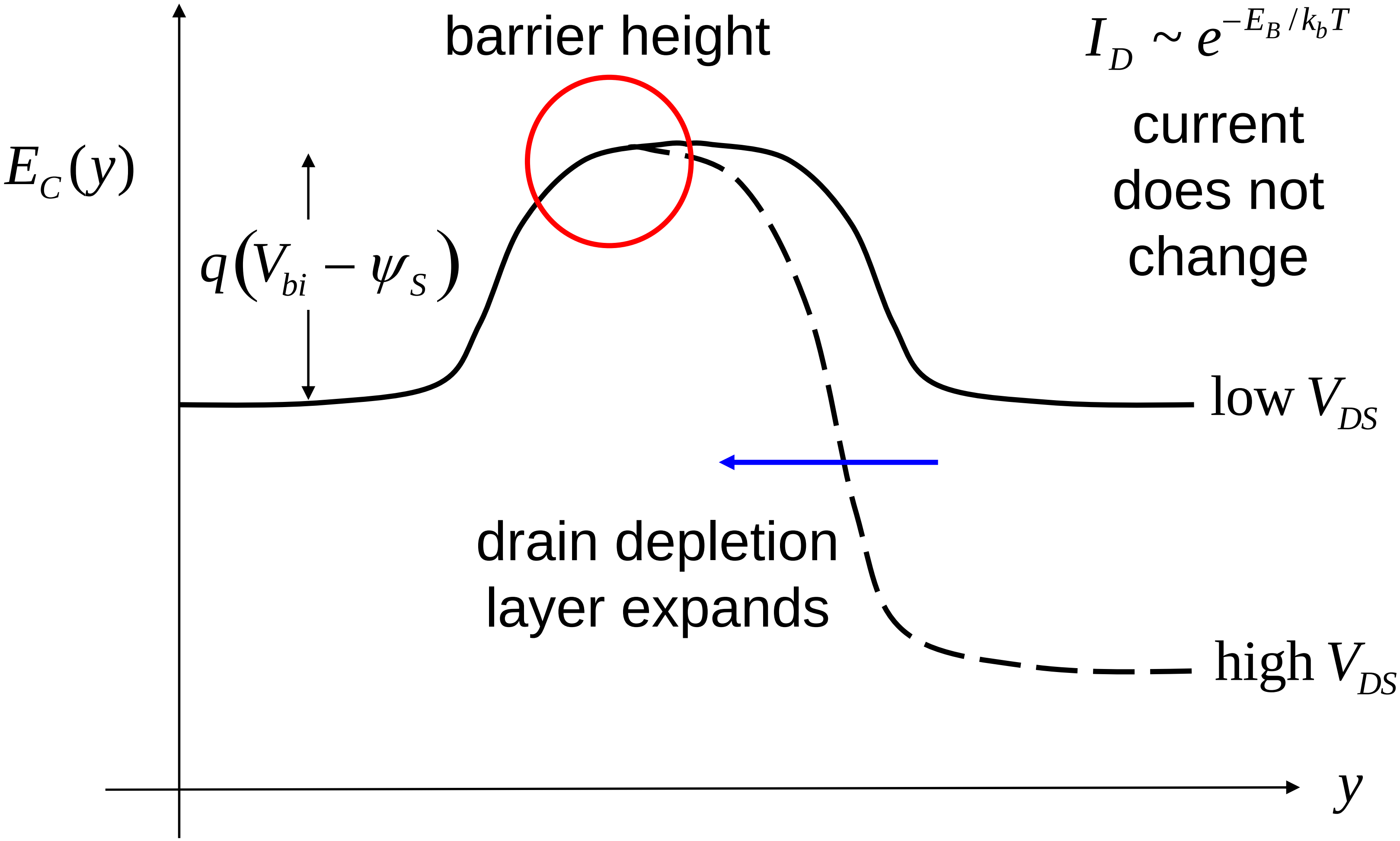
barrier lowering



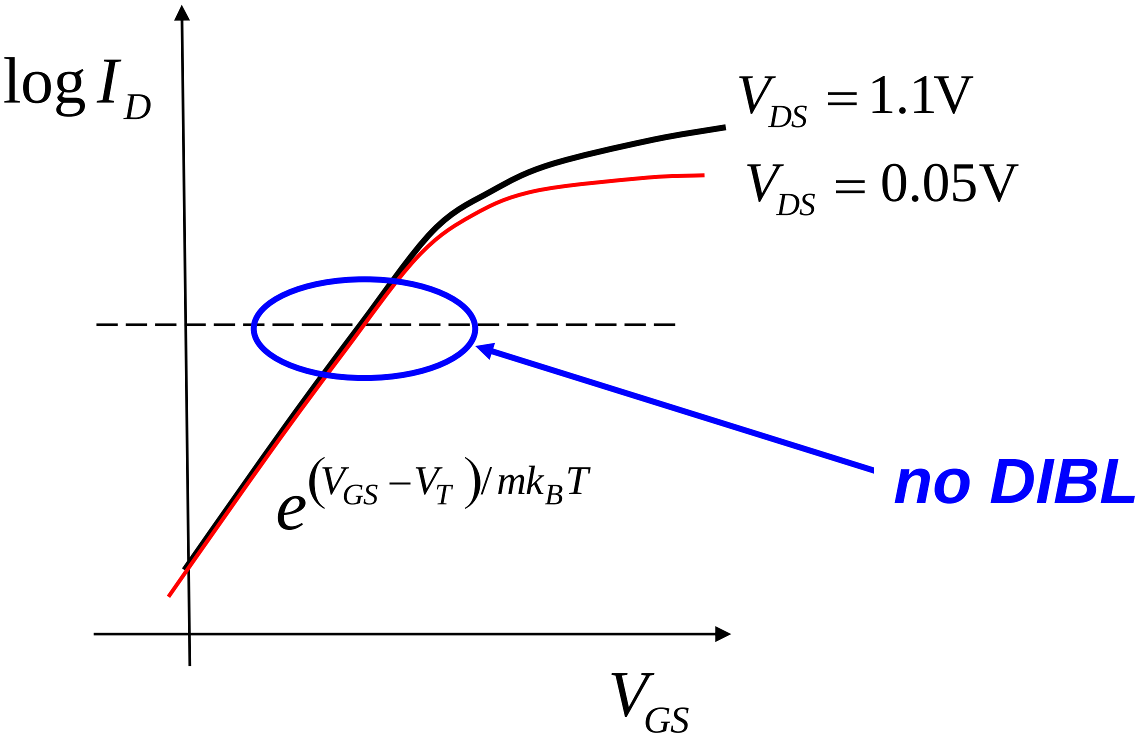
gate controls barrier height

$$I_D \sim e^{-E_B/k_bT}$$

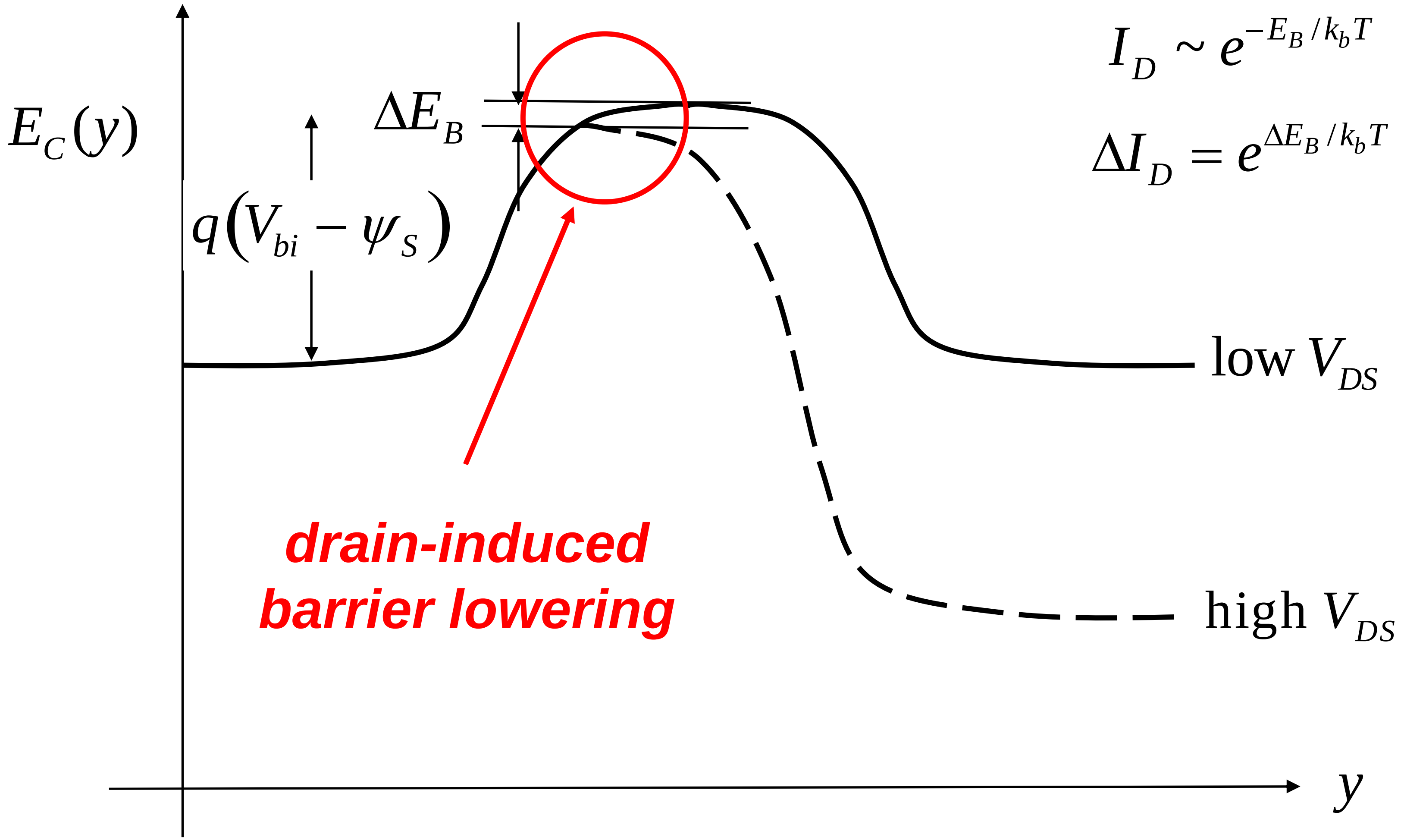
current does not change

drain depletion layer expands

barrier lowering (ii)



barrier lowering (iii)

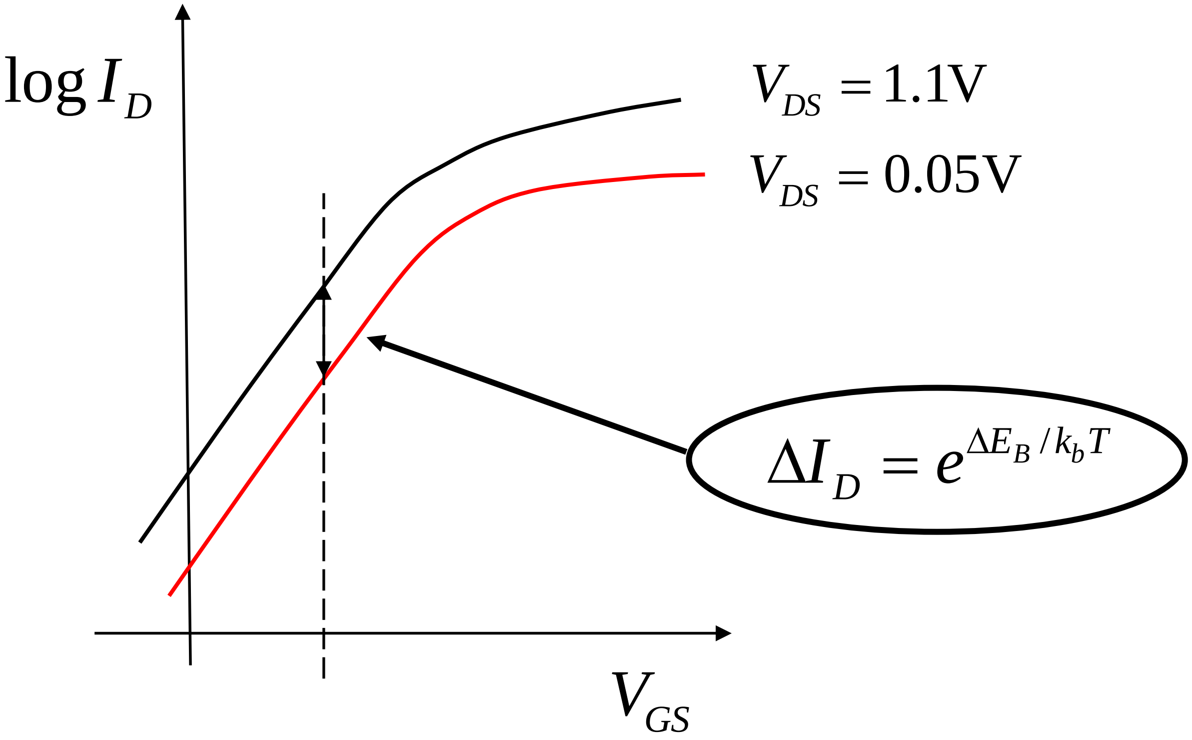


$$I_D \sim e^{-E_B / k_b T}$$

$$\Delta I_D = e^{\Delta E_B / k_b T}$$

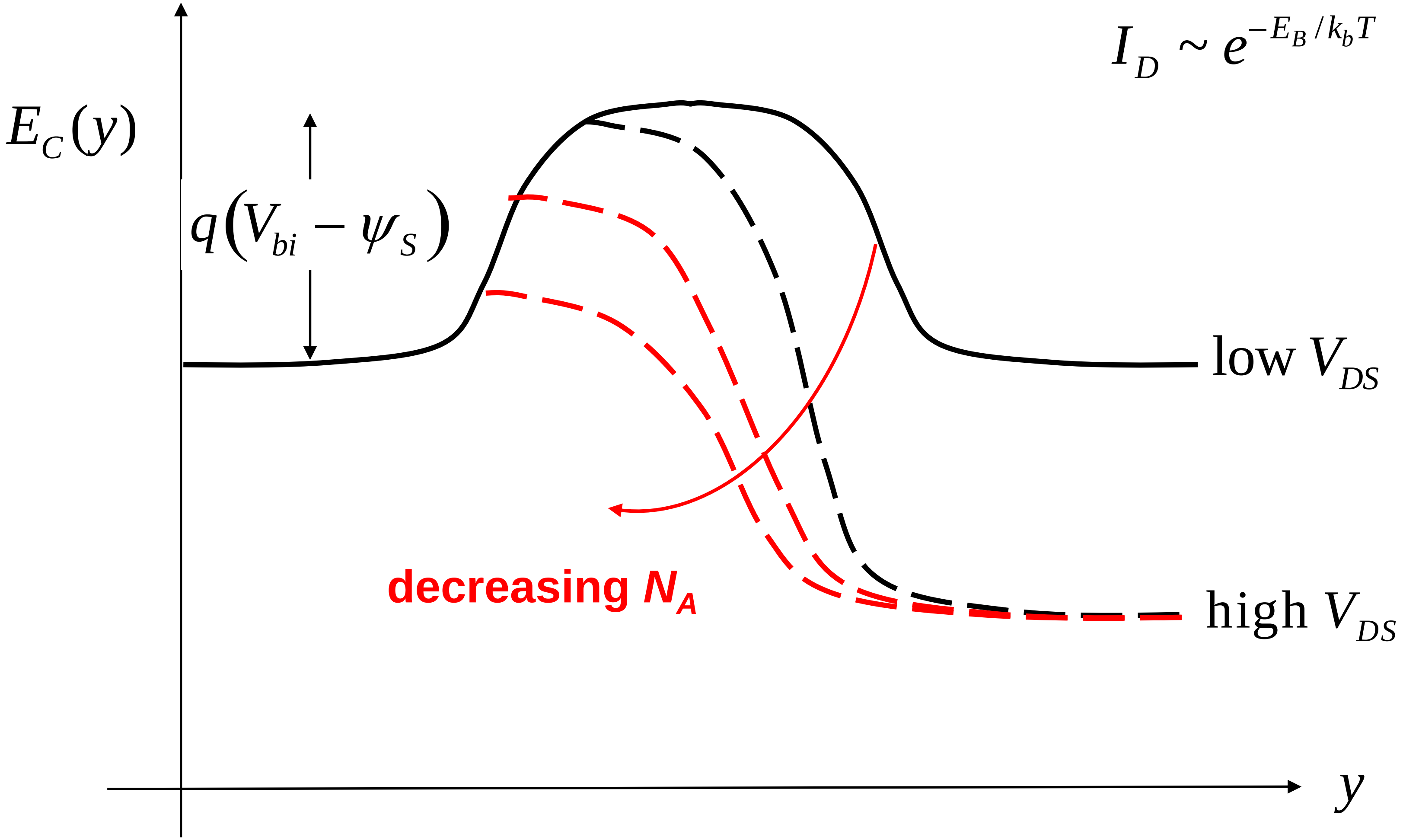
drain-induced barrier lowering

barrier lowering (iv)

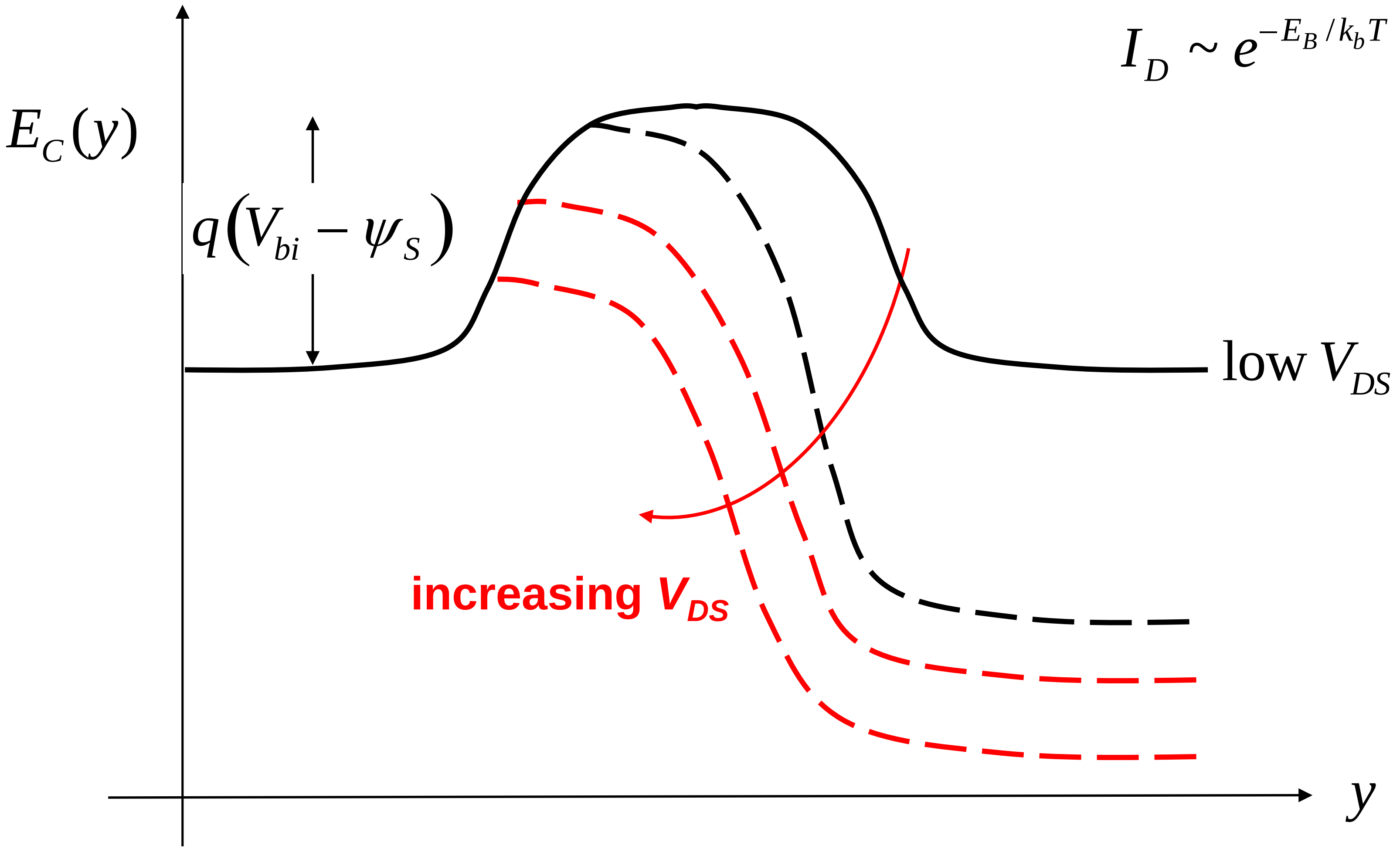


$$\Delta I_D = e^{\Delta E_B / k_b T}$$

punchthrough

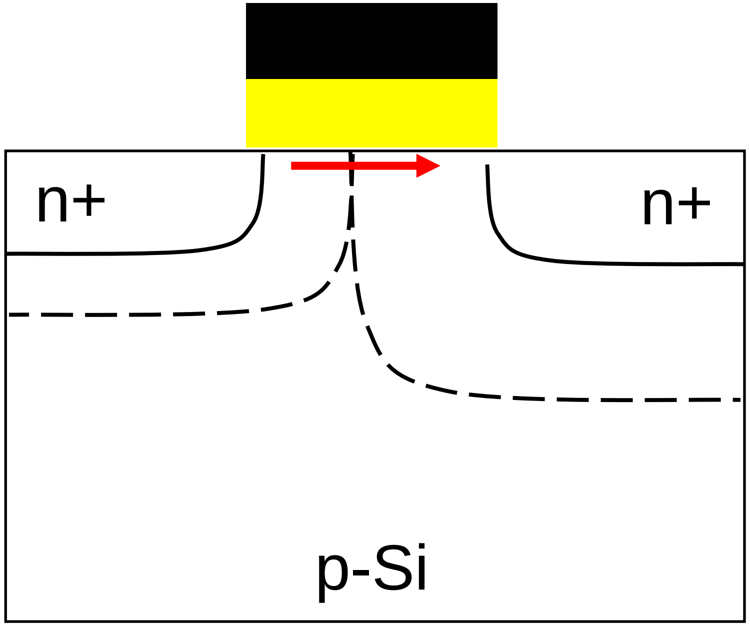


punchthrough (ii)

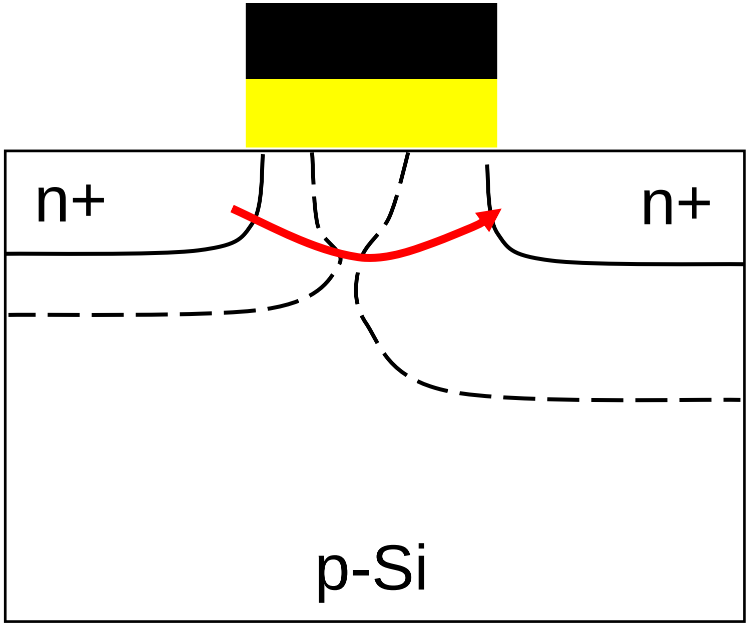


punchthrough (iii)

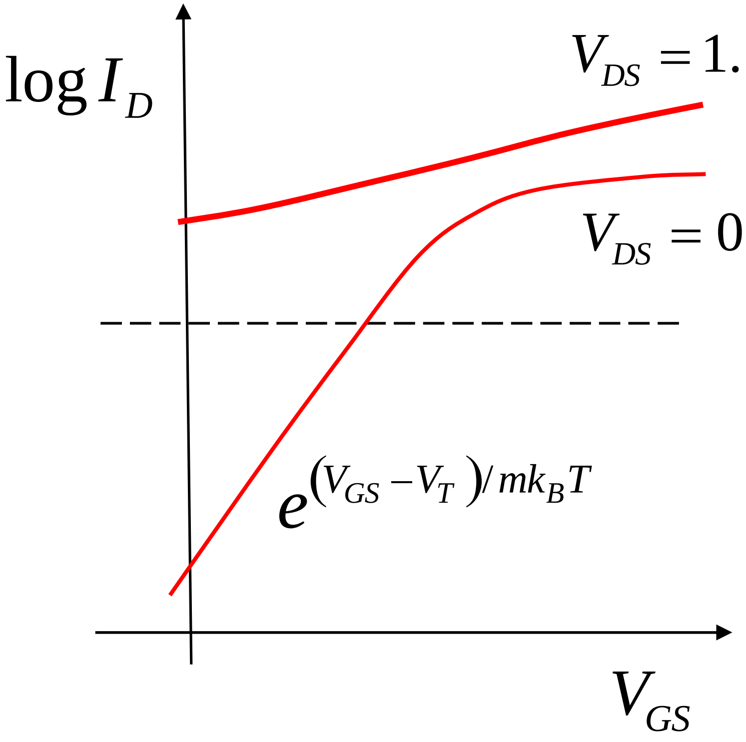
surface punchthrough

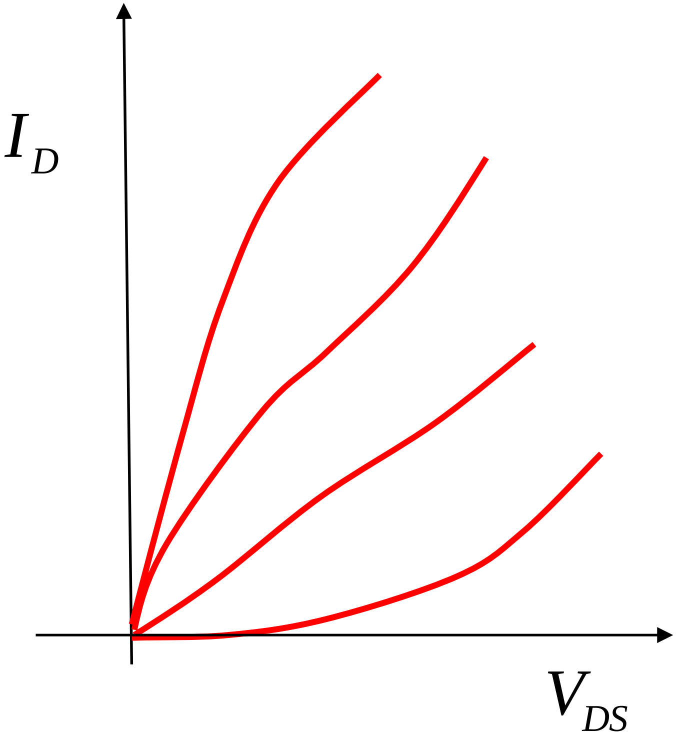


bulk punchthrough



punchthrough (iv)





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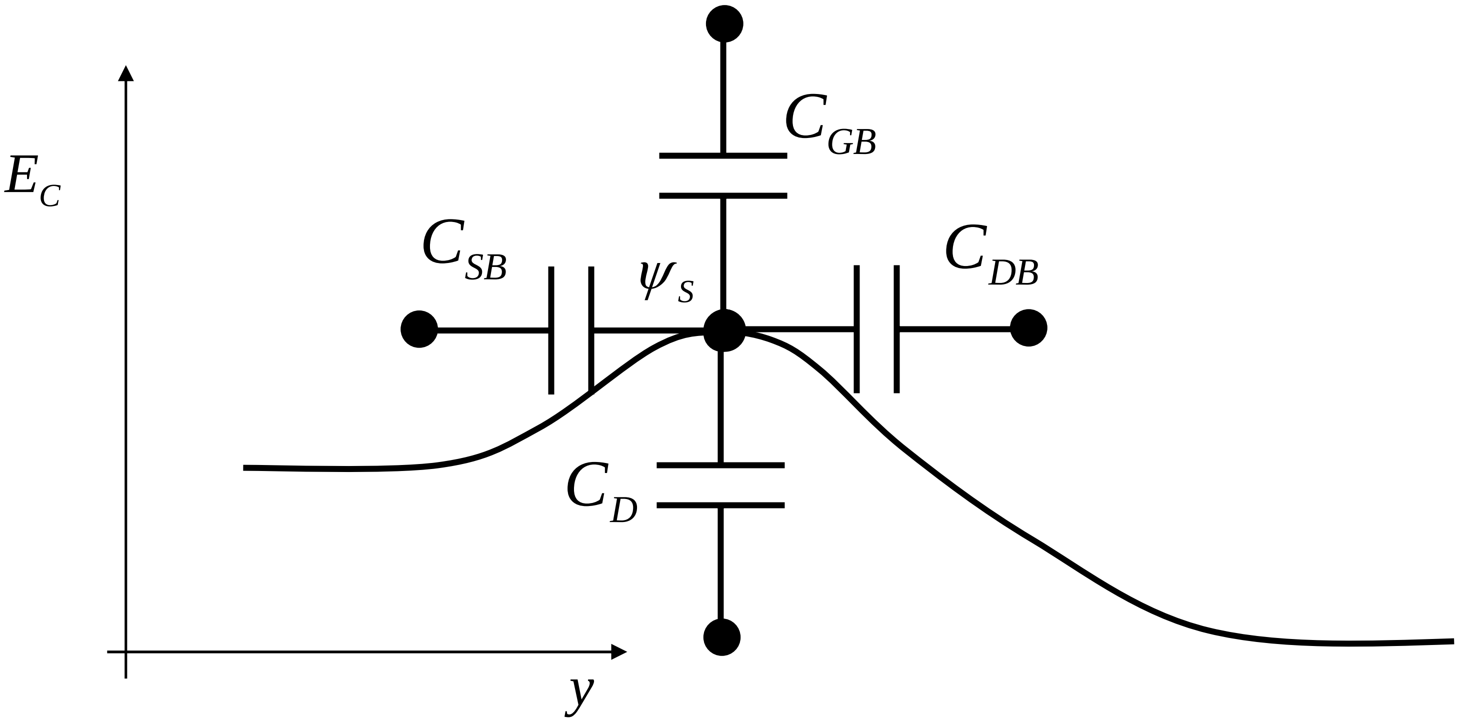
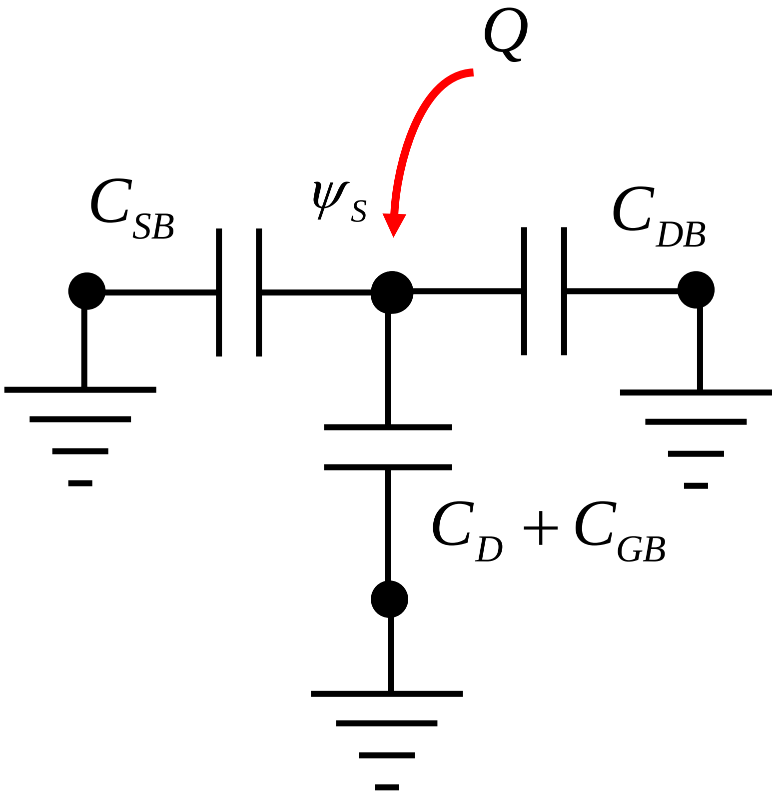
2D capacitor model



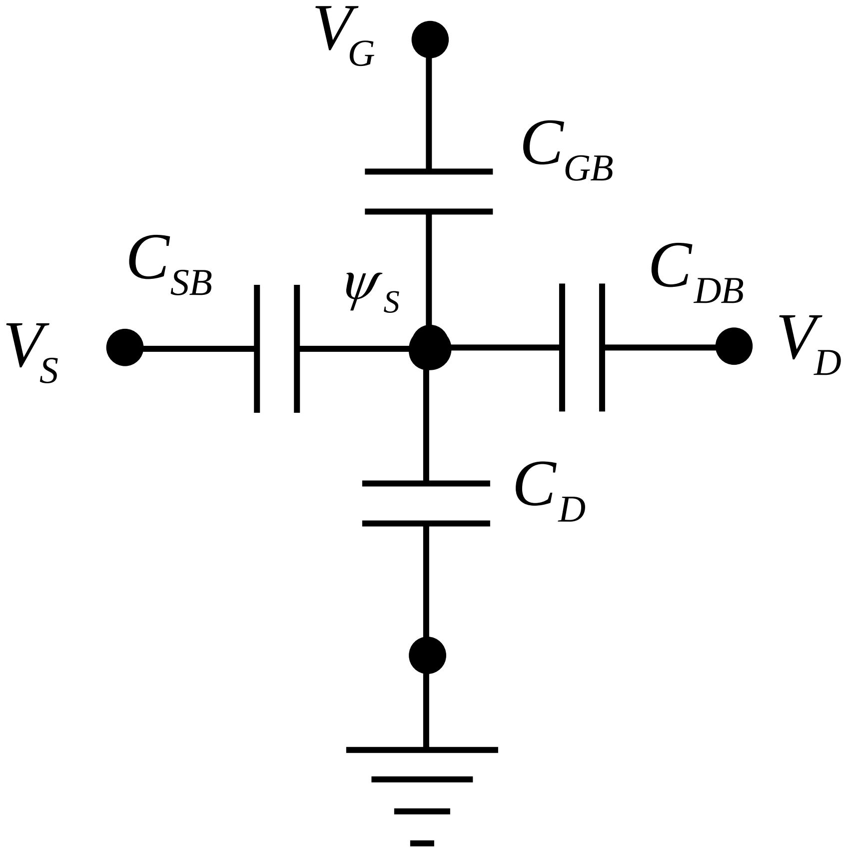
2D capacitor model ($V = 0$)



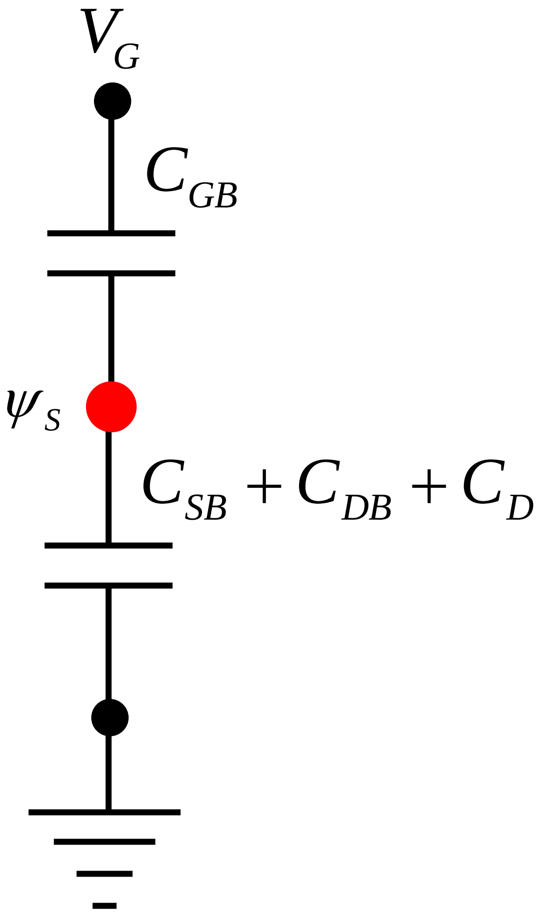
$$\psi_S = \frac{Q}{C_\Sigma}$$

$$C_\Sigma = C_{GB} + C_{SB} + C_{DB} + C_D$$

2D capacitor model (Q = 0)



$$V_S = V_D = 0$$



$$\psi_S = \frac{C_{GB}}{C_\Sigma} V_G$$

2D capacitor model (general solution)

$$\boxed{\psi_S = \frac{C_{GB}}{C_\Sigma}V_G + \frac{C_{SB}}{C_\Sigma}V_S + \frac{C_{DB}}{C_\Sigma}V_D + \frac{Q}{C_\Sigma}}$$

$$C_\Sigma = C_{GB} + C_{SB} + C_{DB} + C_D$$

$$C_{GB} = C_{ox}WL \qquad C_D = \text{depletion layer capacitance}$$

recall:

$$V_G = \psi_S - \frac{Q}{C_{ox}}$$

2D capacitor model ($V_S = Q = 0$)

$$\boxed{\psi_S = \frac{C_{GB}}{C_\Sigma} V_G + \frac{C_{DB}}{C_\Sigma} V_D}$$

$$\frac{\partial \psi_S}{\partial V_G} = \frac{C_{GB}}{C_\Sigma} \qquad \frac{\partial \psi_S}{\partial V_D} = \frac{C_{DB}}{C_\Sigma}$$

$$\frac{\partial \psi_S}{\partial V_G} >> \frac{\partial \psi_S}{\partial V_D} \Rightarrow \boxed{C_{GB} >> C_{DB}}$$

need $t_{ox} << L$

2D capacitor model

$$\psi_S = \frac{C_{GB}}{C_\Sigma} V_G + \frac{C_{DB}}{C_\Sigma} V_D \qquad \left(V_S = Q = 0 \quad C_\Sigma = C_{DB} + C_D\right)$$

$$I_D \propto e^{q\psi_S / k_B T} = e^{qV_{GS}/mk_B T}$$

$$\boxed{S = 2.3m\left(k_B T/q\right)}$$

$$m = C_\Sigma / C_{GB}$$

$$\boxed{DIBL = C_{DB}/C_{GB}}$$

$$m = \left(C_{GB} + C_{DB} + C_D\right)/C_{GB}$$
$$= \left[1 + \left(C_{DB} + C_D\right)/C_{GB}\right]$$

2D electrostatics: C_{DB} not negligible *S* increases.

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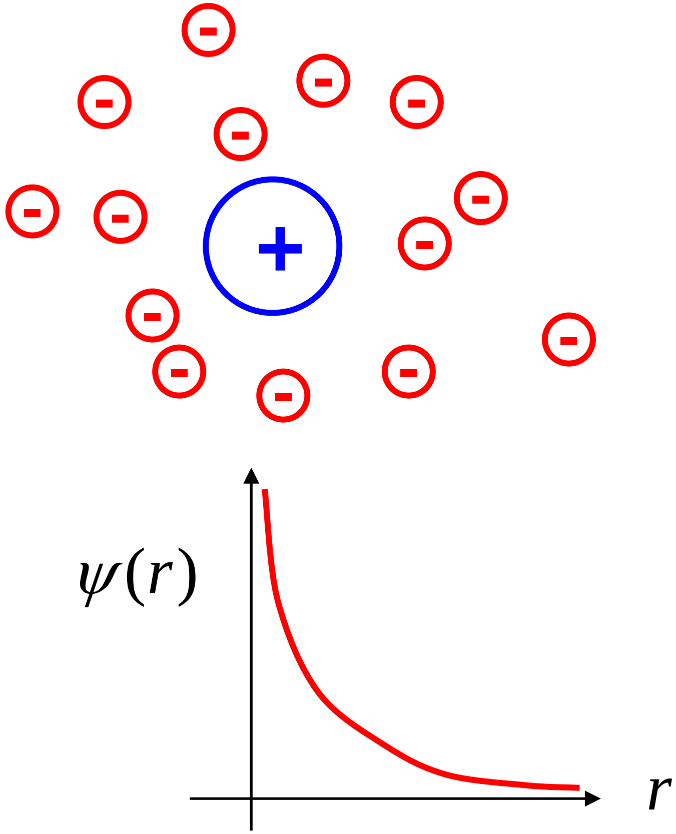
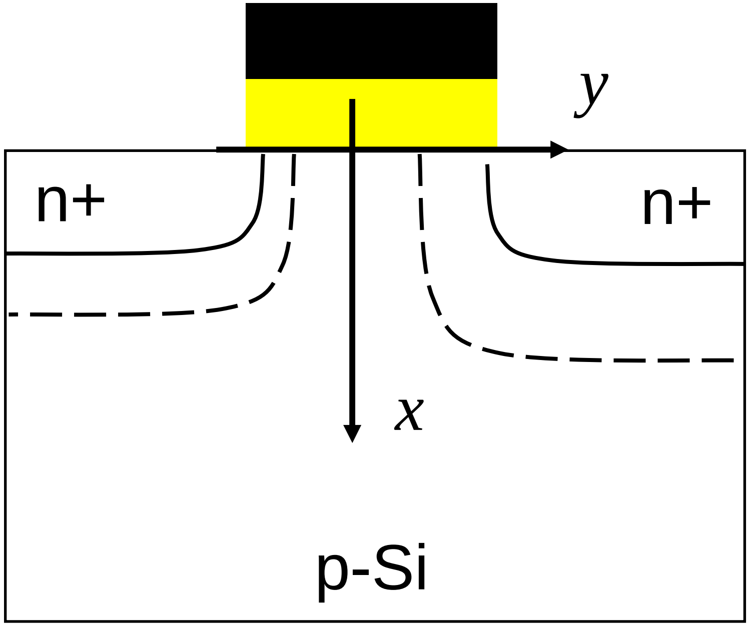
screening by free carriers



$$\psi(r) = \frac{q}{4\pi\varepsilon_{Si}\, r} e^{-r/L_D}$$

$$L_D = \sqrt{\frac{\varepsilon_{Si} k_B T}{q^2 N_D}}$$

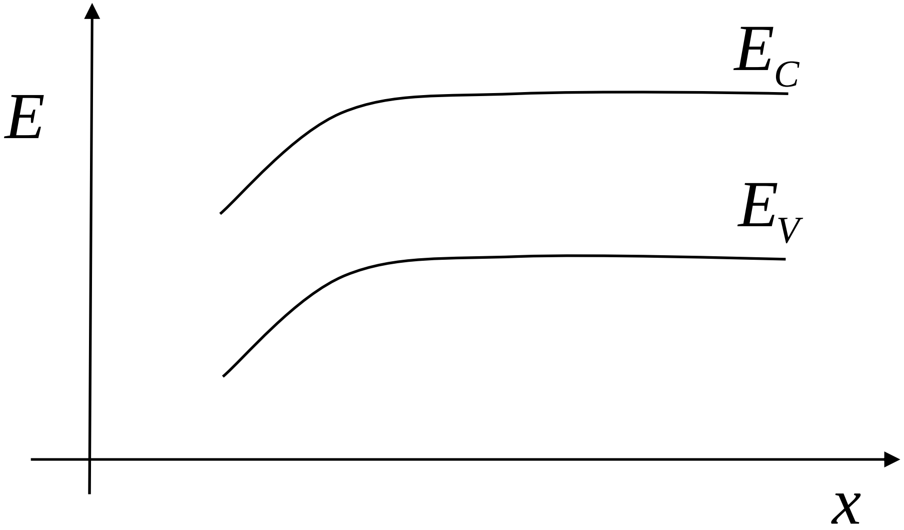
geometric screening



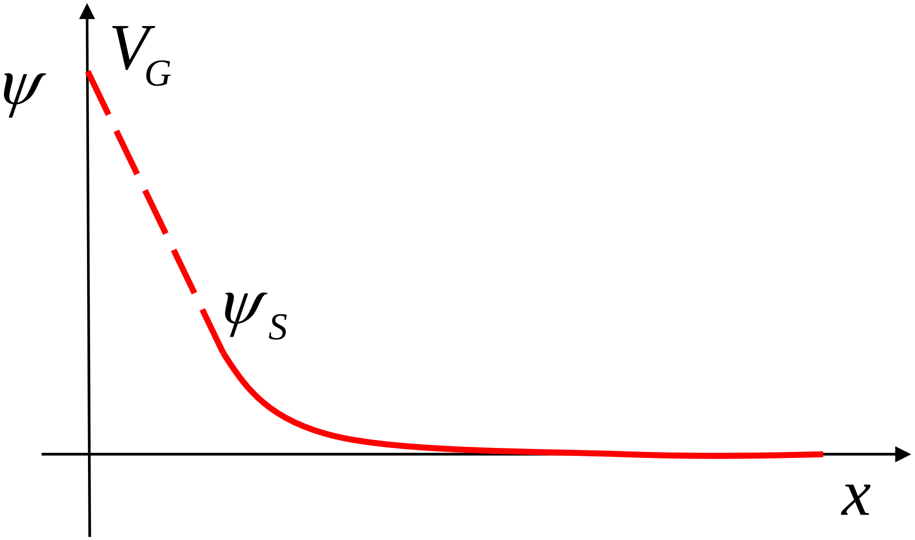
$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}} \quad (\text{below} V_T)$$

'convert' this to a 1D equation

recall 1D



$$\frac{\partial^2\psi}{\partial x^2} = \frac{qN_A}{\varepsilon_{Si}}$$



$$\frac{\partial^2\psi}{\partial x^2} \approx \frac{\left(V_G - \psi_S\right)}{\Lambda^2}$$

$$\Lambda = ?$$

geometric screening length

in 1D:

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{qN_A}{\varepsilon_{Si}} \qquad (1)$$

we will write this as:

$$\frac{\partial^2 \psi}{\partial x^2} \approx \frac{\left(V_G - \psi_S\right)}{\Lambda^2} = \frac{qN_A}{\varepsilon_{Si}} \qquad (2)$$

the solution to the 1D Poisson equation gives:

$$V_G = \psi_S - Q_S / C_{ox} = \psi_S + qN_A W_{DM} / C_{ox} \qquad (3)$$

use (3) in (2) to find Λ

geometric screening length (ii)

$$\Lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{OX}} W_{DM} t_{OX}}$$

$$\boxed{\frac{\partial^2 \psi}{\partial y^2} + \frac{(V_G - \psi_S)}{\Lambda^2} = \frac{qN_A}{\varepsilon_{Si}}}$$

when $\frac{\partial^2 \psi}{\partial y^2} << \frac{\partial^2 \psi}{\partial y^2}$

we get the correct 1D result

How do we interpret Λ?

geometric screening length (iii)

$$\frac{\partial^2 \psi}{\partial y^2} + \frac{(V_G - \psi_S)}{\Lambda^2} = \frac{qN_A}{\varepsilon_{Si}}$$

$$\phi = \psi_S - V_G + \frac{qN_A}{\varepsilon_{Si}} \Lambda^2$$

$$\boxed{\frac{d^2 \phi}{dy^2} - \frac{\phi}{\Lambda^2} = 0}$$

source

$$\phi = \phi(0)$$

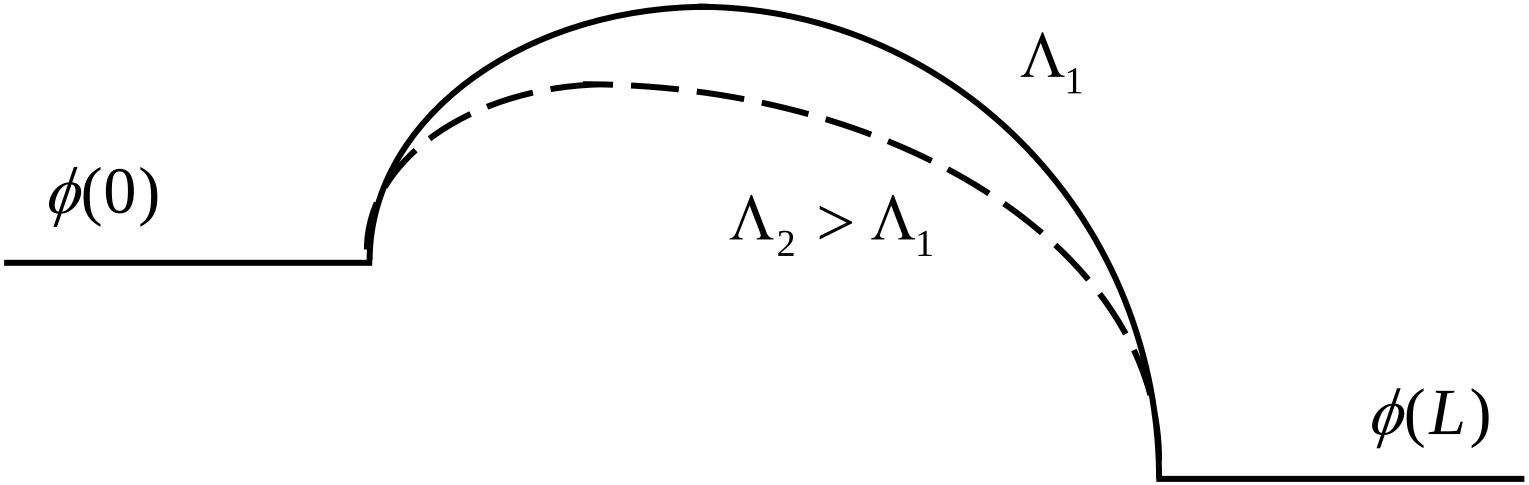
drain

$$\phi = \phi(L)$$

geometric screening length (iv)

$L >> \Lambda$ (long channel)

$L \approx (1.5 - 2)\Lambda$ (typical)



$$\phi(y) = A\cosh(y/\Lambda) + B\sinh(y/\Lambda)$$

analytical solutions

$$\Delta V_T \approx 8(m-1)\sqrt{V_{bi}\left(V_{bi}+V_{DS}\right)}e^{-L/\lambda}$$

$$\left(x_j \geq W_{DM}\right)$$

$$S \approx \frac{2.3mk_BT}{q}\left(1+\frac{11t_{ox}}{W_{DM}}e^{-L/\lambda}\right)$$

$$\lambda = 2mW_{DM}/\pi$$

See Taur and Ning, Appendix 6

geometric screeing length vs. device geometry

$$\Lambda_{BULK} \approx \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{OX}} W_{DM} t_{OX}}$$

$$\Lambda_{SOI} \approx \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{OX}} t_{Si} t_{OX}} < \Lambda_{BULK}$$

$$\Lambda_{DG\ SOI} \approx \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{OX}} t_{Si} t_{OX}} < \Lambda_{SOI}$$

$$\Lambda_{CYL} < \Lambda_{DG\ SOI}$$

see:
D.J. Frank, Y. Taur, and H.S.P. Wong, ‘Generalized scale length for 2D Effects in MOSFETs,” *IEEE EDL*, **19**, p. 385, 1998.

The objective in MOSFET design is to make L > Λ

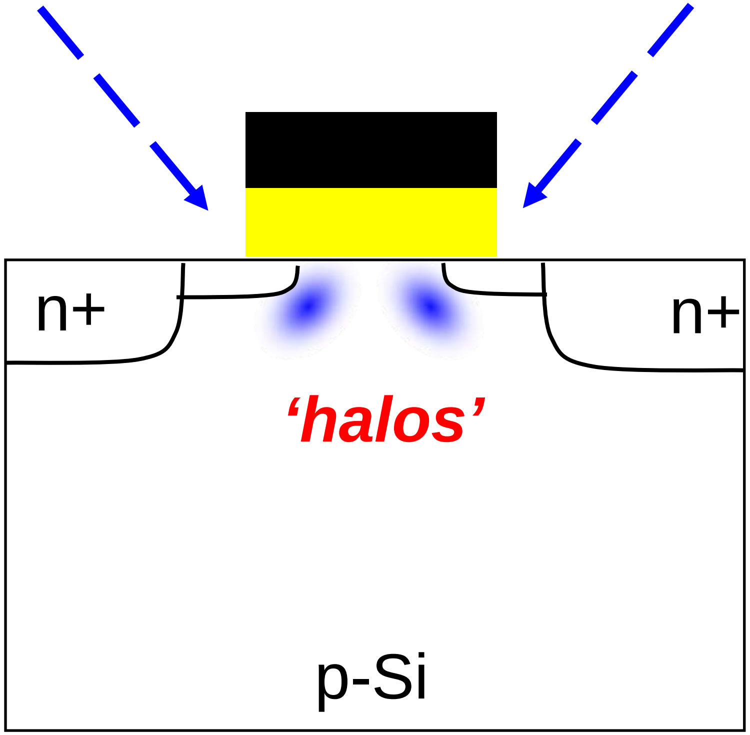
$$L \approx \left(1.5 - 2\right)\Lambda \quad \text{(typical)}$$

outline

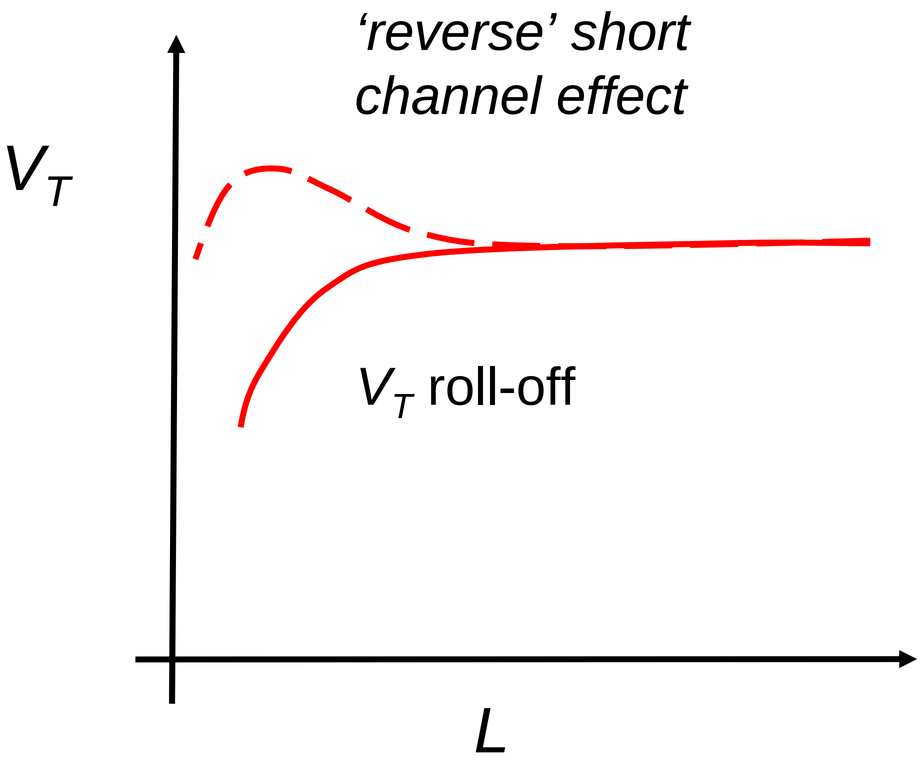
1) Consequences of 2D electrostatics
2) 2D Poisson equation
3) Charge sharing model
4) Barrier lowering
5) 2D capacitor model
6) Geometric screening length
7) Discussion
8) Summary

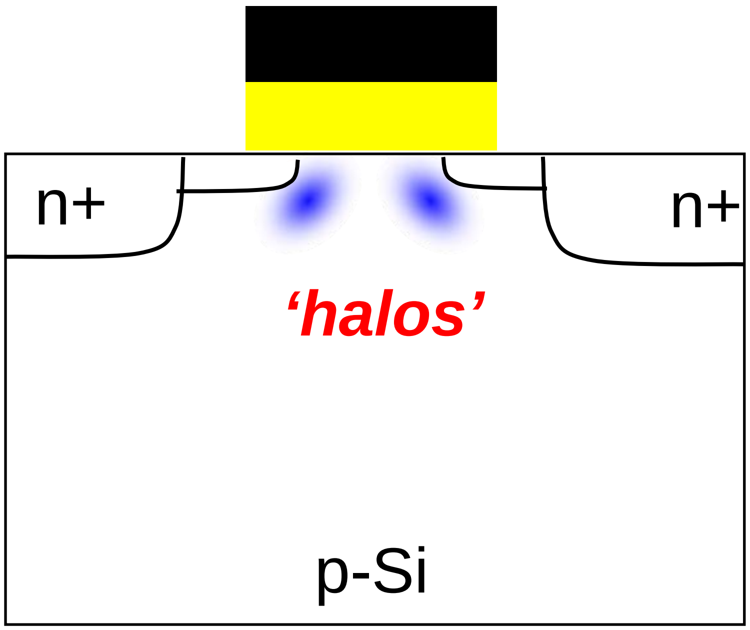
controlling 2D electrostatics

1) $t_{ox} << L$
2) shallow x_j
3) thin W_{DM}
4) non-uniform doping



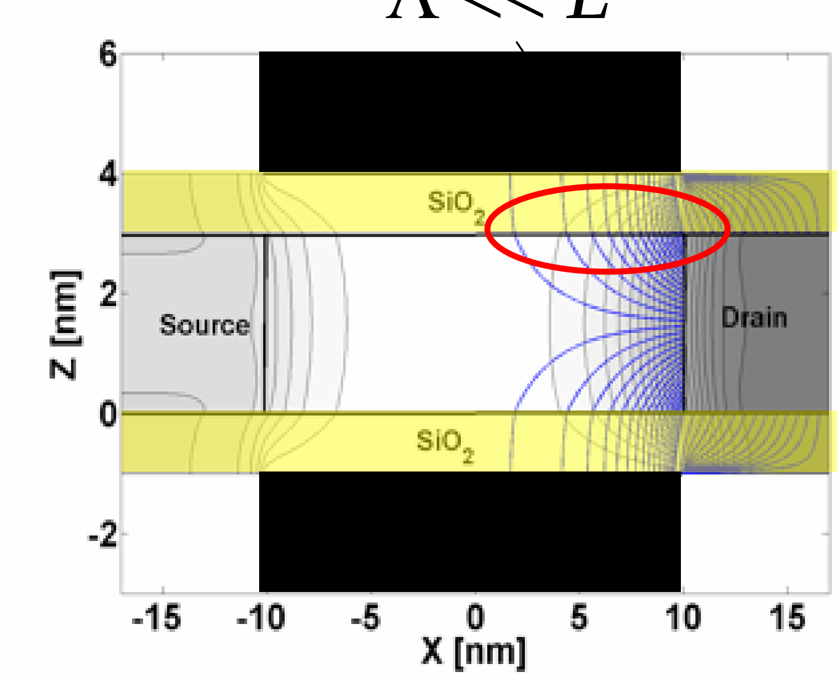
reverse short channel effect





double gate transistors

$\Lambda << L$



nanoMOS simulations by Himadri Pal and Raseong Kim (Purdue)

geometric screening length

Λ

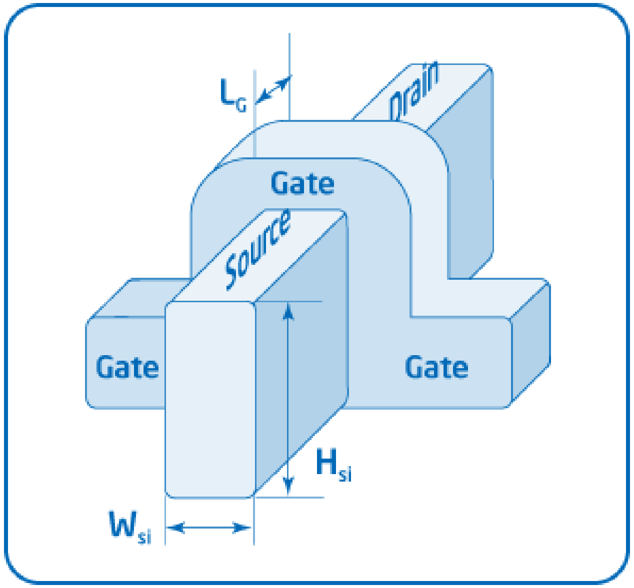
channel length scaling

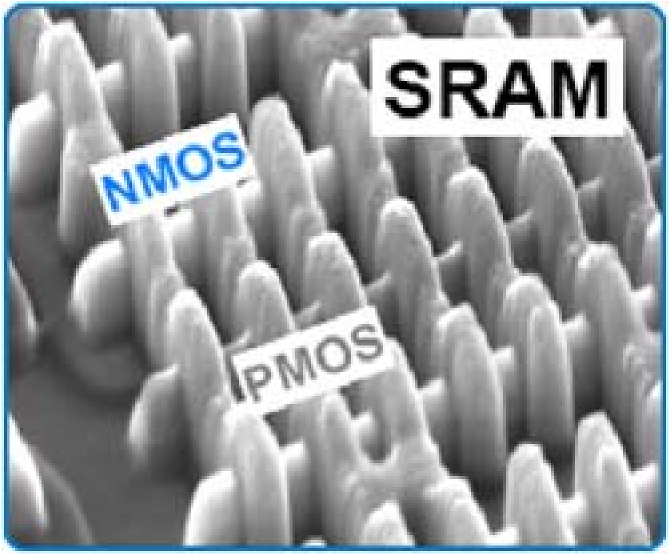
$L >> \Lambda$

$\Lambda_{DG\ SOI} < \Lambda_{BULK}$

nonplanar MOSFETS

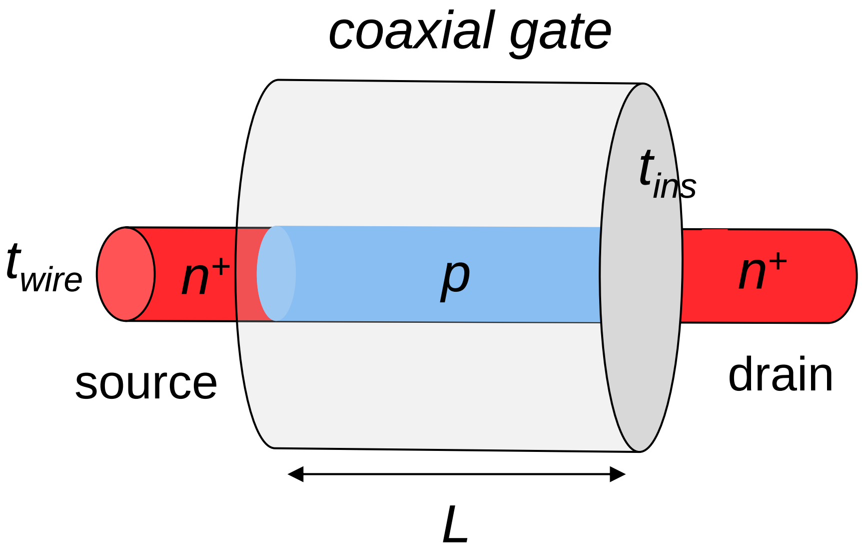
Intel Tri-Gate





J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, and R. Chau. “Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates, and Strain Engineering,” VLSI Technology Digest, June 2006, pp. 62-63.

nanowire transistors



geometric screening length

$$\Lambda$$

channel length scaling

$$L >> \Lambda$$

$$\Lambda_{CYL} < \Lambda_{DG\ SOI} < \Lambda_{BULK}$$

C. P. Auth and J.D. Plummer, "Scaling Theory for Cylindrical, Full-Depleted, Surrounding Gate MOSFET's," *IEEE EDL*, **18**, p. 74, 1997.

outline

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summary

1) 2D electrostatics is a critical issue in device scaling

2) Understanding 2D electrostatics is essential for transistor designers