EE-612: Lecture 12: 2D Electrostatics

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outline

1) Consequences of 2D electrostatics
2) 2D Poisson equation
3) Charge sharing model
4) Barrier lowering
5) 2D capacitor model
6) Geometric screening length
7) Discussion
8) Summary
\( I_D \) vs. \( V_{DS} \) (long channel)

1) square law

\[
I_D = \frac{W}{2L} \mu_{\text{eff}} C_{\text{ox}} \left( V_{GS} - V_T \right)^2 \frac{1}{m}
\]

2) low output conductance

\[
g_d = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS}}
\]
$I_D$ vs. $V_{DS}$ (short channel)

1) linear with $V_{GS}$

$$I_D = W \nu_{sat} C_{ox} (V_{GS} - V_T)$$

2) high output conductance

$$g_d = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS}}$$

see Taur and Ning, pp. 154-158
channel length modulation

\[ I_D = \mu_{\text{eff}} C_{ox} \frac{W}{2L'} (V_{GS} - V_T)^2 \]

\[ V_{GS} > V_T \]
\[ V_{DS} > V_{GS} - V_T \]

**pinch-off region:**
1) high lateral electric field \( E_y >> E_x \)
2) small carrier density
3) under control of drain, not gate (GCA does not apply)

\[ L' = L - \Delta L < L \]
$V_T$ roll-off

\[ V_T = V_{FB} + 2\psi_B + \sqrt{2q\varepsilon_{Si} N_A (2\psi_B) / C_{ox}} \]

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DIBL

\[ (V_{GS} - V_T)^\alpha \]

\[ e^{(V_{GS} - V_T)/mk_B T} \]

\[ V_{DS} = 1.1 \text{V} \]

\[ V_{DS} = 0.05 \text{V} \]

“Drain-Induced Barrier Lowering” (DIBL) mV/V
stronger short channel effects

\[ (V_{GS} - V_T)^\alpha \]

\[ e^{(V_{GS} - V_T) / m_BT} \]

\[ V_{DS} = 1.1V \]
\[ V_{DS} = 0.05V \]

\[ S(V_{DS} = 1.1V) > S(V_{DS} = 0.05V) \]
severe short channel effects

\[ V_{DS} = 1.1V \]
\[ V_{DS} = 0.05V \]

\[ \log I_D \]
\[ e^{(V_{GS} - V_T)/mK_B T} \]

Current weakly dependent on \( V_{GS} \)

‘punch through’
punchthrough

\[ N_A(\text{min}) : \text{punch through} \]

\[ W_S + W_D < L \]
short channel effects

1) $I_D$ linear not quadratic with gate voltage
2) high output conductance
3) threshold voltage roll-off
4) increased DIBL
5) increased $S$
6) punchthrough
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2D Poisson equation

1) MOS Capacitor:
\[
\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho}{\varepsilon_{Si}} = \frac{qN_A}{\varepsilon_{Si}} \quad \text{(below } V_T \text{)}
\]

2) MOSFET:
\[
\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}} \quad \text{(below } V_T \text{)}
\]
2D Poisson equation (ii)

1) Long channel MOSFET below threshold:

\[
\frac{\partial^2 \psi}{\partial x^2} \gg \frac{\partial^2 \psi}{\partial y^2}
\]

gradual channel approximation (GCA):

\[
Q_I(y) = -C_G \left[ V_G - V_T - mV(y) \right]
\]
2D Poisson equation (iii)

1) Short channel MOSFET below threshold:

\[
\frac{\partial^2 \psi}{\partial x^2} = \frac{qN_A}{\varepsilon_{Si}} \frac{\partial^2 \psi}{\partial y^2}
\]

\[
\frac{\partial^2 \psi}{\partial x^2} = \frac{qN_A}{\varepsilon_{Si}} < 0
\]

\[
N_A^{eff} < N_A
\]

\[
V_T < V_T^{(long \ channel)}
\]

explanys $V_T$ roll-off

Increasing $V_{DS}$

$\frac{\partial^2 E_C}{\partial y^2} < 0$

$y \ (nm) \ ---\rightarrow$

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2D potential contours

\[ \psi = 1.0 \]

\[ \psi = 0.5 \]

\[ \psi = 0.4 \]

\[ \psi = 0.3 \]

\[ \psi = 0.2 \]

\[ \psi = 0.1 \]

\[ \psi = 0 \]

\[ \psi_s = 1V \]

\[ \psi = 0V \]

\[ E_C \]

\[ E_F \]

\[ E_V \]

\[ E(x) \]

p-Si
2D potential contours

\[ \psi = V_{bi} \]

\[ \psi = 0 \]

p-Si

n+
2D potential contours (long channel)

like 1D MOS capacitor
2D potential contours (short channel)

(See Fig. 3.18 of Taur and Ning)
field lines

\[ \psi = V_{bi} \]

\[ \psi = 0 \]

\[ \psi = V_{bi} \]

p-Si

n+ n+

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field lines (bulk)
field lines (SOI)
field lines (SOI)

‘gate all around’

FINFET

tri-gate
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charge sharing model

\[ \bar{Q}_D = (W W_{DM}) q N_A \]
charge sharing model (ii)
charge sharing model (ii)

\[ \bar{Q}_D' = W \left( \frac{L + L'}{2} \right) W_{DM} qN_A \]
charge sharing model (iii)

\[ V_T = V_{FB} + 2\psi_B - \gamma \frac{Q_D}{C_{OX}} < V_T \text{ (long channel)} \]

\[ \gamma = \frac{L + L'}{2L} = 1 - \frac{x_j}{L} \left( \sqrt{1 + \frac{2W_{DM}}{x_j}} - 1 \right) \]

(prob. 3.6, Taur and Ning)

for \( \gamma \sim 1 \), need:

\[ \begin{cases} 
  x_j << L \\
  W_{DM} << x_j 
\end{cases} \]

increase channel doping

\[ \text{S/D extensions} \]

\[ \text{p-Si} \]
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barrier lowering

$E_C(y)$

$q(V_{bi} - \psi_S)$

gate controls barrier height

drain depletion layer expands

$I_D \sim e^{-E_B/k_bT}$

current does not change

low $V_{DS}$

high $V_{DS}$

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barrier lowering (ii)

\[ \log I_D = e^{(V_{GS} - V_T)/mk_BT} \]

- \( V_{DS} = 1.1V \)
- \( V_{DS} = 0.05V \)

no DIBL
barrier lowering (iii)

\[ I_D \sim e^{-E_B/k_bT} \]

\[ \Delta I_D = e^{\Delta E_B/k_bT} \]

\[ q(V_{bi} - \psi_S) \]

\[ \Delta E_B \]

\[ y \]

\[ E_C(y) \]

\[ \text{drain-induced barrier lowering} \]

low \( V_{DS} \)

high \( V_{DS} \)
barrier lowering (iv)

\[ V_{DS} = 1.1V \]
\[ V_{DS} = 0.05V \]

\[ \Delta I_D = e^{\Delta E_B / k_b T} \]
punchthrough

\[ I_D \sim e^{-E_B/k_B T} \]

\[ E_C(y) \]

\[ q(V_{bi} - \psi_S) \]

\[ y \]

low \( V_{DS} \)

decreasing \( N_A \)

high \( V_{DS} \)
punchthrough (ii)

\[ I_D \sim e^{-E_B/k_B T} \]

\[ E_C(y) \]

\[ q(V_{bi} - \psi_S) \]

low \( V_{DS} \)

increasing \( V_{DS} \)
punchthrough (iii)

surface punchthrough  

bulk punchthrough  

\[ \text{p-Si} \]

\[ \text{n}^+ \quad \text{n}^+ \]

\[ \text{p-Si} \]

\[ \text{n}^+ \quad \text{n}^+ \]
punchthrough (iv)

\[ V_{DS} = 0.05\text{V} \]

\[ V_{DS} = 1.1\text{V} \]

\[ \log I_D \]

\[ e^{(V_{GS} - V_T)/mk_B T} \]

\[ V_{GS} \]

\[ I_D \]

\[ V_{DS} \]
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2D capacitor model
2D capacitor model \((V = 0)\)

\[
\psi_S = \frac{Q}{C_\Sigma}
\]

\[
C_\Sigma = C_{GB} + C_{SB} + C_{DB} + C_D
\]
2D capacitor model \((Q = 0)\)

\[
V_S = V_D = 0
\]

\[
\psi_S = \frac{C_{GB}}{C_{\Sigma}} V_G
\]

\[
C_{ SB} + C_{DB} + C_D
\]
2D capacitor model (general solution)

\[ \psi_S = \frac{C_{GB}}{C_{\Sigma}} V_G + \frac{C_{SB}}{C_{\Sigma}} V_S + \frac{C_{DB}}{C_{\Sigma}} V_D + \frac{Q}{C_{\Sigma}} \]

\[ C_{\Sigma} = C_{GB} + C_{SB} + C_{DB} + C_D \]

\[ C_{GB} = C_{ox} WL \quad C_D = \text{depletion layer capacitance} \]

Recall:

\[ V_G = \psi_S - \frac{Q}{C_{ox}} \]
2D capacitor model \((V_S = Q = 0)\)

\[
\psi_S = \frac{C_{GB}}{C_\Sigma} V_G + \frac{C_{DB}}{C_\Sigma} V_D
\]

\[
\frac{\partial \psi_S}{\partial V_G} = \frac{C_{GB}}{C_\Sigma} \quad \frac{\partial \psi_S}{\partial V_D} = \frac{C_{DB}}{C_\Sigma}
\]

\[
\frac{\partial \psi_S}{\partial V_G} \gg \frac{\partial \psi_S}{\partial V_D} \Rightarrow C_{GB} \gg C_{DB}
\]

need \(t_{ox} \ll L\)
2D capacitor model

\[
\psi_s = \frac{C_{GB}}{C_\Sigma} V_G + \frac{C_{DB}}{C_\Sigma} V_D \quad \left( V_s = Q = 0 \quad C_\Sigma = C_{DB} + C_D \right)
\]

\[
I_D \propto e^{q\psi_s/k_B T} = e^{qV_{GS}/mk_B T}
\]

\[
m = C_\Sigma / C_{GB}
\]

\[
m = \left( C_{GB} + C_{DB} + C_D \right) / C_{GB}
\]

\[
= \left[ 1 + \left( C_{DB} + C_D \right) / C_{GB} \right]
\]

2D electrostatics: \( C_{DB} \) not negligible \( S \) increases.
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screening by free carriers

\[ \psi(r) = \frac{q}{4\pi \varepsilon_{Si} r} e^{-r/L_D} \]

\[ L_D = \sqrt{\frac{\varepsilon_{Si} k_B T}{q^2 N_D}} \]
geometric screening

\[ \frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}} \quad \text{(below } V_T \text{)} \]

‘convert’ this to a 1D equation
recall 1D

\[
\frac{\partial^2 \psi}{\partial x^2} = \frac{qN_A}{\varepsilon_{Si}}
\]

\[
\frac{\partial^2 \psi}{\partial x^2} \approx \frac{(V_G - \psi_S)}{\Lambda^2}
\]

\[\Lambda = ?\]
geometric screening length

in 1D:

\[
\frac{\partial^2 \psi}{\partial x^2} = \frac{qN_A}{\varepsilon_{Si}}
\]  

we will write this as:

\[
\frac{\partial^2 \psi}{\partial x^2} \approx \left( V_G - \psi_S \right) \frac{\Lambda^2}{\varepsilon_{Si}} = \frac{qN_A}{\varepsilon_{Si}}
\]  

the solution to the 1D Poisson equation gives:

\[
V_G = \psi_S - \frac{Q_S}{C_{ox}} = \psi_S + qN_A W_{DM} / C_{ox}
\]

use (3) in (2) to find \( \Lambda \)
The geometric screening length ($\Lambda$) is given by:

$$\Lambda = \sqrt{\frac{\varepsilon_{Si} W_{DM} t_{OX}}{\varepsilon_{OX}}}$$

where $\varepsilon_{Si}$ is the permittivity of silicon, $W_{DM}$ is the effective width, $t_{OX}$ is the oxide thickness, $\varepsilon_{OX}$ is the permittivity of the oxide, $V_G$ is the gate voltage, $\psi_S$ is the surface potential, $\partial^2 \psi / \partial y^2$ is the second derivative of the potential with respect to position, $qN_A$ is the charge density, and $\varepsilon_{Si}$ is the permittivity of silicon.

The equation to obtain the correct 1D result is:

$$\frac{\partial^2 \psi}{\partial y^2} + \frac{(V_G - \psi_S)}{\Lambda^2} = \frac{qN_A}{\varepsilon_{Si}}$$

when

$$\frac{\partial^2 \psi}{\partial y^2} \ll \frac{\partial^2 \psi}{\partial y^2}$$

we get the correct 1D result.

How do we interpret $\Lambda$?
geometric screening length (iii)

\[ \frac{\partial^2 \psi}{\partial y^2} + \left( \frac{V_G - \psi_S}{\Lambda^2} \right) = \frac{qN_A}{\varepsilon_{Si}} \]

\[ \phi = \psi_S - V_G + \frac{qN_A}{\varepsilon_{Si}} \Lambda^2 \]

\[ \frac{d^2 \phi}{dy^2} - \frac{\phi}{\Lambda^2} = 0 \]

source
\[ \phi = \phi(0) \]

drain
\[ \phi = \phi(L) \]
geometric screening length (iv)

\[ \phi(y) = A \cosh(y / \Lambda) + B \sinh(y / \Lambda) \]

\[ L \gg \Lambda \quad \text{(long channel)} \]

\[ L \approx (1.5 - 2)\Lambda \quad \text{(typical)} \]
analytical solutions

\[ \Delta V_T \approx 8(m - 1) \sqrt{V_{bi} (V_{bi} + V_{DS})} e^{-L/\lambda} \]

\[ S \approx \frac{2.3mk_BT}{q} \left( 1 + \frac{11t_{ox}}{W_{DM}} e^{-L/\lambda} \right) \]

\[ \lambda = 2mW_{DM}/\pi \]

See Taur and Ning, Appendix 6
geometric screening length vs. device geometry

\[ \Lambda_{BULK} \approx \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{OX}}} W_{DM} t_{OX} \]

\[ \Lambda_{SOI} \approx \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{OX}}} t_{Si} t_{OX} < \Lambda_{BULK} \]

\[ \Lambda_{DG SOI} \approx \sqrt{\frac{\varepsilon_{Si}}{2 \varepsilon_{OX}}} t_{Si} t_{OX} < \Lambda_{SOI} \]

\[ \Lambda_{CYL} < \Lambda_{DG SOI} \]

see:

The objective in MOSFET design is to make \( L > \Lambda \)

\( L \approx (1.5 - 2)\Lambda \) (typical)
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controlling 2D electrostatics

1) \( t_{ox} \ll L \)
2) shallow \( x_j \)
3) thin \( W_{DM} \)
4) non-uniform doping

n+ \( \rightarrow \) \( \rightarrow \) n+

p-Si

‘halos’
reverse short channel effect

\[ V_T \]

'\text{reverse}' short channel effect

\[ V_T \text{ roll-off} \]

'n+ n+ n+

'halos'

p-Si
double gate transistors

\[ \Lambda << L \]

geometric screening length \[ \Lambda \]

channel length scaling \[ L >> \Lambda \]

\[ \Lambda_{DG\, SOI} < \Lambda_{BULK} \]

nanoMOS simulations by Himadri Pal and Raseong Kim (Purdue)
nonplanar MOSFETS

Intel Tri-Gate

nanowire transistors

\[ \Lambda \]

\[ L \gg \Lambda \]

\[ \Lambda_{CYL} < \Lambda_{DG\ SOI} < \Lambda_{BULK} \]

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summary

1) 2D electrostatics is a critical issue in device scaling

2) Understanding 2D electrostatics is essential for transistor designers