EE-612:
Lecture 15:
Series Resistance
(and effective channel length)

Mark Lundstrom
Electrical and Computer Engineering
Purdue University
West Lafayette, IN USA

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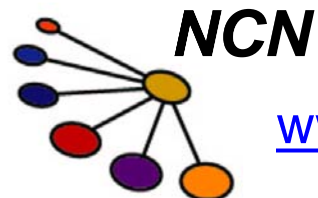

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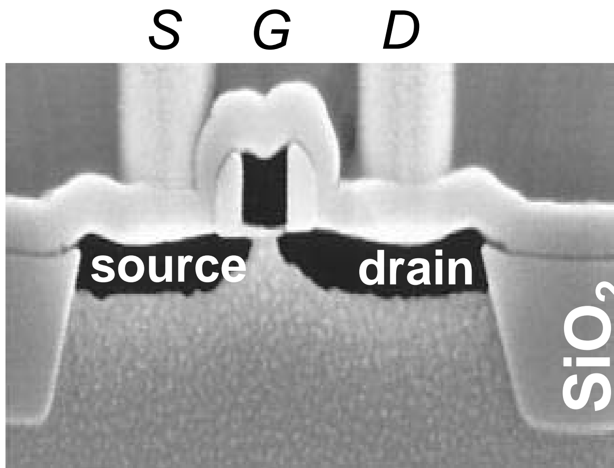
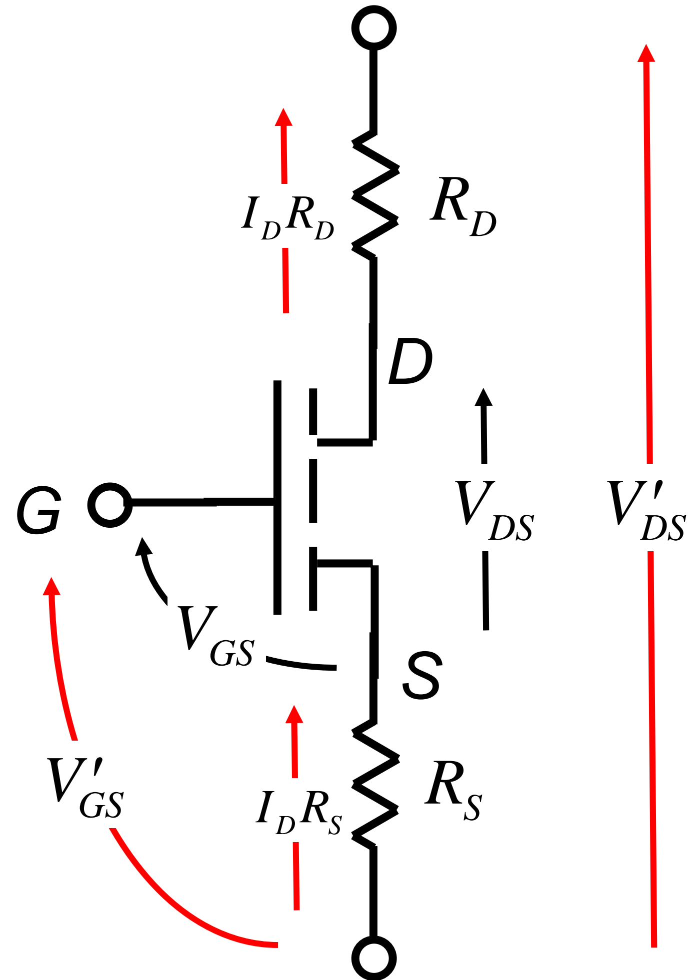
outline

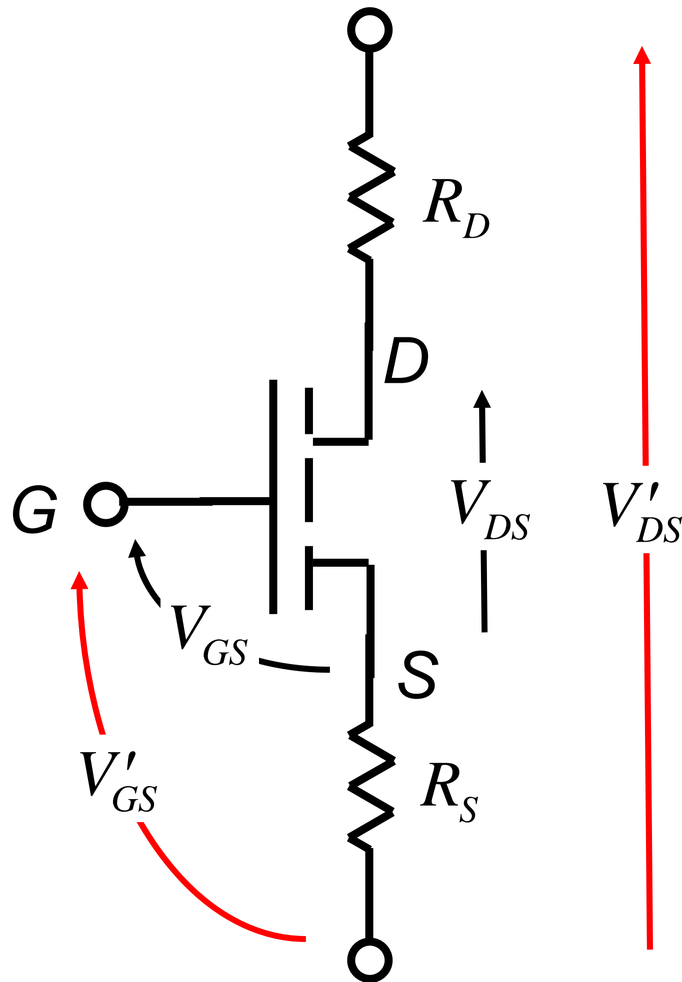
1) Effect on I-V
2) Series resistance components
3) Metal-semiconductor resistance
4) Other series resistance components
5) Discussion
6) Effective Channel Length
7) Summary

series resistance



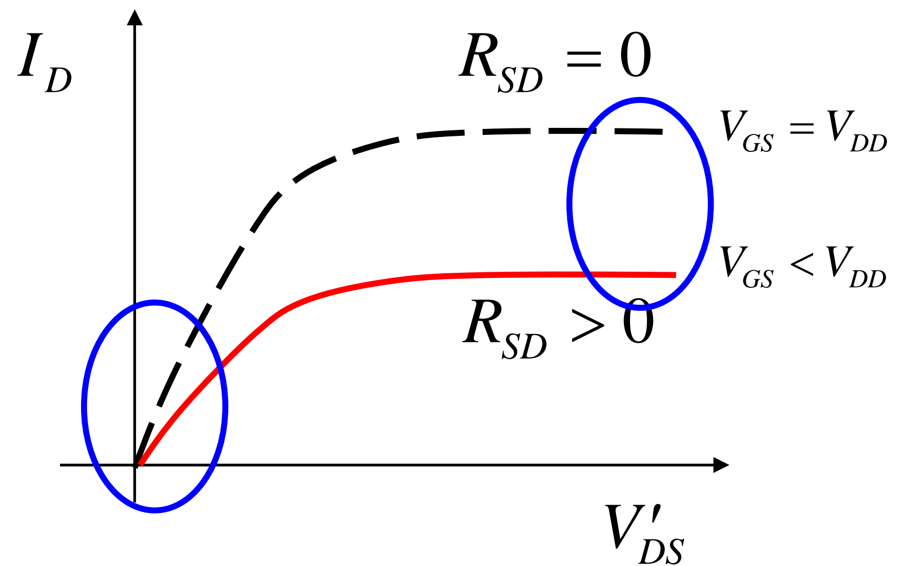


series resistance (ii)



$$V_{GS} = V'_{GS} - I_D R_S$$

$$V_{DS} = V'_{DS} - I_D \left(R_S + R_D\right)$$



series resistance (small V_{DS})

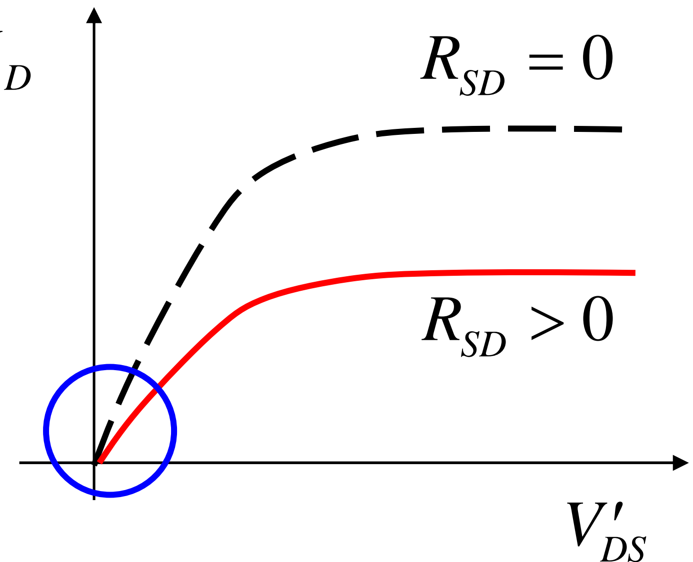
$$\left.\begin{aligned} V_{GS} &= V'_{GS} - I_D R_S \\ V_{DS} &= V'_{DS} - I_D\left(R_S + R_D\right) \end{aligned}\right\}$$

$$I_D^i = \frac{W}{L}\mu_{eff} C_G \left(V_{GS} - V_T\right) V_{DS} = V_{DS} / R_{CH}$$

$$I_D = V'_{DS} / \left(R_{CH} + R_S + R_D\right)$$

$$\Delta I_D = I_D^i - I_D = V'_{DS}\left(\frac{1}{R_{CH}} - \frac{1}{R_{CH} + R_{SD}}\right)$$

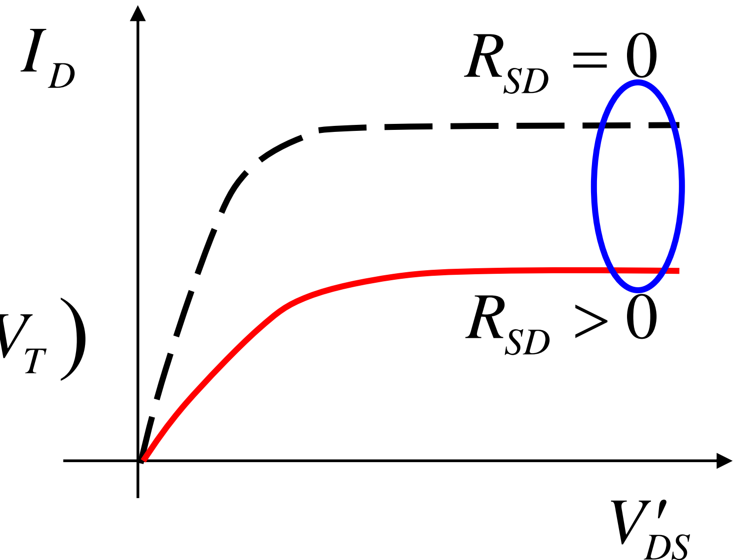
$$= \frac{V'_{DS}}{R_{CH}}\left(\frac{R_{SD}}{R_{CH} + R_{SD}}\right)$$



$$\frac{\Delta I_D}{I_D^i} = \left(\frac{R_{SD}}{R_{TOT}}\right)$$

series resistance (large V_{DS})

$$
\left.\begin{aligned}
V_{GS} &= V'_{GS} - I_D R_S \\
V_{DS} &= V'_{DS} - I_D \left(R_S + R_D\right)
\end{aligned}\right\}
$$



$$I_D^i = W C_G \upsilon_{SAT} \left(V_{GS} - V_T\right) = G_0 \left(V_{GS} - V_T\right)$$

$$I_D = G_0 \left(V'_{GS} - I_D R_S - V_T\right)$$

$$I_D \left(1 + G_0 R_S\right) = G_0 \left(V'_{GS} - V_T\right) = I_D^i$$

$$I_D = \frac{I_D^i}{\left(1 + G_0 R_S\right)}$$

series resistance (large V_{DS})

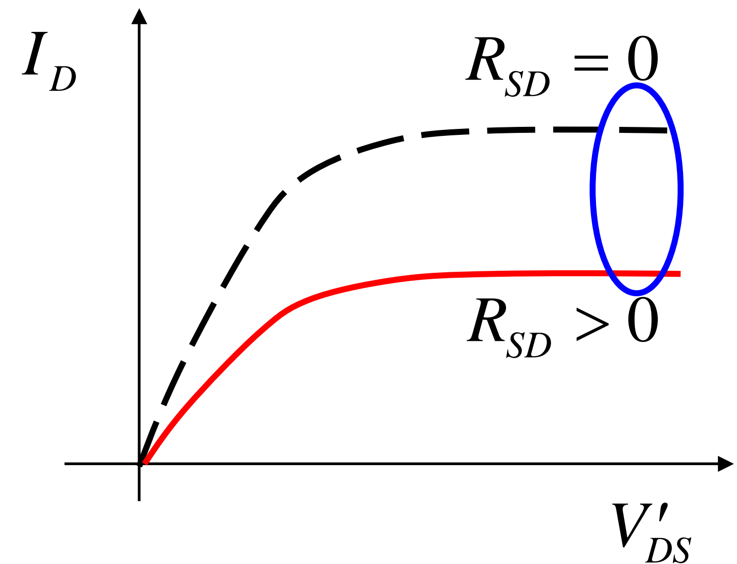
$$I_D = \frac{I_D^i}{\left(1 + G_0 R_S\right)}$$

$$\Delta I_D = I_D^i - \frac{I_D^i}{\left(1 + G_0 R_S\right)}$$

$$\frac{\Delta I_D}{I_D^i} = \frac{G_0 R_S}{\left(1 + G_0 R_S\right)} = \frac{R_S}{\left(1 / G_0 + R_S\right)}$$

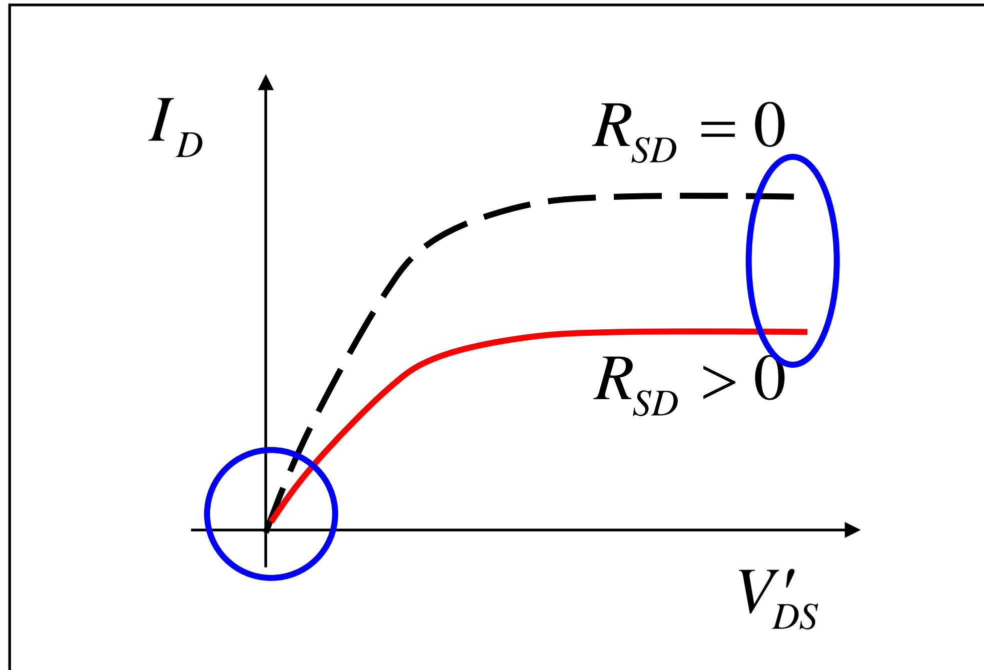
$$I_D^i = G_0 \left(V_{GS} - V_T\right)$$

$$G_0 \approx I_{ON} / V_{DD} = 1 / R_{ON}$$



$$\frac{\Delta I_D}{I_D^i} \approx \frac{R_S}{\left(R_{ON} + R_S\right)} = \frac{R_S}{R_{TOT}}$$

recap



$$\frac{\Delta I_D}{I_D^i} = \left(\frac{R_{SD}}{R_{TOT}} \right)$$

$$\frac{\Delta I_D}{I_D^i} \approx \frac{R_S}{\left(R_{ON} + R_S\right)} = \frac{R_S}{R_{TOT}}$$

$$R_{TOT} \approx R_S + R_D + R_{CH}$$

$$R_{ON} \approx V_{DD} / I_{ON}$$

maximum series resistance

$$\frac{\Delta I_D}{I_D^i} \approx \frac{R_S}{\left(R_{ON} + R_S\right)} < 0.1$$

From ITRS 2007 Ed.

$$I_{ON} = 1513\ \mu\text{A} / \mu\text{m} \qquad V_{DD} = 1\ \text{V}$$

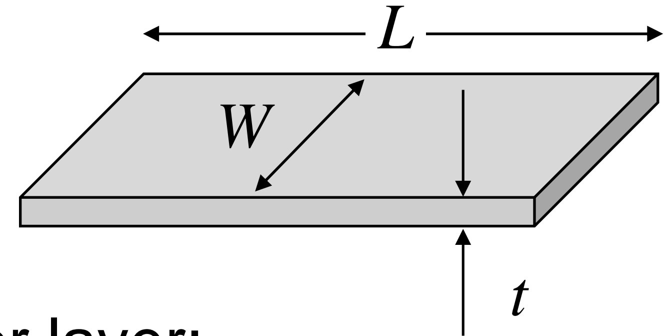
$$R_{ON} = 654\ \ \Omega - \mu\text{m}$$

$$\Rightarrow R_S < 73\ \ \Omega - \mu\text{m}$$

$$R_{SD} = R_S + R_D < 146\ \ \Omega - \mu\text{m} \quad \left(200\ \Omega - \mu\text{m}\right)$$

some terminology to keep straight

1) resistivity of a semiconductor:



$$\rho = \frac{1}{nq\mu_n} \ \Omega\text{-cm} \qquad R = \rho \frac{L}{A} = \rho \frac{L}{Wt} \ \Omega$$

2) sheet resistance of a semiconductor layer:

$$\rho_S = \frac{\rho}{t} \ \Omega/\text{W} \qquad R = \rho_S \frac{L}{W} \ \Omega$$

3) interfacial contact resistivity:

$$\rho_C \ \ \Omega\text{ - cm}^2$$

outline

1) Effect on I-V

2) Series resistance components

3) Metal-semiconductor resistance

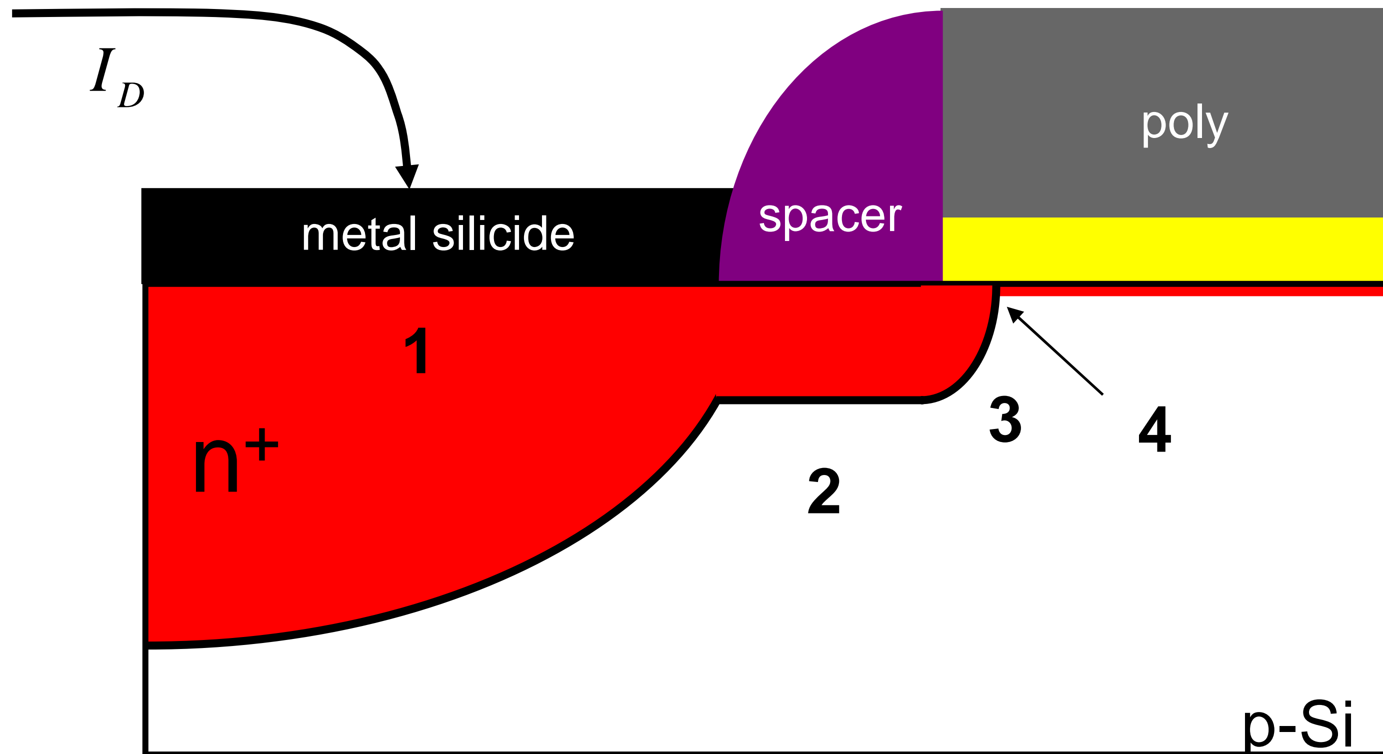
4) Other series resistance components

5) Discussion

6) Effective channel length

7) Summary

physical origin of R_{SD}



1) metal-semiconductor contact resistance
2) extension resistance
3) tip resistance
4) spreading resistance

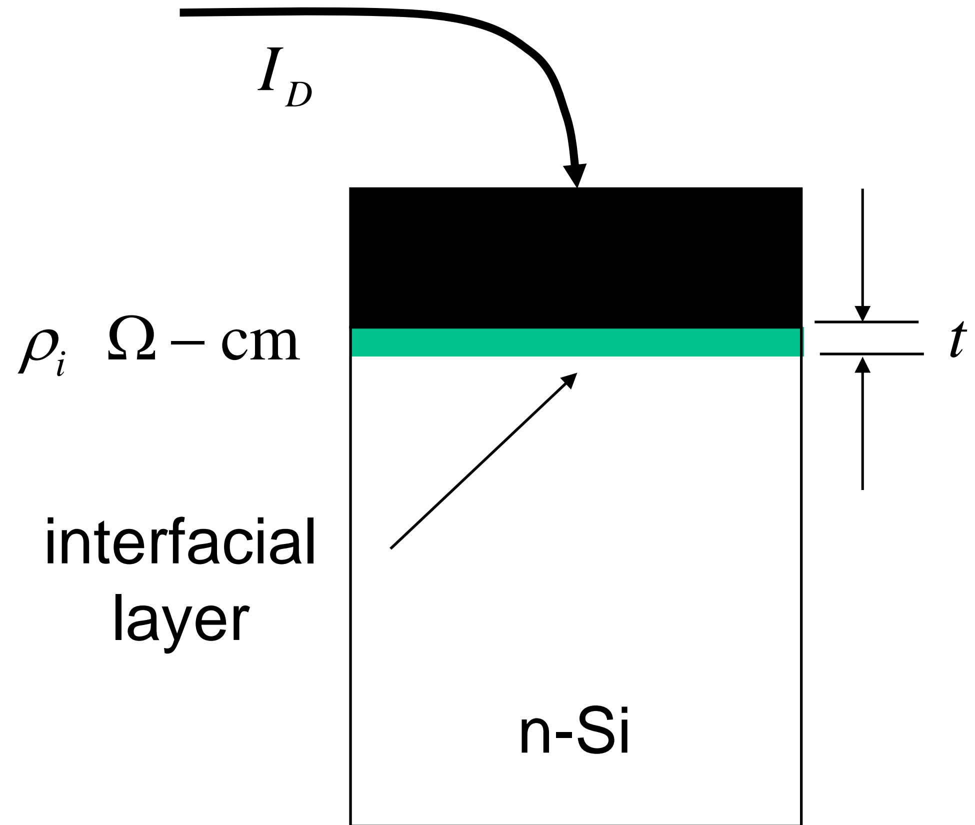
outline

1) Effect on I-V
2) Series resistance components
3) **Metal-semiconductor resistance**
4) Other series resistance components
5) A look at the ITRS
6) Effective channel length
7) Summary

metal-semiconductor contact resistance

metal contact

Area = A_C



Top view

Side view

metal-semiconductor contact resistance

$$R_{C0} = \frac{\rho_i t}{A_C} = \frac{\rho_C}{A_C} \Omega$$

$10^{-8} < \rho_C < 10^{-6}$ ž -cm^2

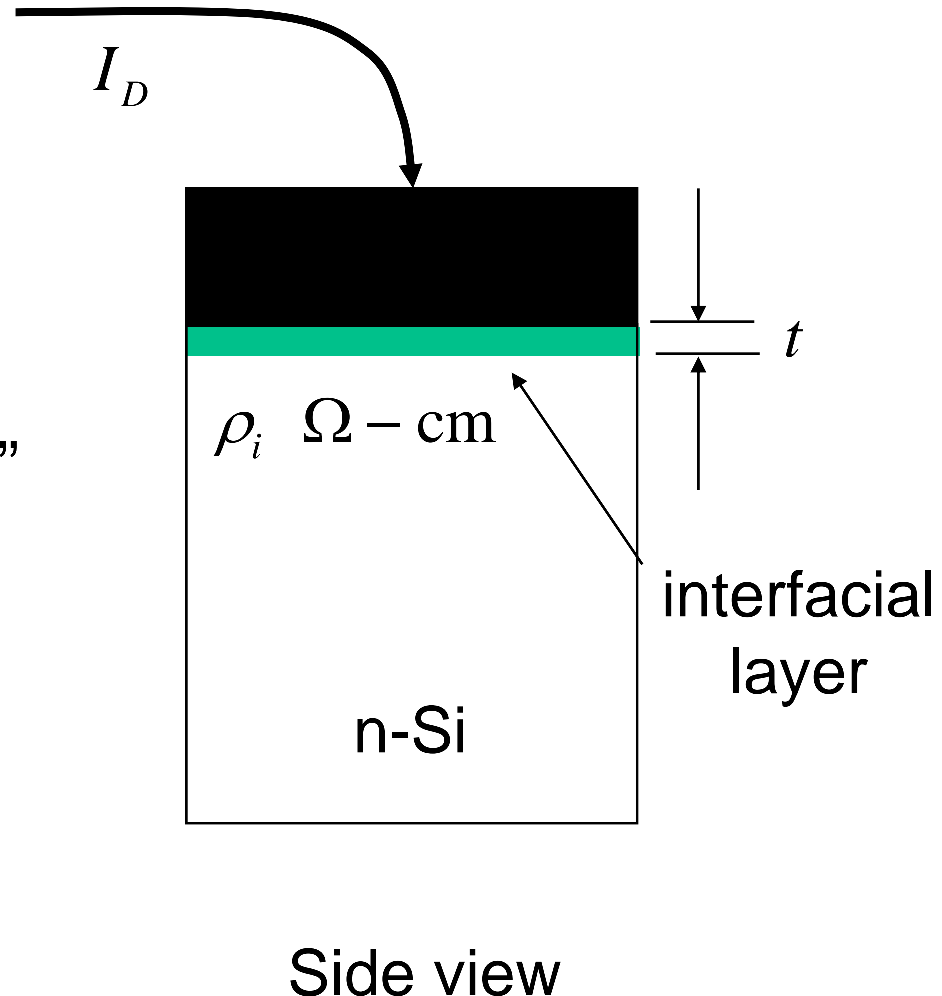
"interfacial contact resistivity"

$A_C = 0.12 \mu m \times 1.0 \mu m$

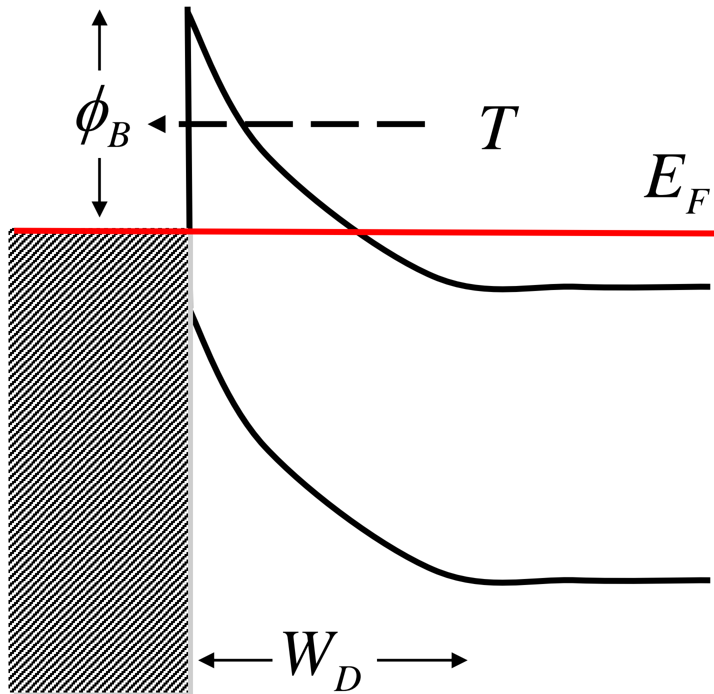
$\rho_C = 10^{-7}$ ž -cm^2

$R_{C0} = 80$ž -μm

2008 technology node
(ITRS 2007 ed.)



what determines the M-S contact resistance?



$$G_C \sim T$$

$$\rho_C \sim 1/T$$

$$T \sim e^{-\phi_B/\phi_0}$$

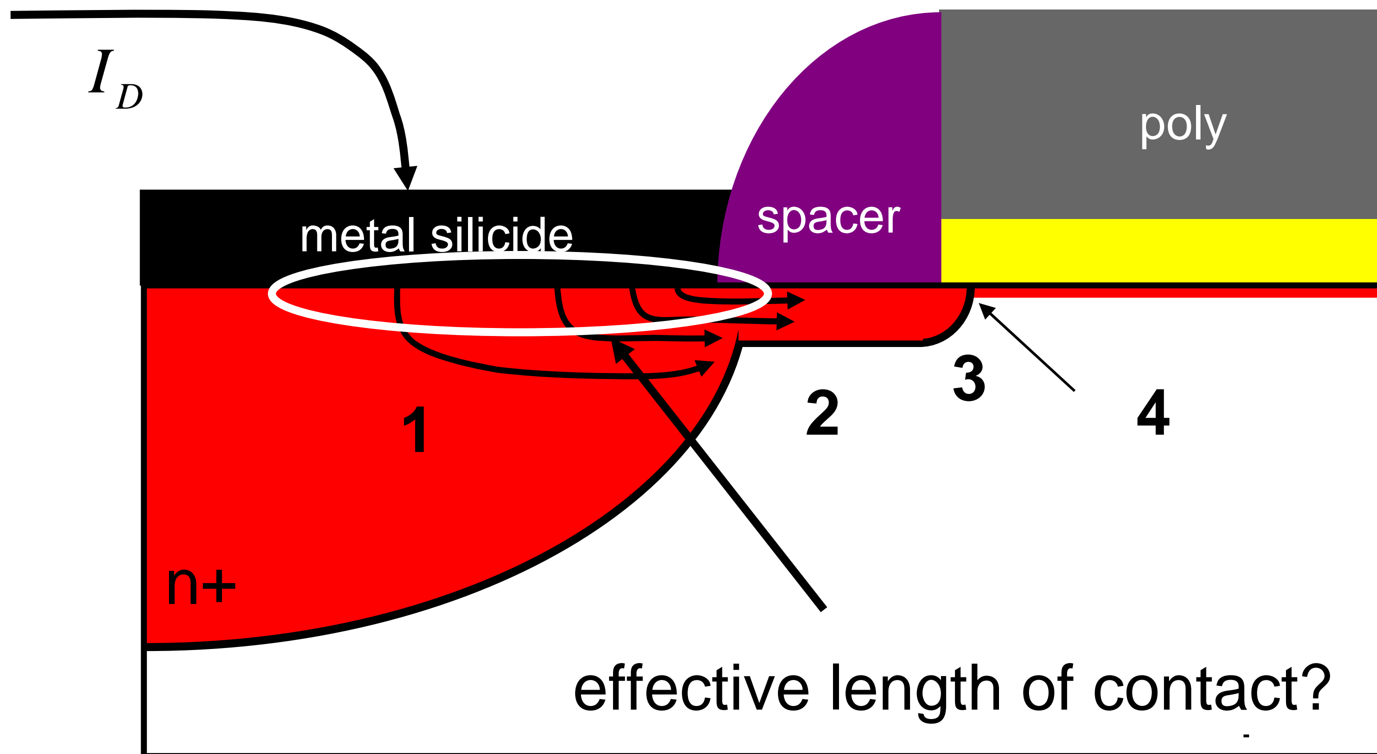
$$T \sim e^{-W_D/W_0}$$

$$W_D \sim 1/\sqrt{N_D}$$

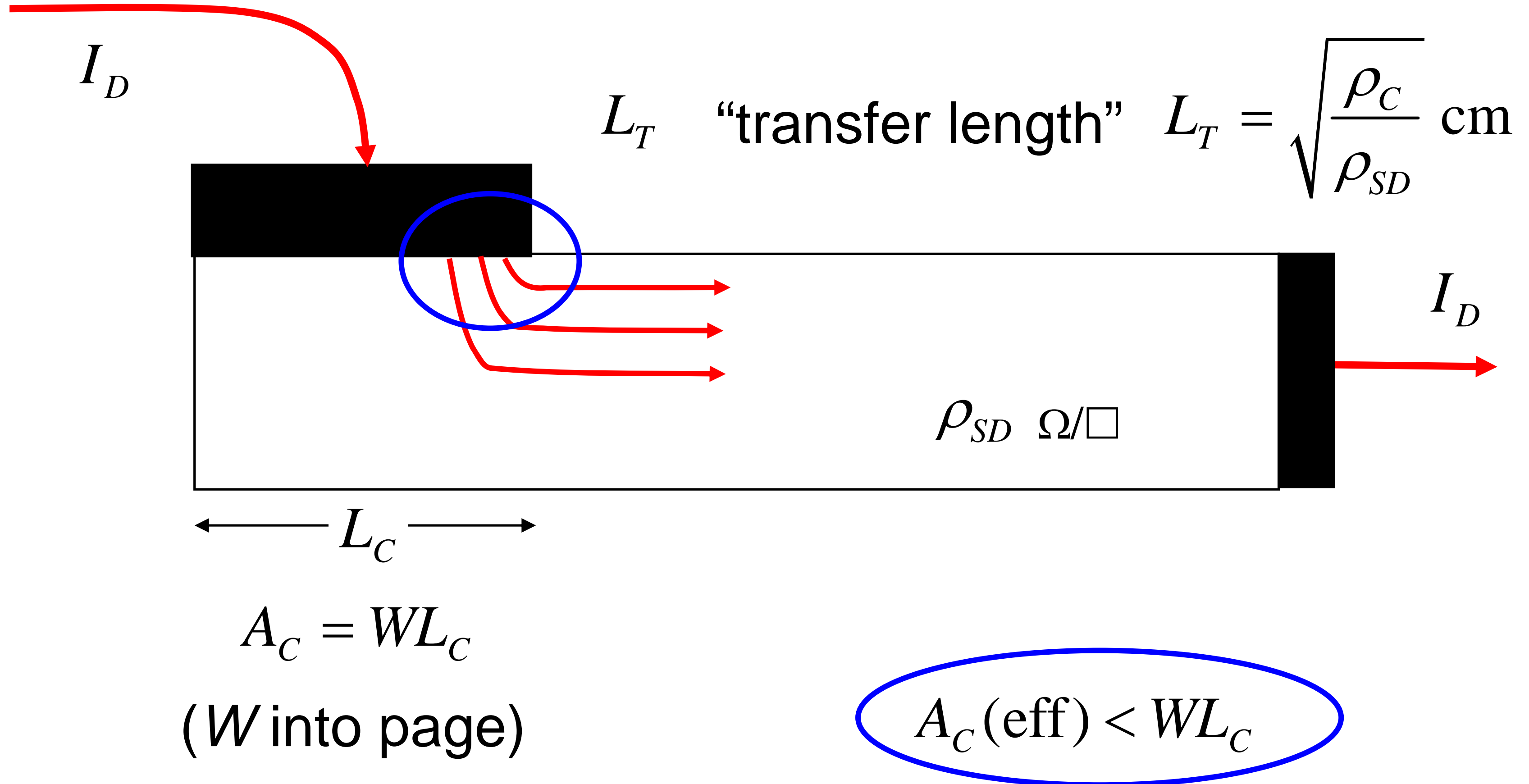
$$\rho_C \propto \exp\left[\frac{4\pi\phi_B}{qh}\sqrt{\frac{m^*\varepsilon_{Si}}{N_D}}\right]$$

(eqn. 5.11) of Taur and Ning)

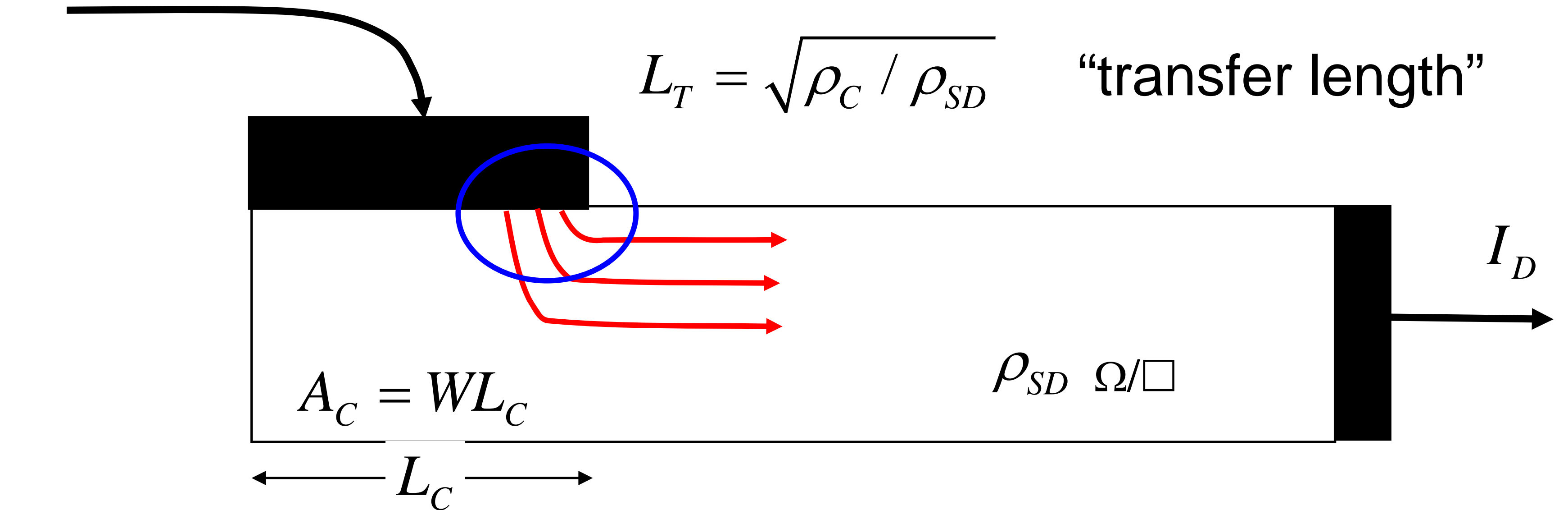
lateral current flow



lateral current flow (ii)



lateral current flow (iii)



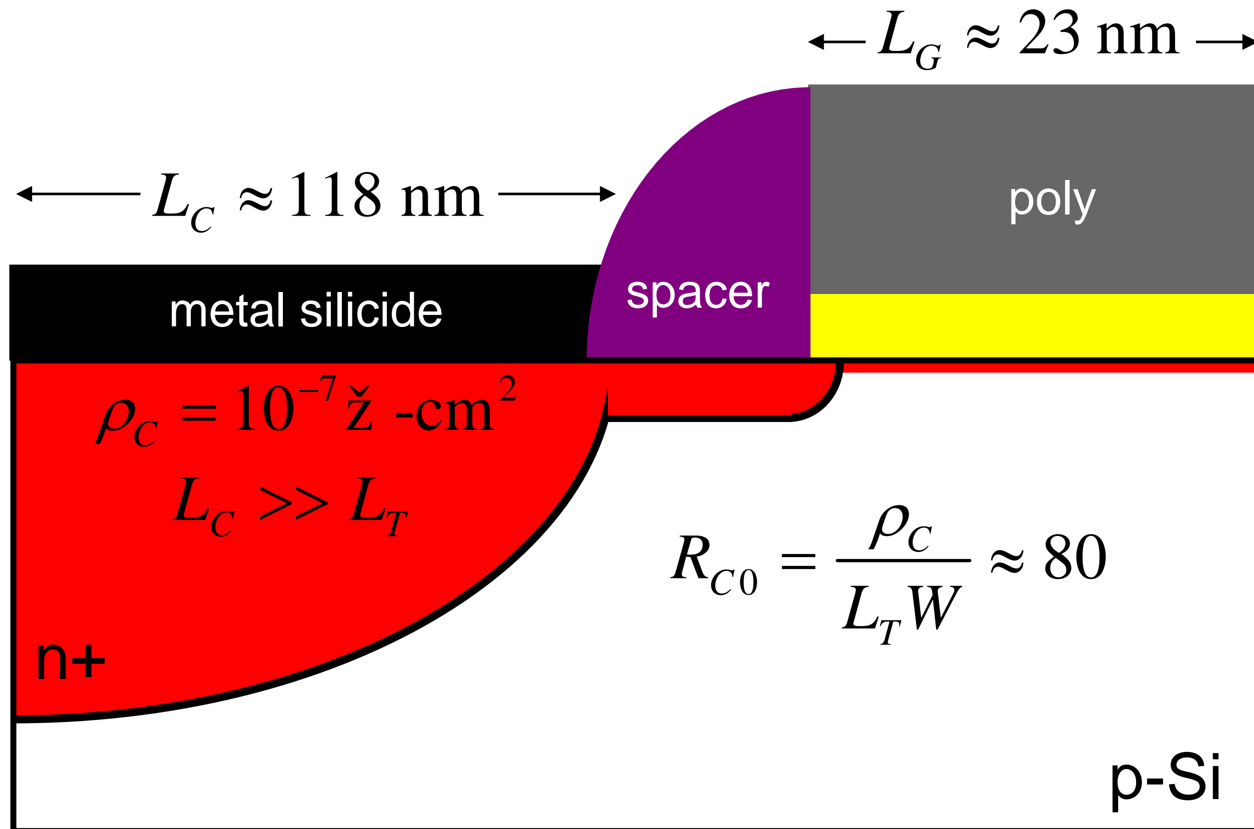
$$R_{C0} = \frac{\sqrt{\rho_C \rho_{SD}}}{W} \coth\left(L_C / L_T\right)$$

Eqn. (5.8) Taur and Ning

i) $L_C \ll L_T$: $R_{C0} = \dfrac{\rho_C}{L_C W}$

ii) $L_C \gg L_T$: $R_{C0} = \dfrac{\rho_C}{L_T W}$

silicide - Si contact resistance



2008 Technology node (2007 Ed. ITRS, PIDS chapter)

outline

1) Effect on I-V
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3) Metal-semiconductor resistance
4) **Other series resistance components**
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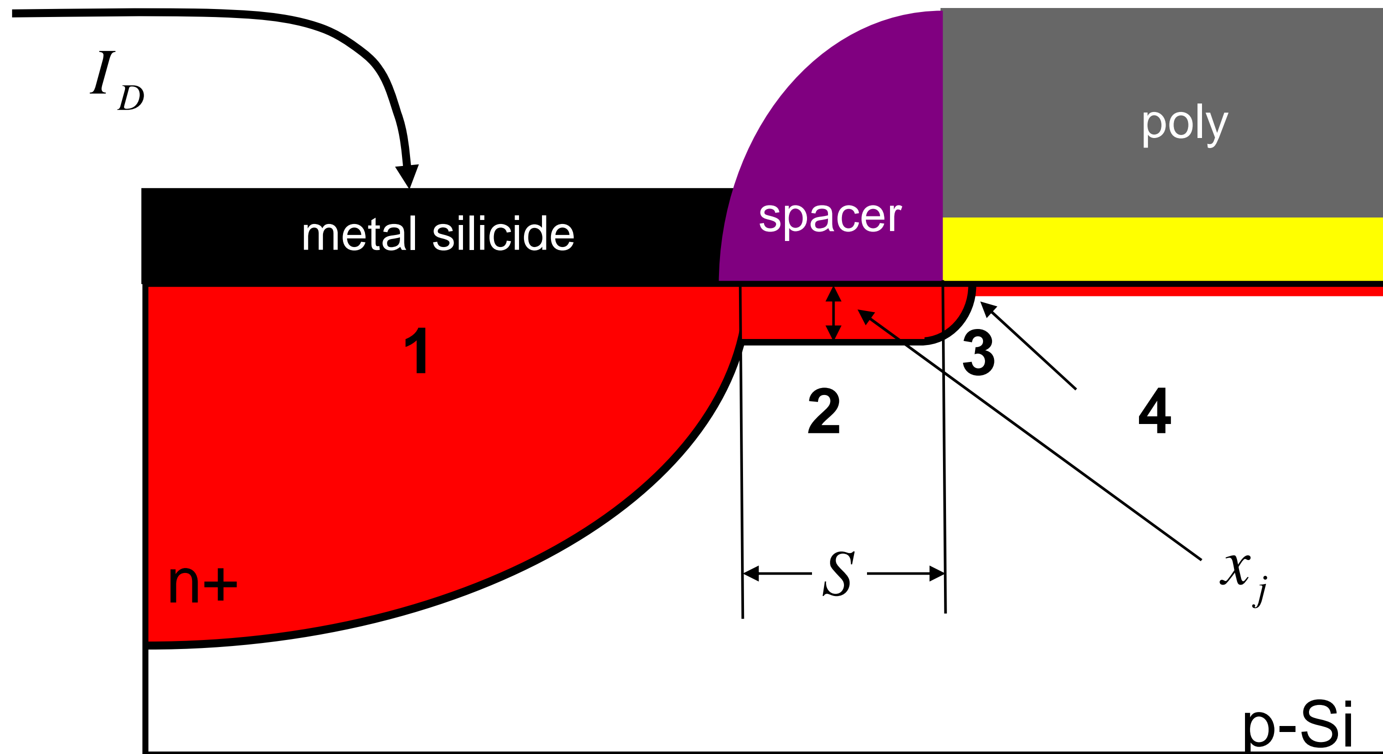
6) Effective channel length
7) Summary

physical origin of R_{SD}

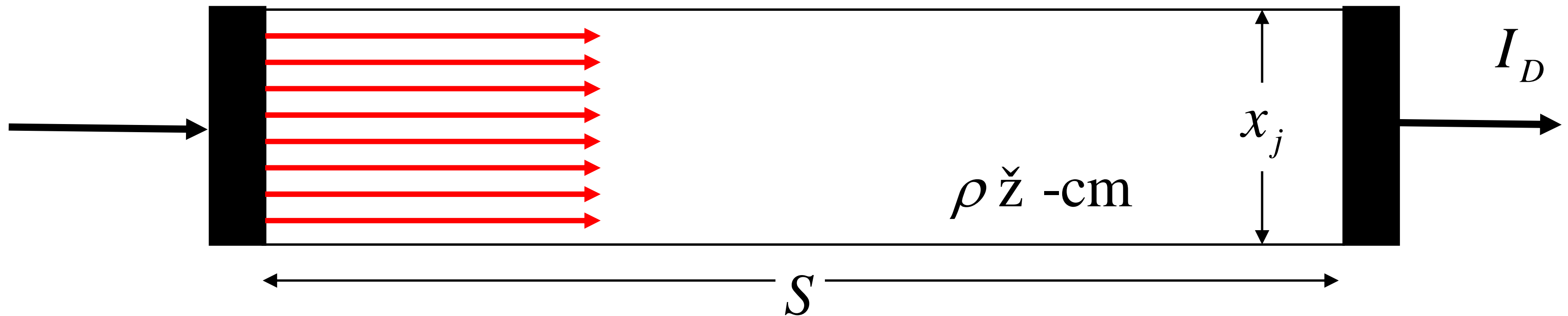


1) metal-semiconductor contact resistance
2) **extension resistance**
3) tip resistance
4) spreading resistance

resistance of the S/D extension

$$\rho = 1/\left(N_D q \mu_n\right)$$

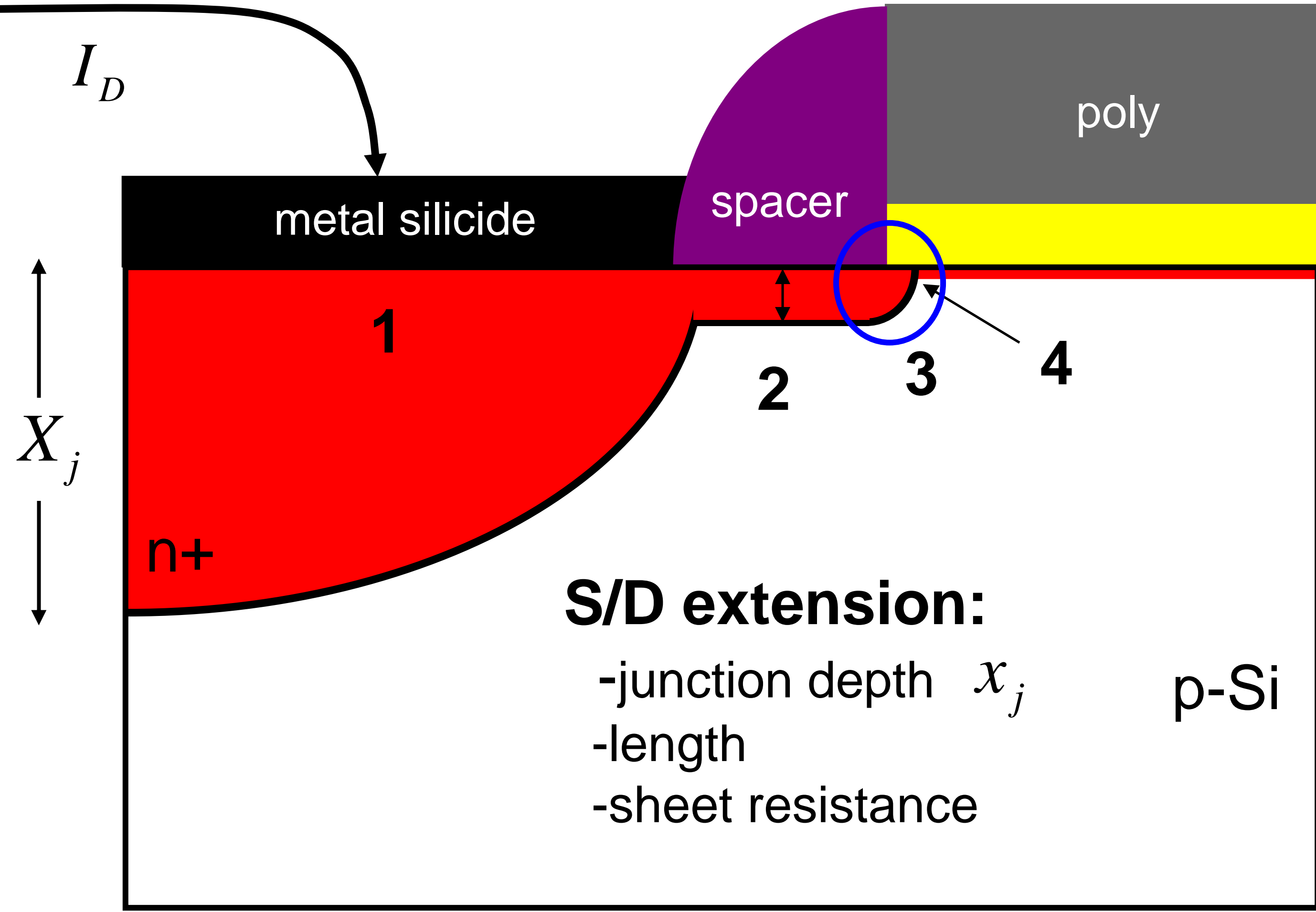
(W into page)



$$R_{EXT} = \rho \frac{S}{x_j W} = \left(\frac{\rho}{x_j}\right)\frac{S}{W} = \rho_{EXT}\frac{S}{W}$$

ρ_{EXT} Ω/□ sheet resistance of the S/D extensions

2008 technology



ITRS 2007 Edition (Front End Processes)

$$x_j = 11\ \text{nm}$$

$$\rho_{EXT} = 740\ \Omega / \text{W}$$

$$X_j = 25.3\,\text{nm}$$

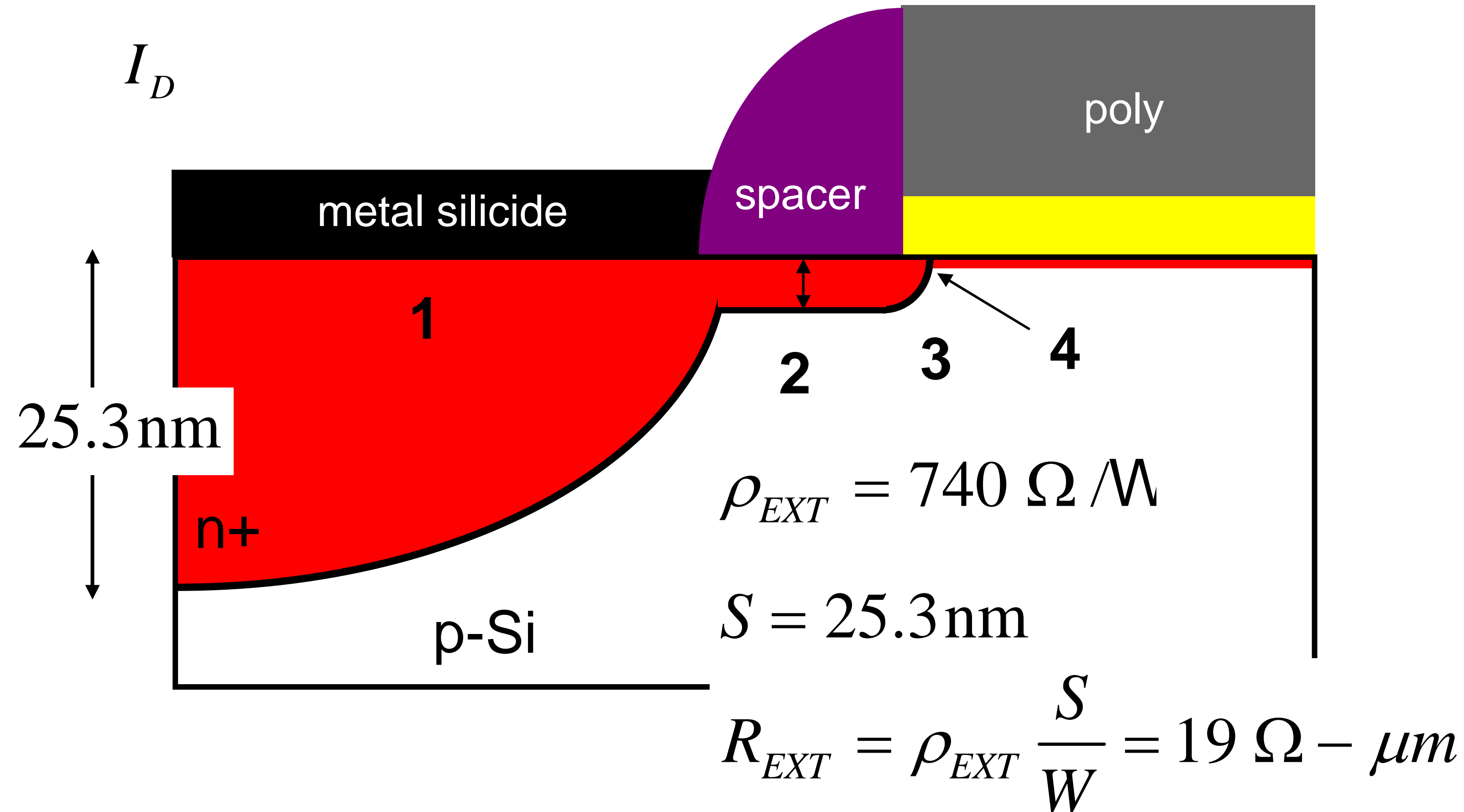
$$\left(S = 25.3\,\text{nm}\right)$$

Table FEP4a Thermal, Thin Film, Doping and Etching Technology Requirements—Near-term Years

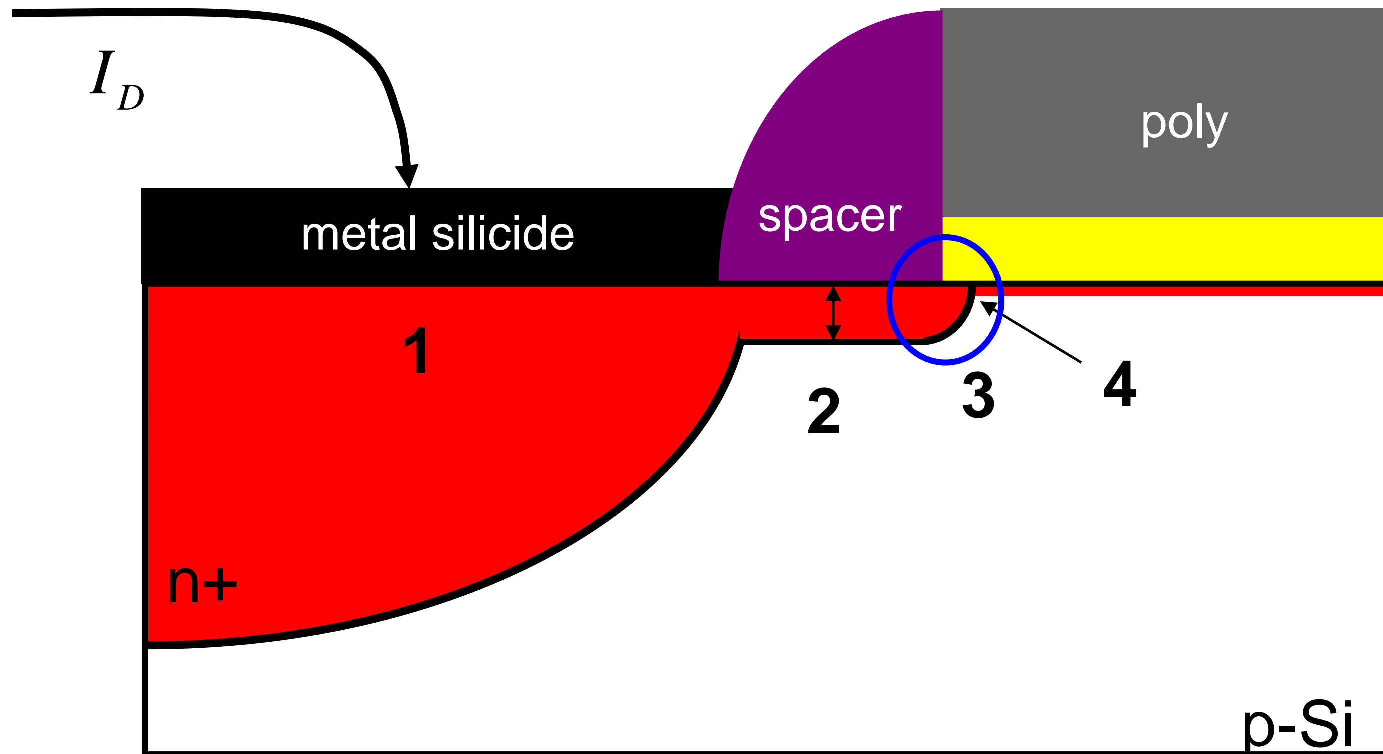
Grey cells indicate the requirements projected only for intermediate, or long-term years. Near-term line items are not included.

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 1E20-doped poly-Si [A, A1, A2]	1								
Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	1.1	0.5							
Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 3E20-doped poly-Si [A, A1, A2]	1.2	0.71	0.54	0.41					
Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]		0.9	0.75	0.65	0.55	0.5			
Gate dielectric leakage at 100 °C (A/cm²) bulk high-performance [B, B1, B2]	8.0E+02	8.7E+02	1.0E+03	1.1E+03	1.3E+03	1.4E+03			
Metal gate work function for bulk MPU/ASIC $\lvert E_{c,v} - \phi_m \rvert$ (eV) [C]		<0.2	<0.2	<0.2	<0.2	<0.2			
Channel doping concentration (cm^{-3}), for bulk design [D]	4.8E+18	3.7E+18	4.1E+18	5.4E+18	6.6E+18	8.4E+18			
Bulk/FDSOI/DG – Long channel electron mobility enhancement factor due to strain for MPU/ASIC [E]	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
Drain extension X_j (nm) for bulk MPU/ASIC [F]	12.5	11	10	9	8	7			
Maximum allowable parasitic series resistance for bulk NMOS MPU/ASIC × width ((Ω–μm) from PIDS [G]	200	200	200	180	180	180			
Maximum drain extension sheet resistance for bulk MPU/ASIC (NMOS) (Ω/sq) [G]	650	740	810	900	1015	1160			
Extension lateral abruptness for bulk MPU/ASIC (nm/decade) [H]	2.5	2.3	2.0	1.8	1.6	1.4			
Contact X_j (nm) for bulk MPU/ASIC [I]	27.5	25.3	22	19.8	17.6	15.4			

2008 technology

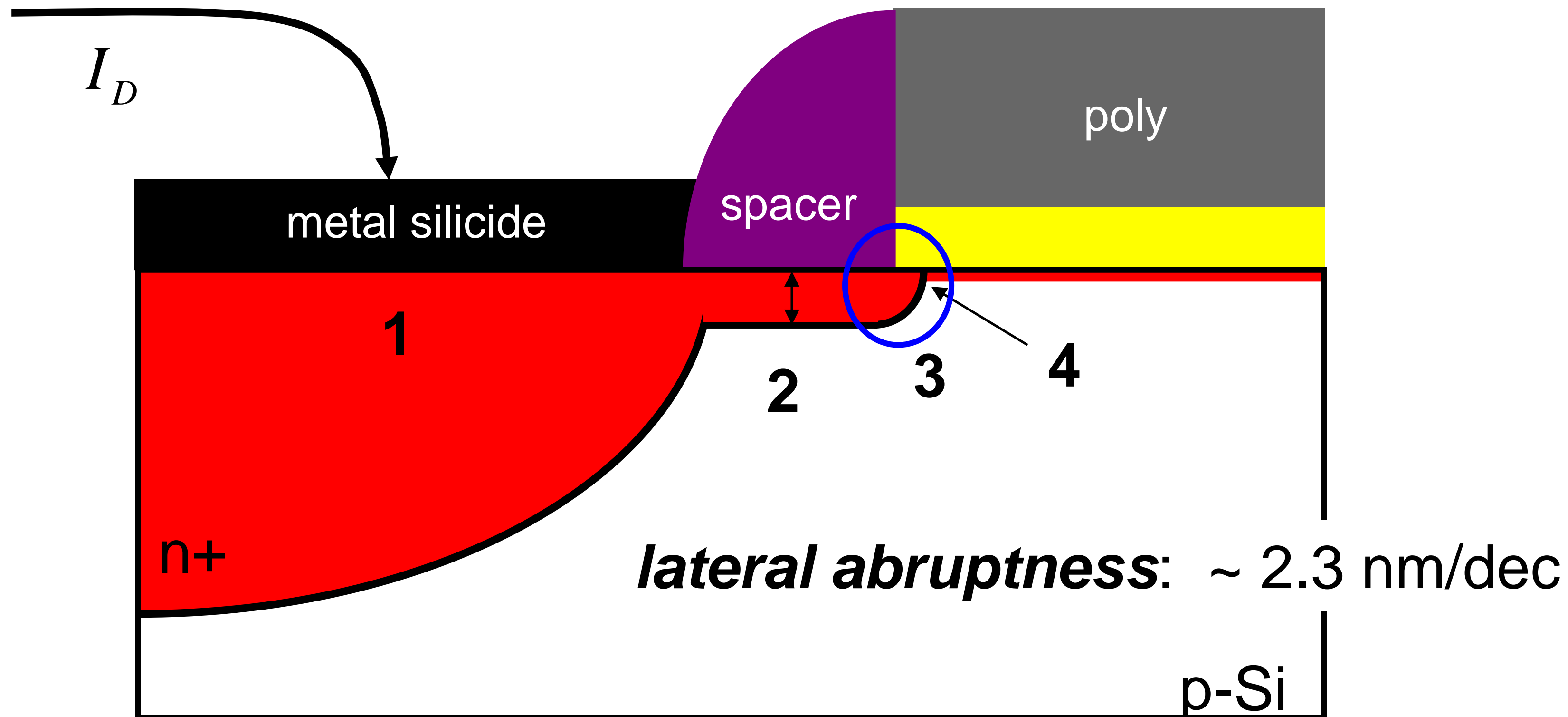


physical origin of R_{SD}



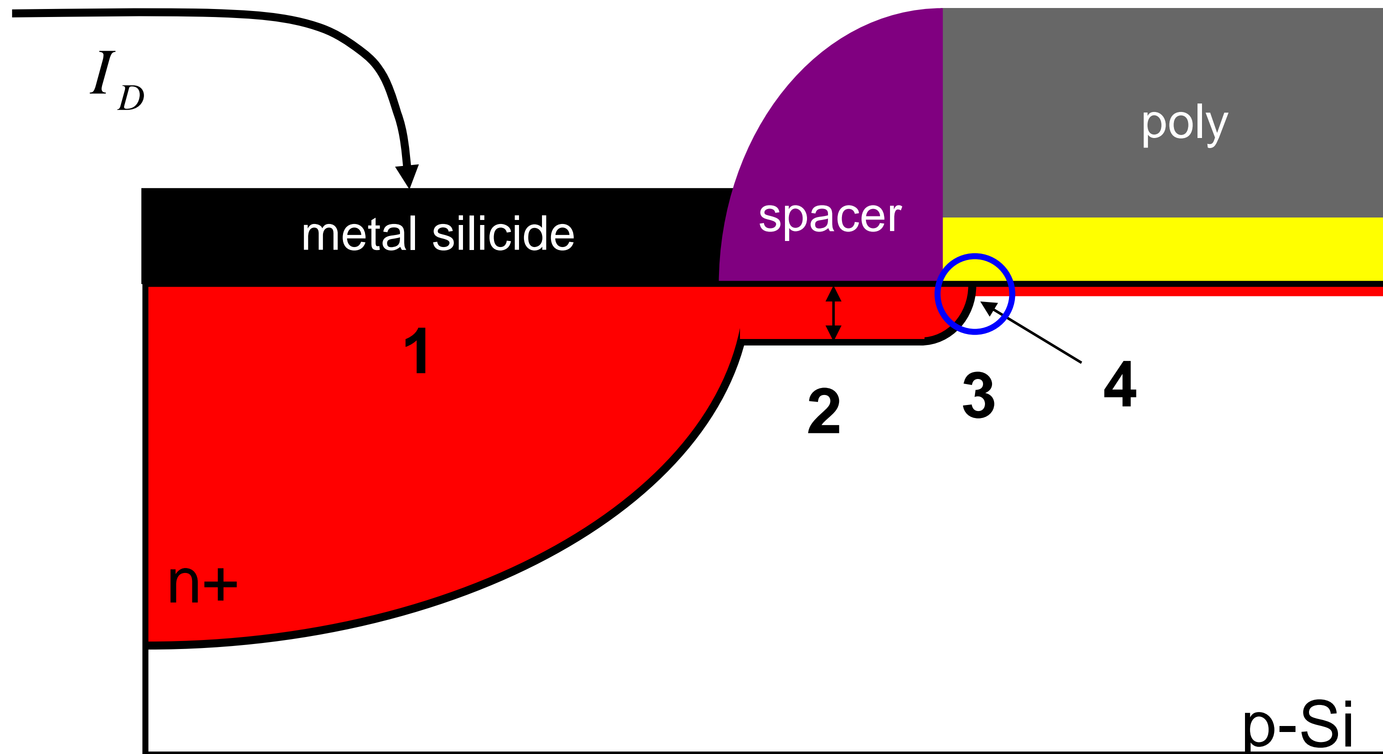
1) metal-semiconductor contact resistance
2) extension resistance
3) **tip resistance**
4) spreading resistance

physical origin of R_{SD}



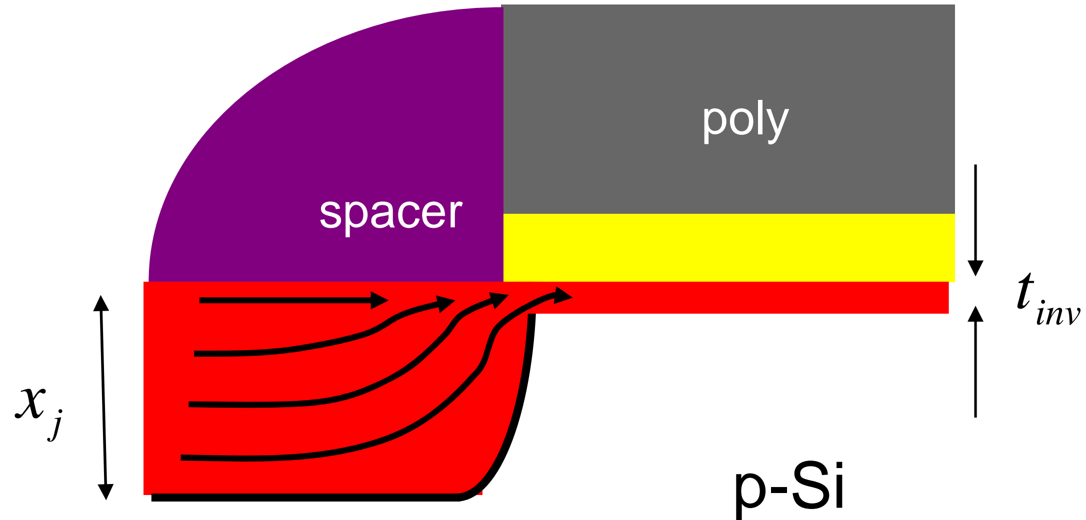
-tip resistance is controlled by the steepness of the junction
-steepness measured in nm/dec
-tip resistance is a significant part of R_{SD}

physical origin of R_{SD}



1) metal-semiconductor contact resistance
2) extension resistance
3) tip resistance
4) **spreading resistance**

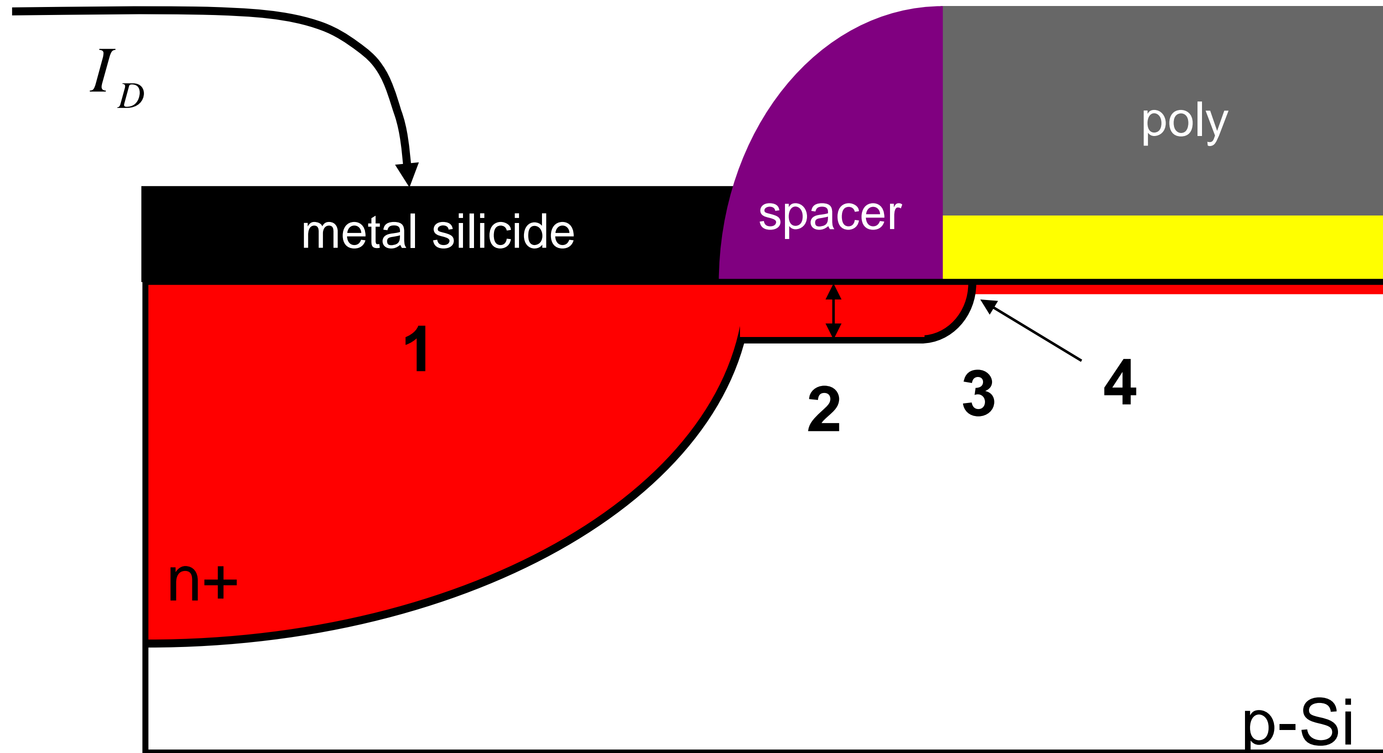
spreading resistance



$$R_{SPR} = \frac{2\rho}{\pi W}\ln\left(0.75\,\frac{x_j}{t_{inv}}\right)$$

Eqn. (5.6) of Taur and Ning

components of R_{SD}



$$R_S = R_D = R_{C0} + R_{EXT} + R_{TIP} + R_{SPR}$$

outline

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summary: components of R_{SD}

$$R_S = R_D = R_{C0} + R_{EXT} + R_{TIP} + R_{SPR} = R_{SD}/2 < 200\ \Omega-\mu\text{m}$$

1) $R_{C0} = \dfrac{\rho_C}{A_C(\text{eff})}$ $\qquad A_C(\text{eff}) \approx WL_C$ $\qquad R_{C0} \approx 80 \quad \Omega-\mu\text{m}$

2) $R_{EXT} = \rho_{EXT}\dfrac{S}{W}$ $\qquad R_{EXT} \approx 20 \quad \Omega-\mu\text{m}$

3,4) $R_{TIP} + R_{SPR}$ $\qquad$ 'link-up resistance'

scaling considerations

$$R_{ON} = \frac{V_{DD}}{I_{ON}} \rightarrow \frac{V_{DD}/\kappa}{I_{ON}/\kappa} \qquad R_{ON} \rightarrow R_{ON}$$

In practice, R_{ON} is ***decreasing***

want $R_S < 10\% \, R_{ON}$

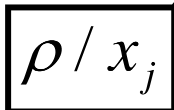
How does R_S *scale?*

scaling of R_S

$$R_S = R_{C0} + R_{EXT} + R_{TIP} + R_{SPR}$$

$$R_{C0} = \frac{\rho_C}{A_C(\text{eff})} \rightarrow \frac{\rho_C}{A_C(\text{eff})/\kappa^2} \qquad R_{C0} \rightarrow \kappa^2 R_{C0}$$

$$R_{EXT} = \rho_{EXT}\frac{S}{W} \rightarrow \kappa\,\rho_{EXT}\frac{S/\kappa}{W/\kappa} \qquad R_{EXT} \rightarrow \kappa R_{EXT}$$



ρ / x_j

R_S increases with scaling!

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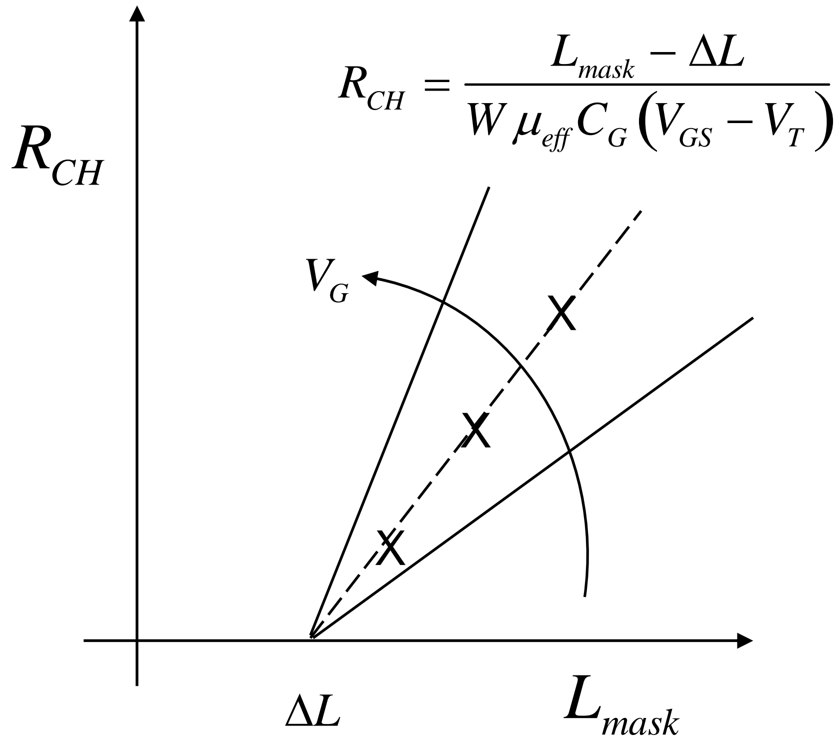
effective channel length

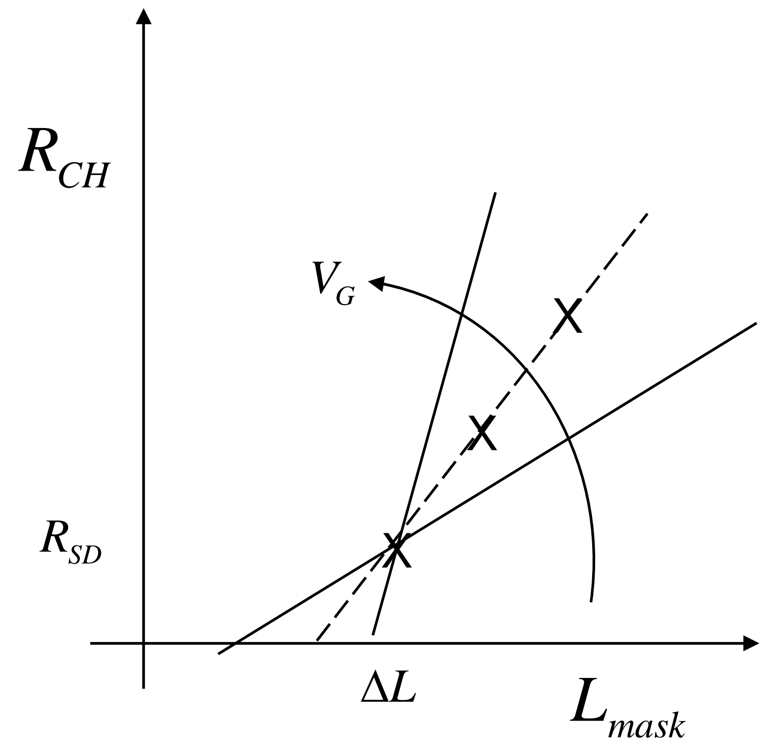
$$I_D = \frac{W}{L_{eff}} \mu_{eff} C_G \left(V_{GS} - V_T\right) V_{DS} = V_{DS} / R_{CH}$$

$$\frac{V_{DS}}{I_D} = R_{CH} = \frac{L_{eff}}{W \mu_{eff} C_G \left(V_{GS} - V_T\right)} = \frac{L_{mask} - \Delta L}{W \mu_{eff} C_G \left(V_{GS} - V_T\right)}$$

measuring Leff

with series resistance





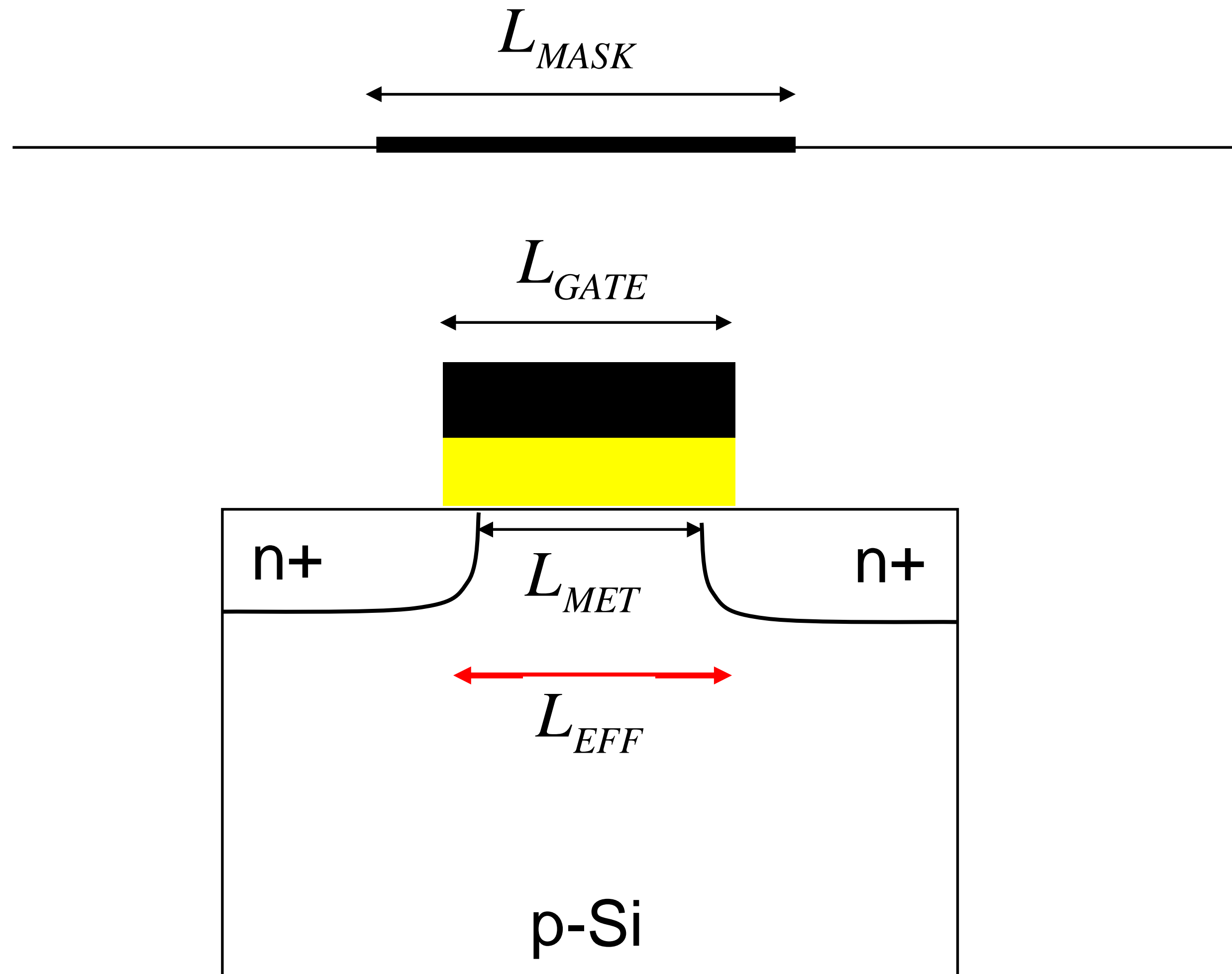
what is Leff?

"measure of gate-controlled current"

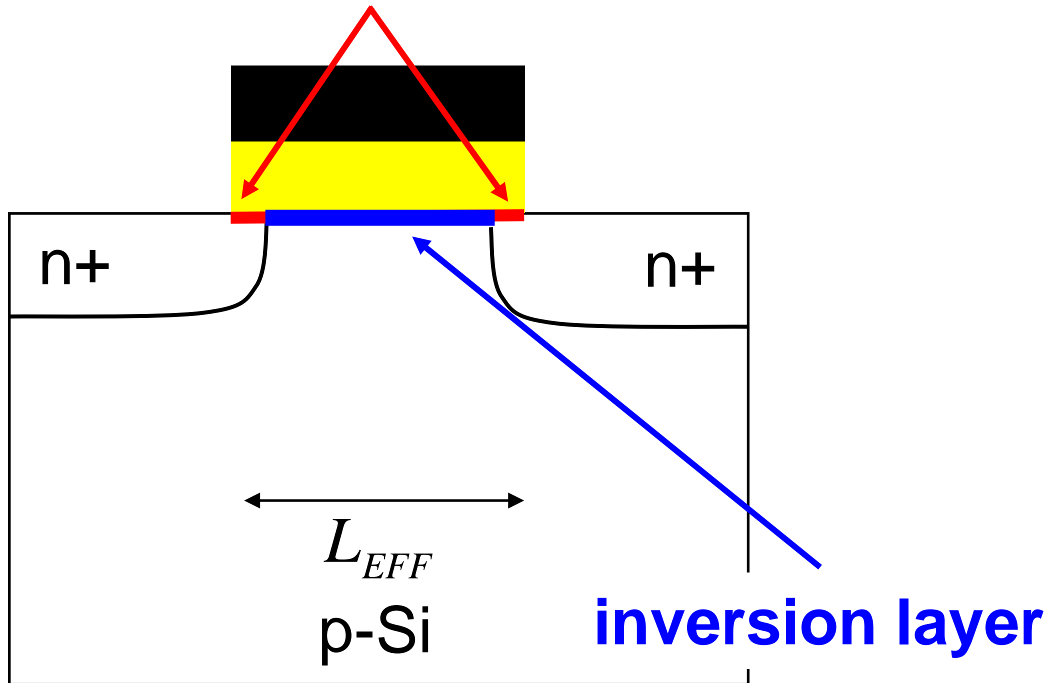
Y. Taur, *IEEE Trans. Electron Devices*, **47**, pp. 160-170, 2000

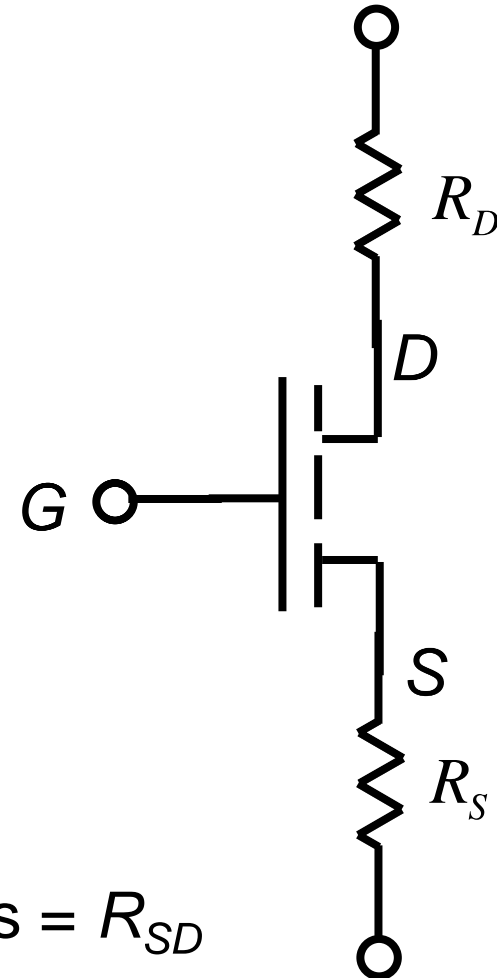
See also, Taur and Ning, pp. 202-221

various channel lengths



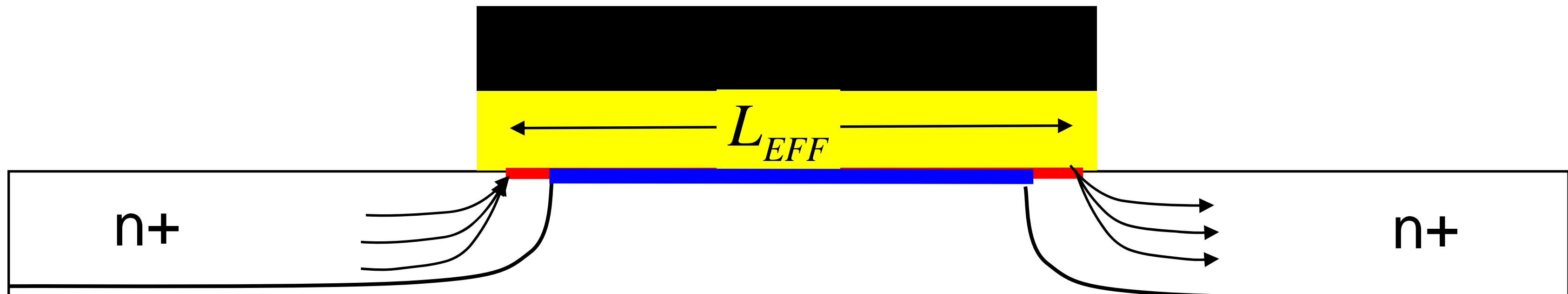
physical interpretation





gate voltage independent resistances = R_{SD}

physical interpretation



when sheet resistance underneath the accumulation layer is less than the sheet resistance of the accumulation layer, current spreads into the bulk n+ region and the channel ends.

outline

1) Effect on I-V
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summary

Achieving an acceptably low series resistance is a serious challenge that gets more difficult as device scaling continues.