EE-612:
Lecture 16:
MOSFET Leakage

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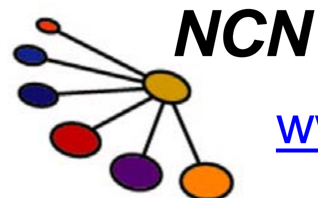

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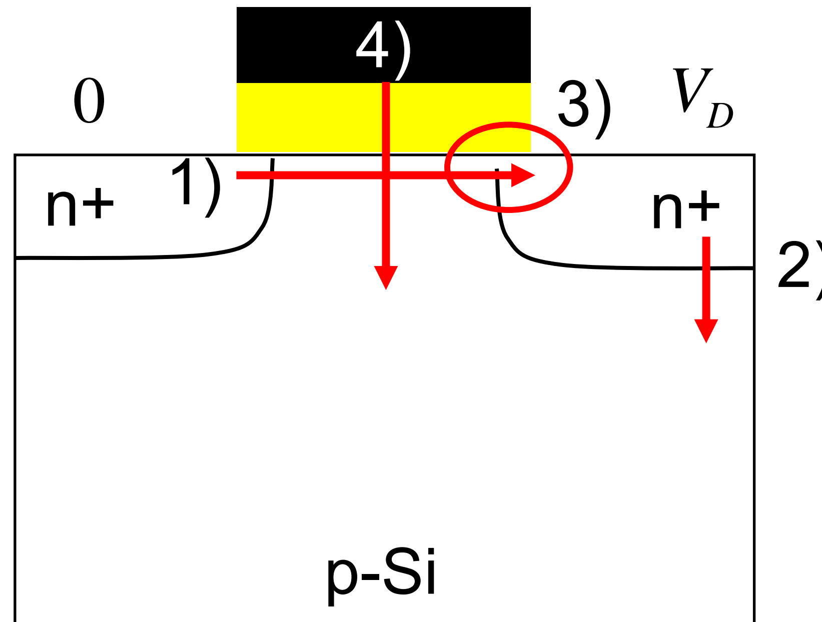
outline

1) MOSFET leakage components
2) Band to band tunneling
3) Gate-induced drain leakage
4) Gate leakage
5) Scaling and ITRS
6) Summary

leakage components



1) subthreshold current
2) junction leakage
3) gate-induced drain leakage (GIDL)
4) gate-leakage

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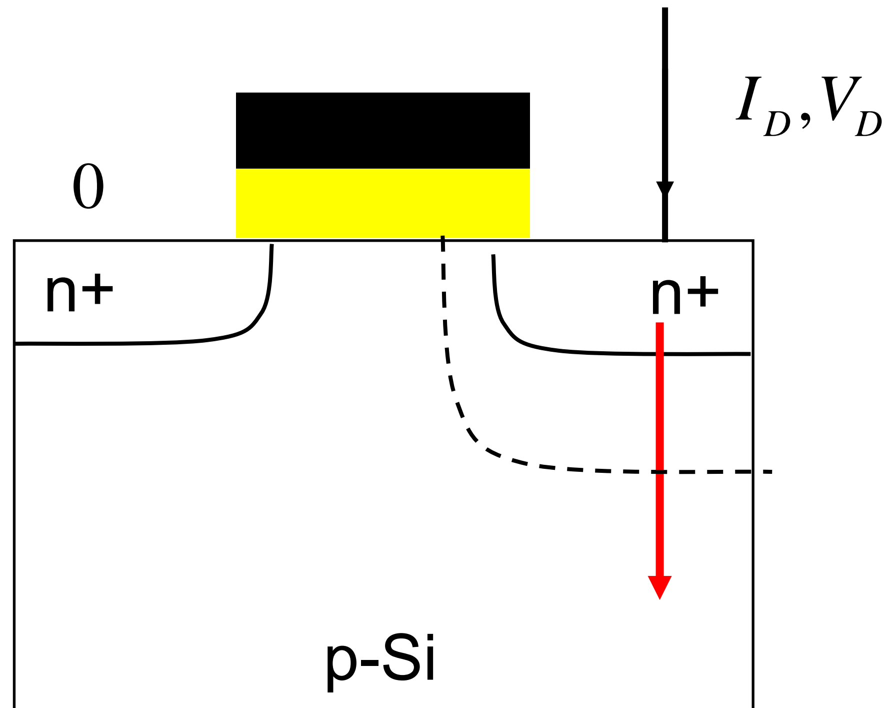
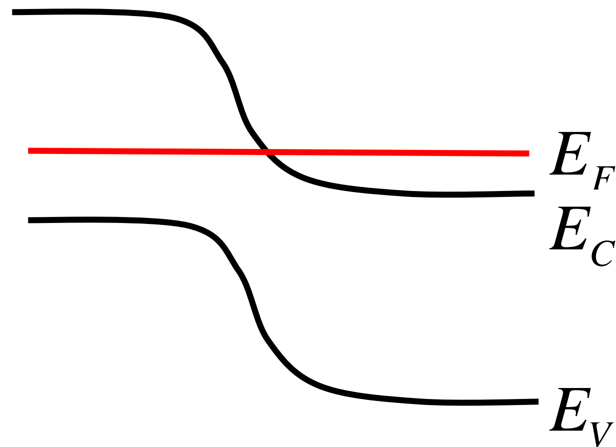
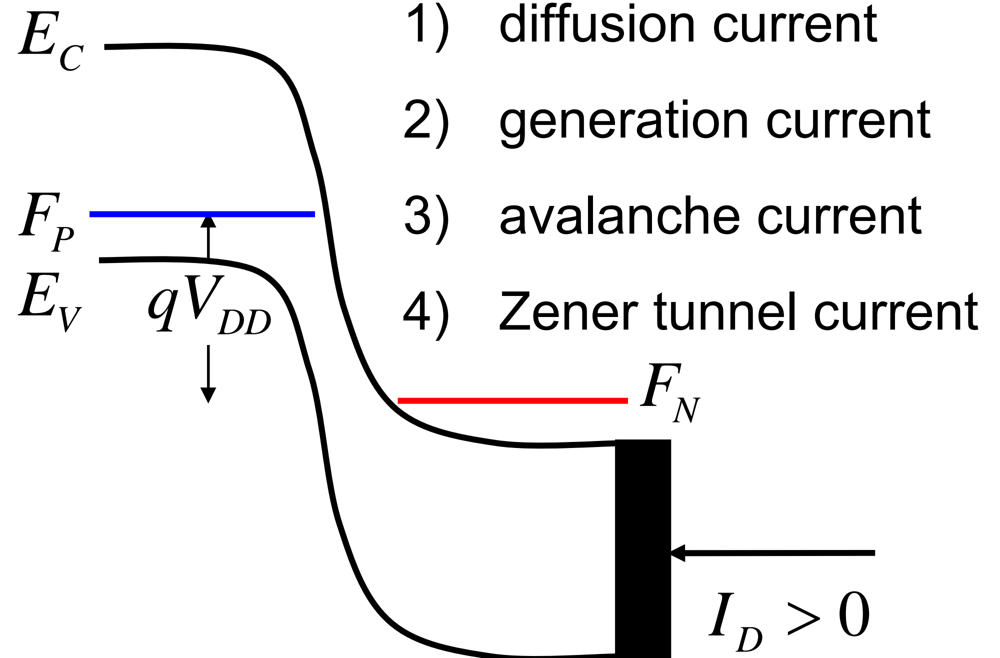
drain leakage current

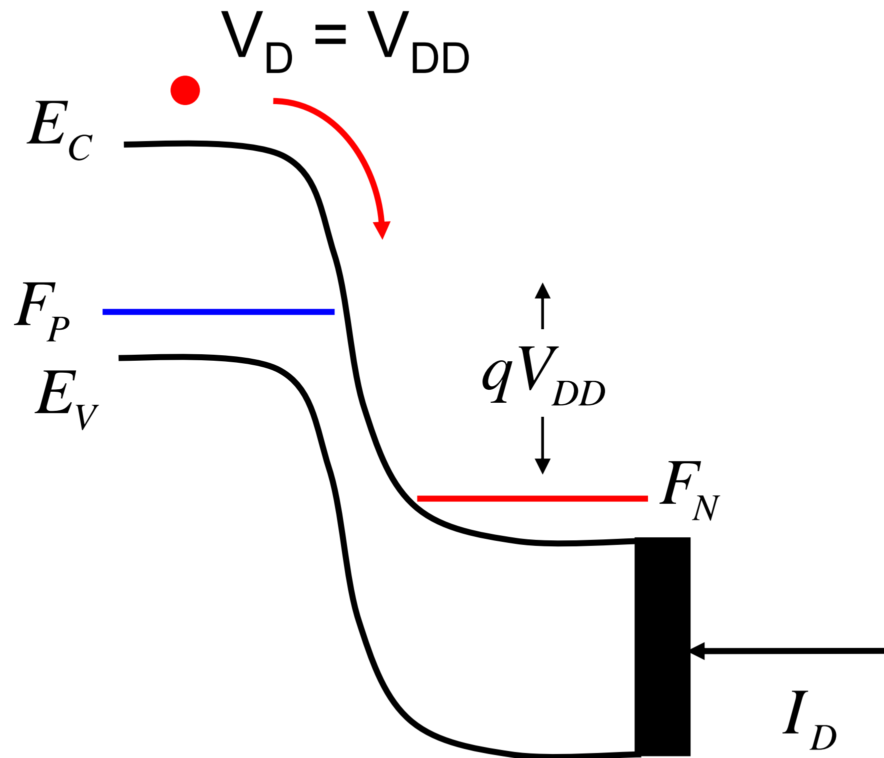


junction leakage current components





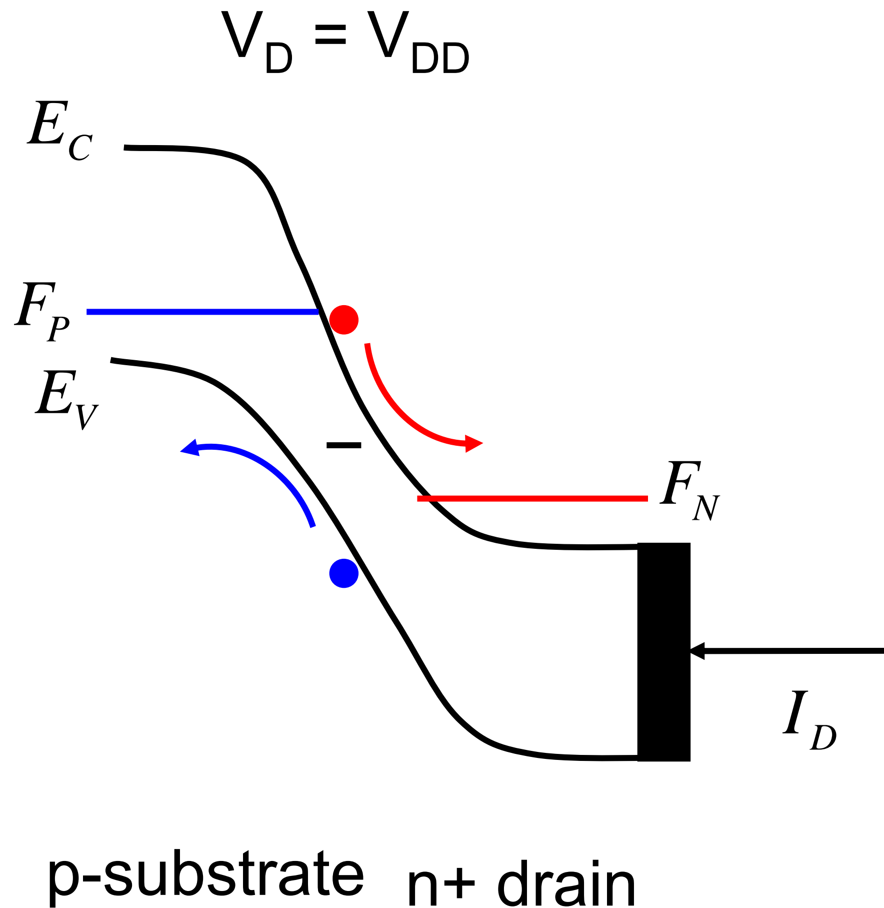
diffusion current



$$J_n = q\frac{D_n}{L_n}\frac{n_i^2}{N_A}\left(e^{qV_D/k_BT} - 1\right)$$

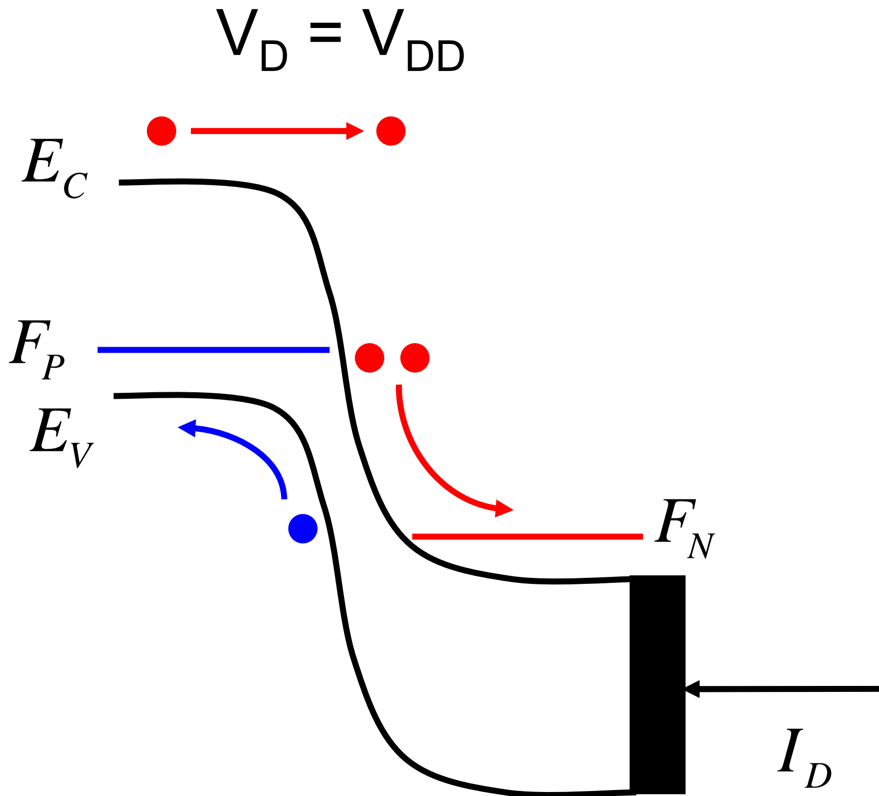
p-substrate   n+ drain

generation current



$$J_n = qW_{eff}\left(V_D\right)\frac{n_i}{2\tau}\left(e^{qV_D/2k_BT} - 1\right)$$

avalanche current



p-substrate n+ drain

$$dJ_n = \alpha_n J_n dx + \alpha_p J_p dx$$

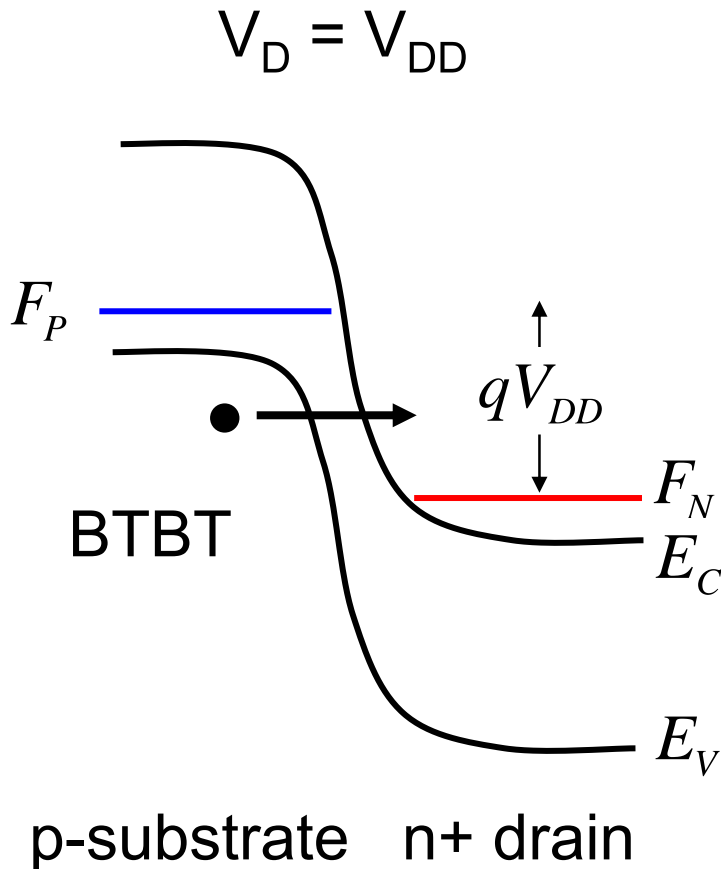
empirical expression: $\alpha = Ae^{-b/E}$

the ***peak*** electric field is the most important

α ***decreases*** as T increases

BTBT in the drain-substrate junction

$V_D = V_{DD}$



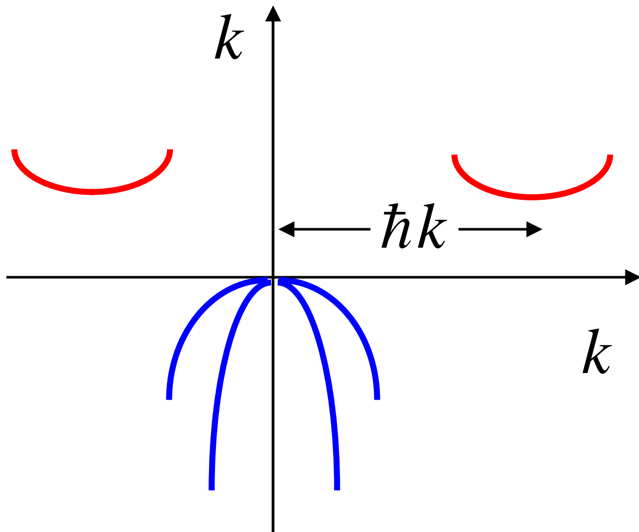
expect J(BTBT) to vary as: $e^{-E_G/A}$

also should vary as: $e^{-W_{DEPL}/B}$

$e^{-C/E}$

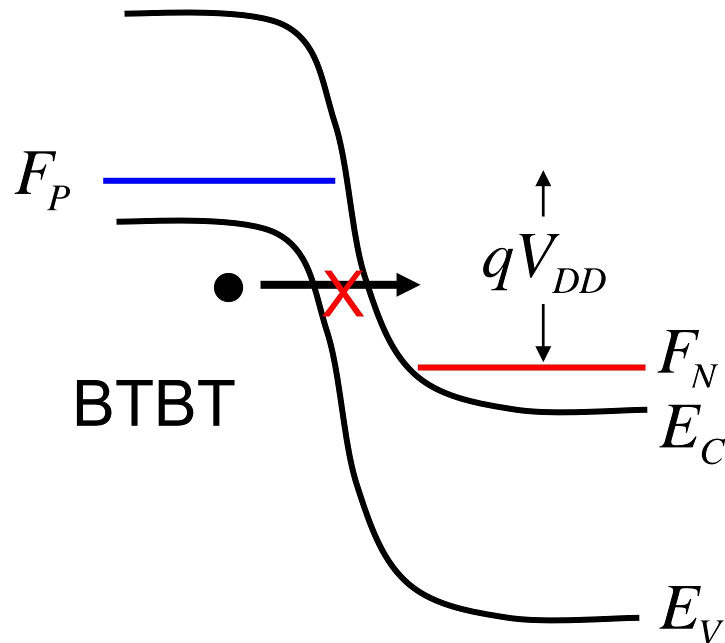
BTBT in the drain-substrate junction

k-space



conserve crystal momentum by phonon emission or absorption

$V_D = V_{DD}$



defect-assisted tunneling

BTBT (iii)

tunneling probability should involve the barrier height (E_G) and the barrier width (depletion layer)

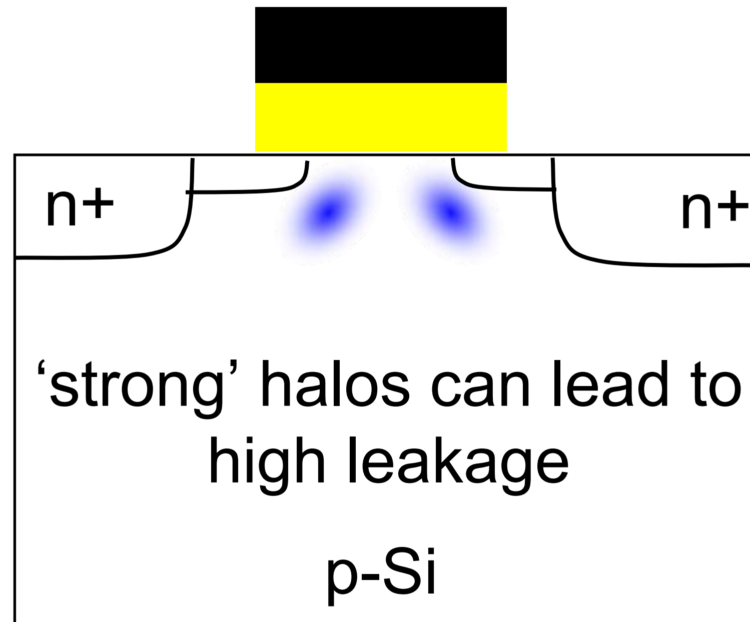
$$J_{B-B} = \frac{\sqrt{2m^*}q^3 E V_{DD}}{4\pi^3 \hbar^2 E_G^{1/2}} \exp\left[-\frac{4\sqrt{2m^*}E_G^{3/2}}{3qE\hbar}\right]$$

eqn. (2.27) of Taur and Ning

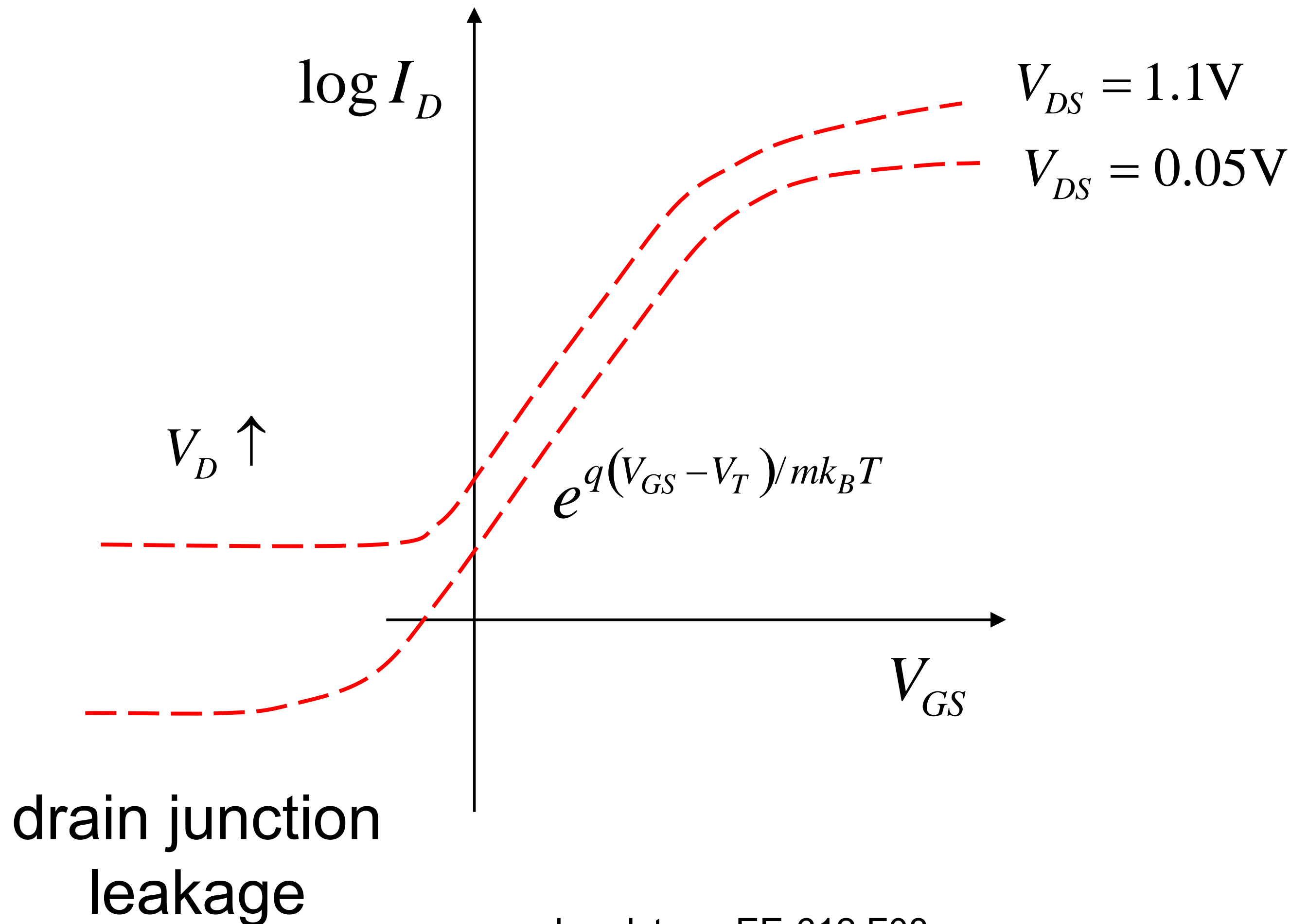
$$E = \sqrt{\frac{2qN_A\left(V_{DD} + V_{bi}\right)}{\varepsilon_{Si}}}$$

for $N_A = 5 \times 10^{18}$ cm^{-3}, V_{DD}=1V, J_{B-B} ~ 1A/cm^2

BTBT and halos



BTBT: effect on I-V



BTBT (iv)

BTBT trends

BTBT is becoming increasingly important as channel doping densities increase.

It is also a concern for alternative channel materials with smaller bandgaps.

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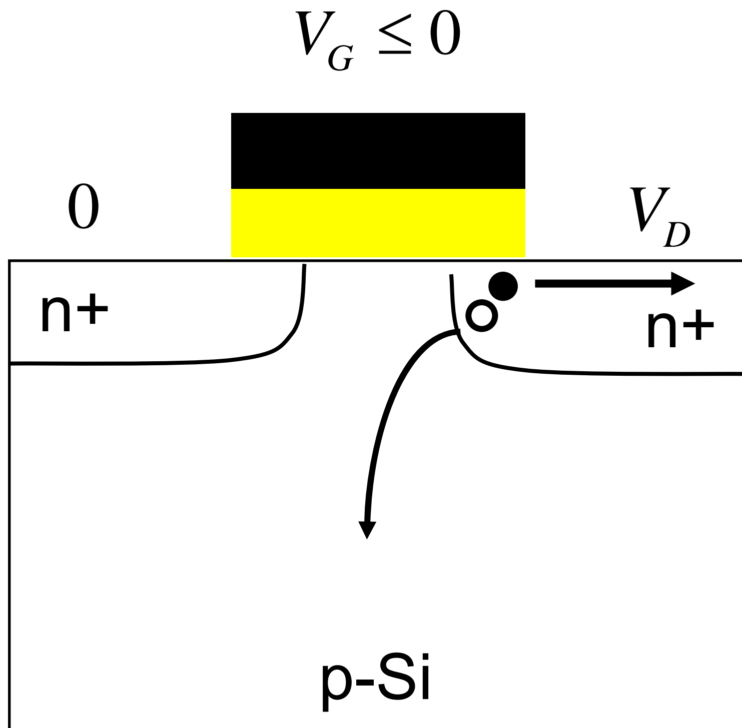
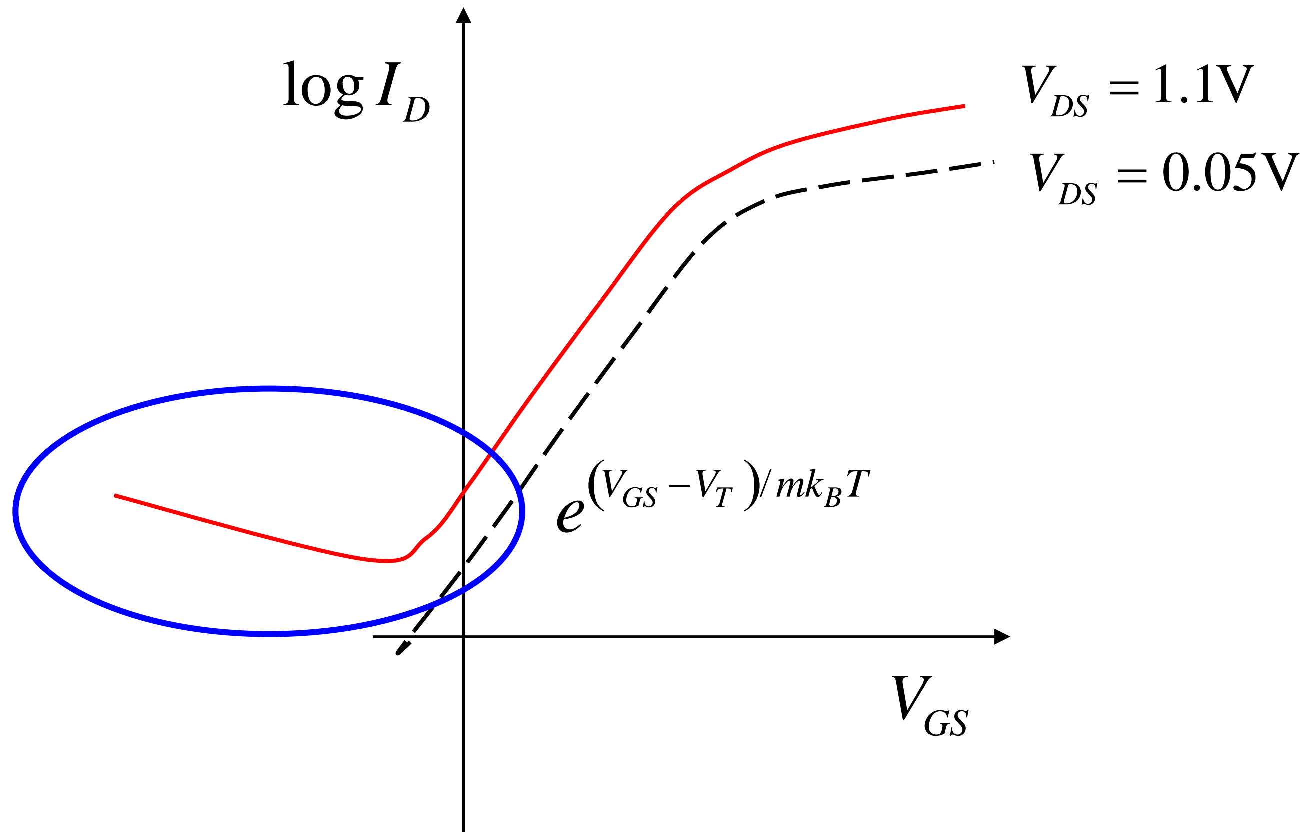
gate-induced BTBT

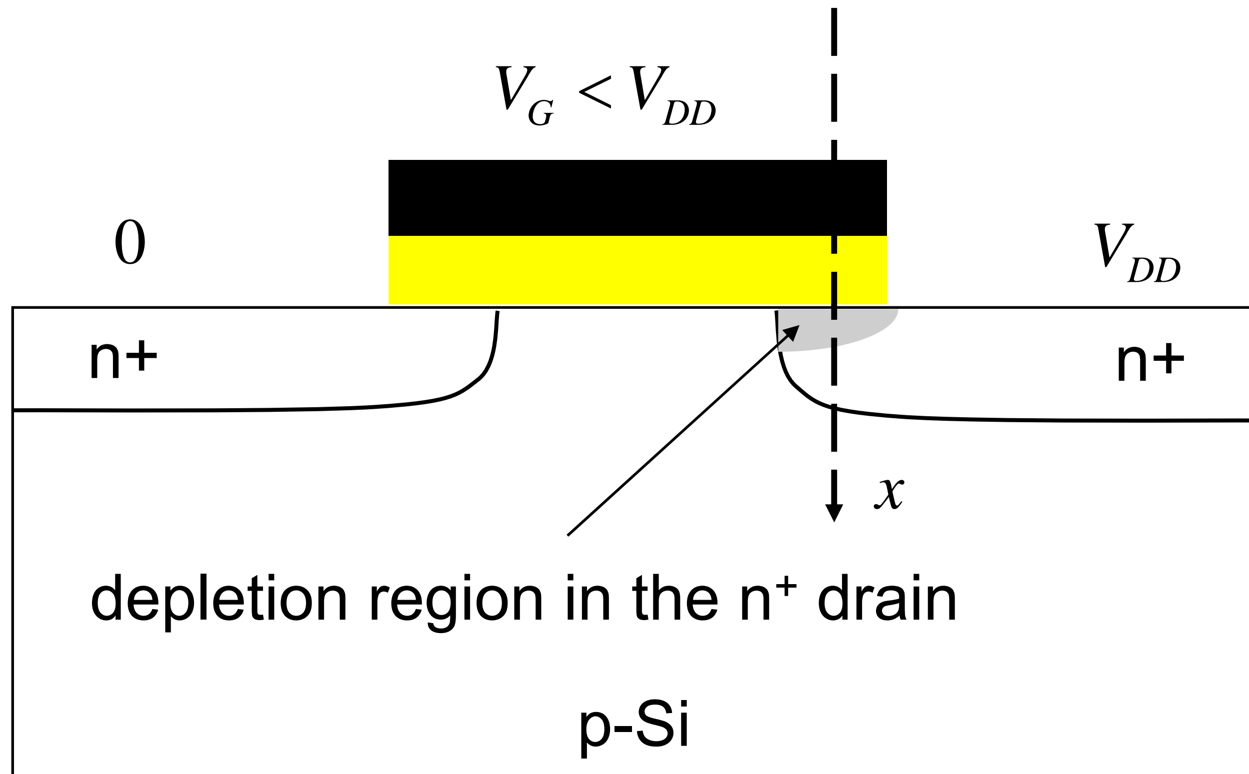


BTBT can occur at the surface!

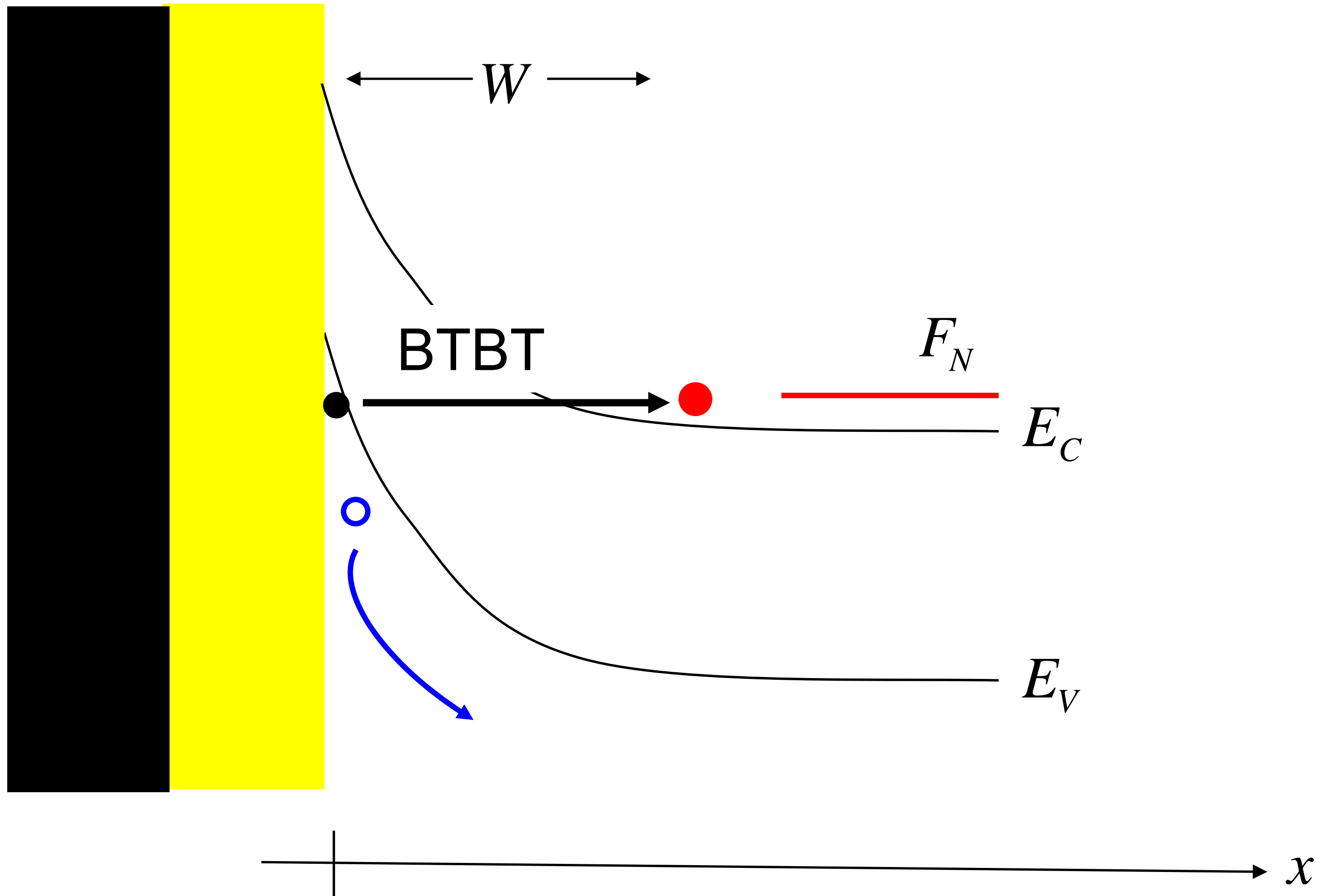
gate-induced BTBT: effect on I-V



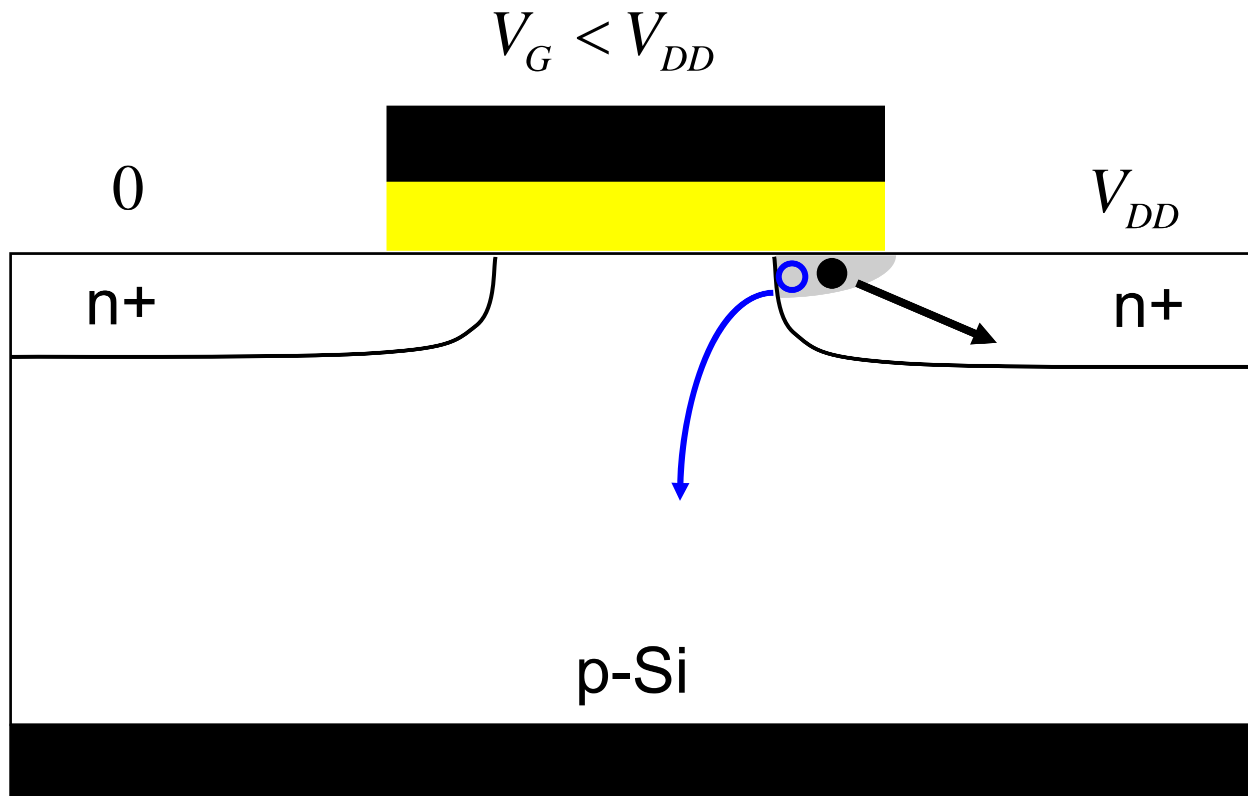
gate-induced drain leakage (GIDL)



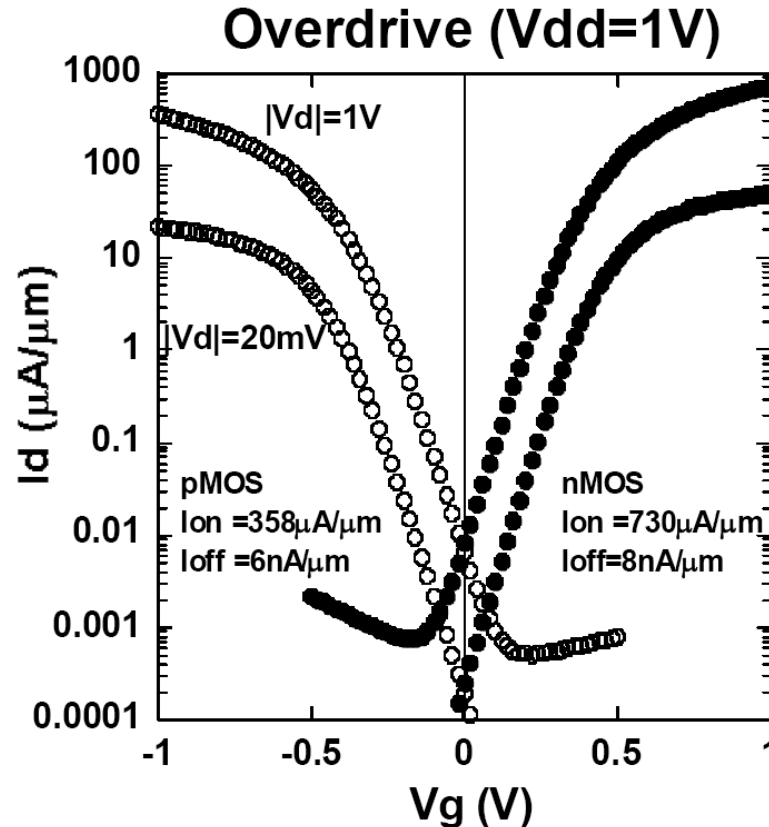
GIDL (iii)



GIDL (iii)



GIDL: example



M. Okuno, et al., "45-nm Node CMOS Integration with a Novel STI Structure and Full-NCS/Cu Interlayers for Low-Operation-Power (LOP) Applications," IEDM, Washington DC. Dec. 5-7, 2005

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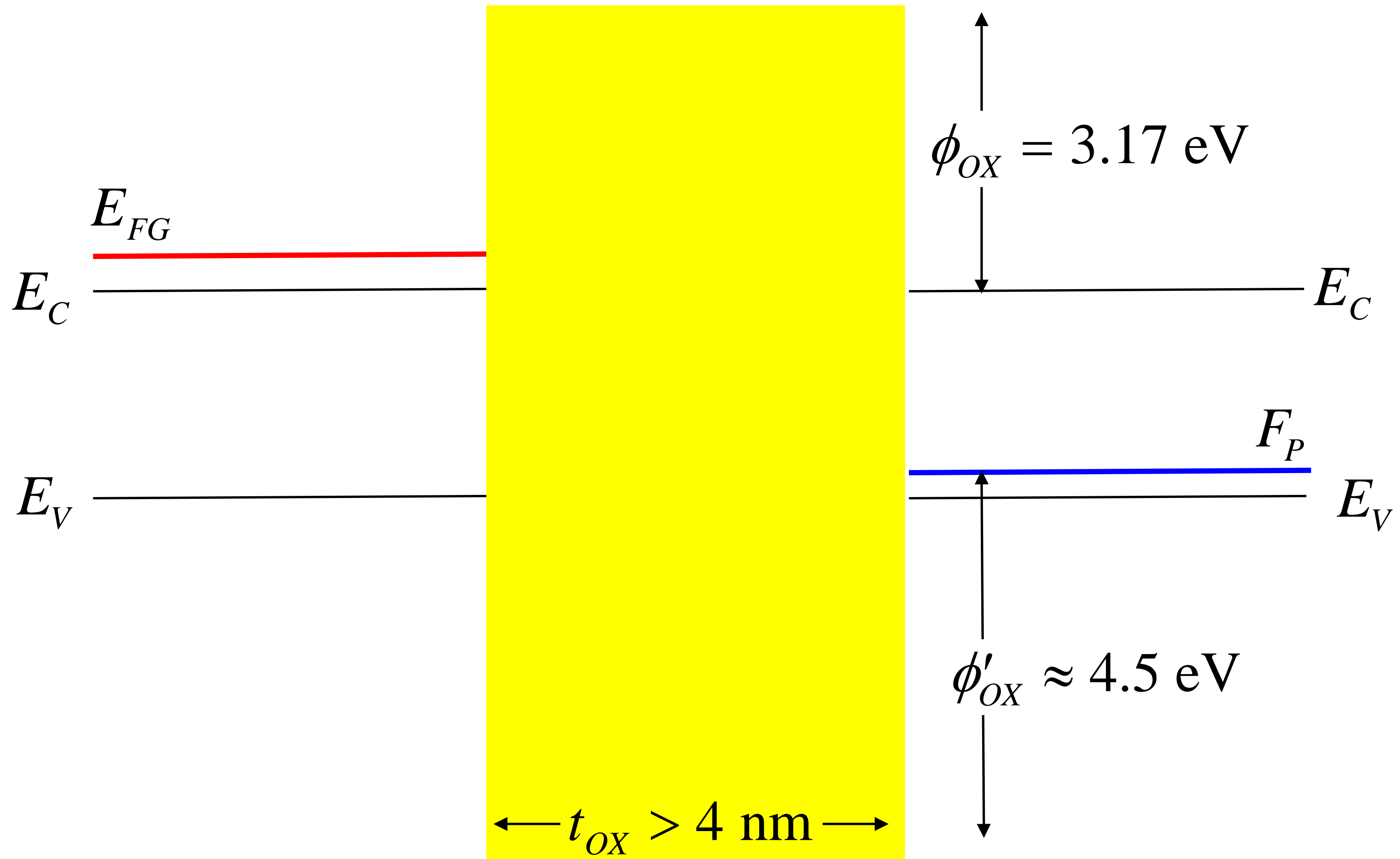
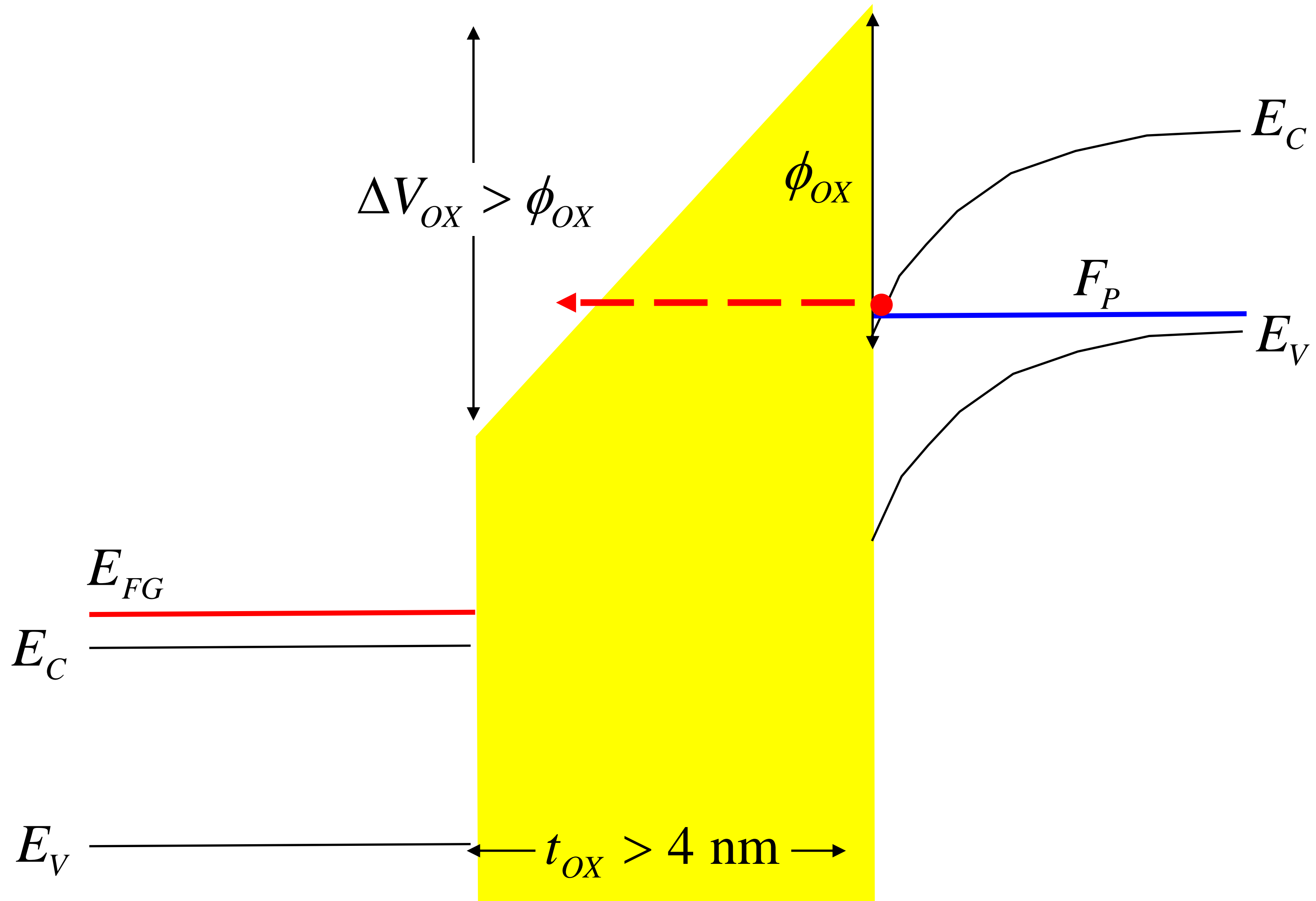
gate leakage



Fowler-Nordheim tunneling



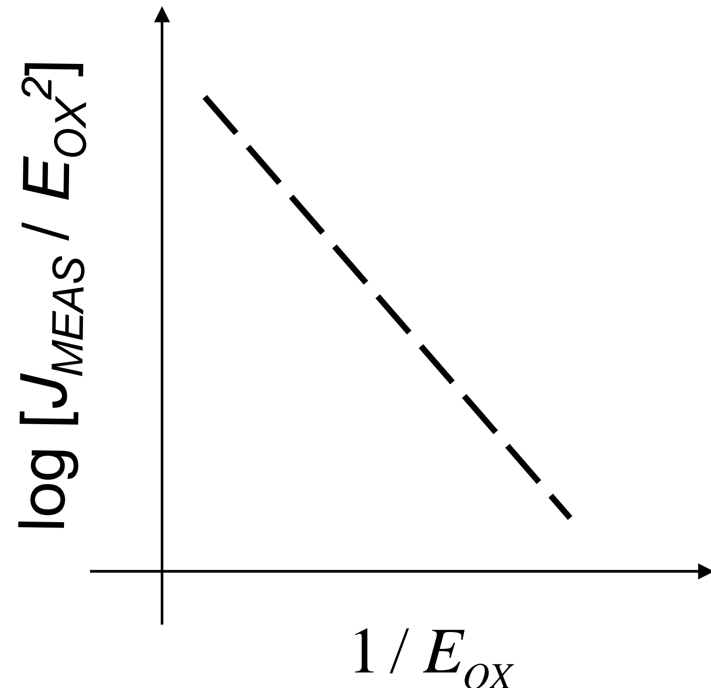
Fowler-Nordheim tunneling (ii)

$$J_{FN} = \frac{q^3 E_{OX}^2}{16\pi^2 \hbar \phi_{OX}} \exp\left[-\frac{4\sqrt{2m^*}\phi_{OX}^{3/2}}{3\hbar q E_{OX}} \right]$$ eqn. (2.209) Taur and Ning

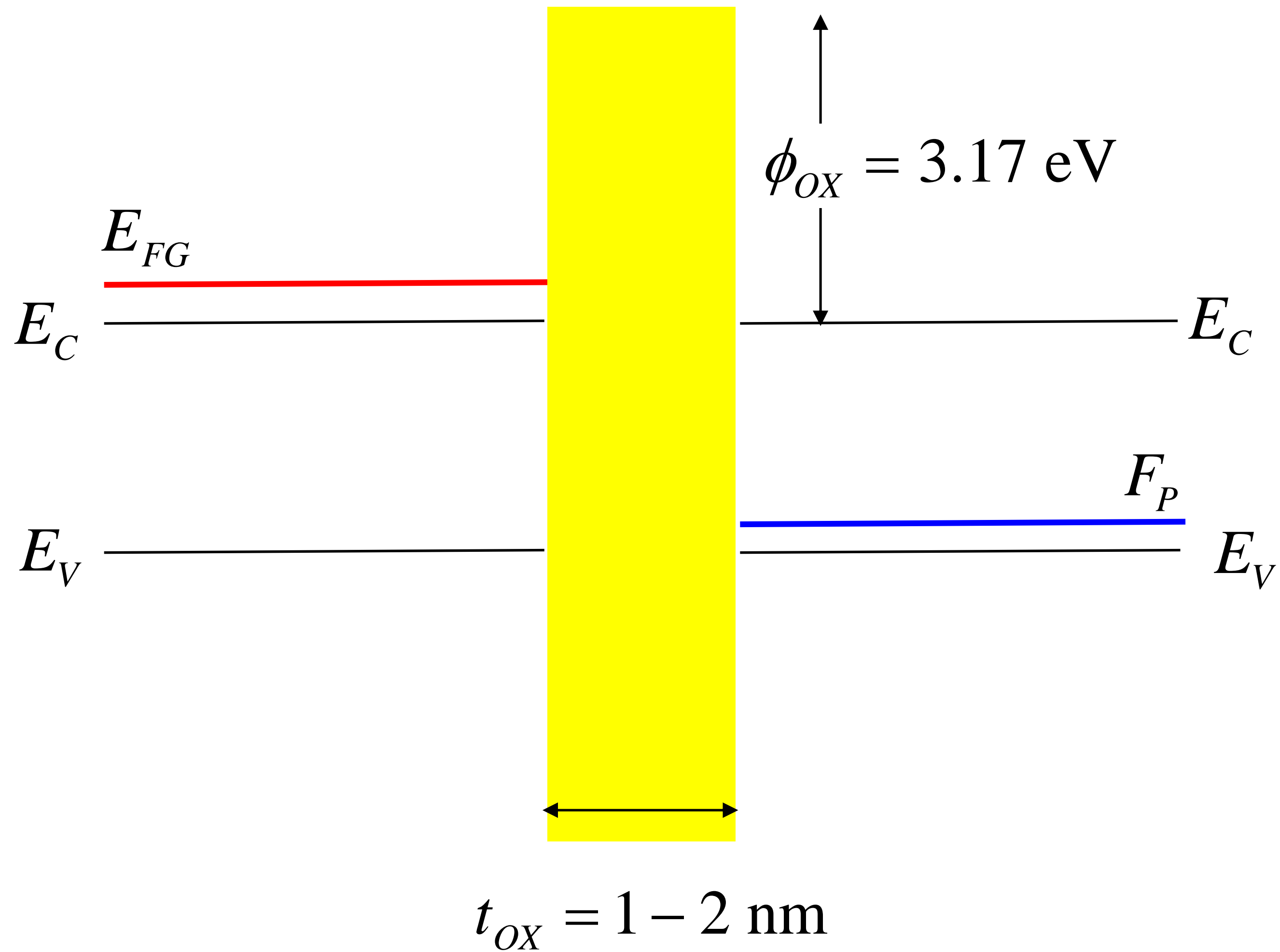
$$J_{FN} / C_1 E_{OX}^2 = \exp\left[-\frac{C_2}{E_{OX}} \right]$$

$$E_{OX} = 8 \text{ MV/cm}$$

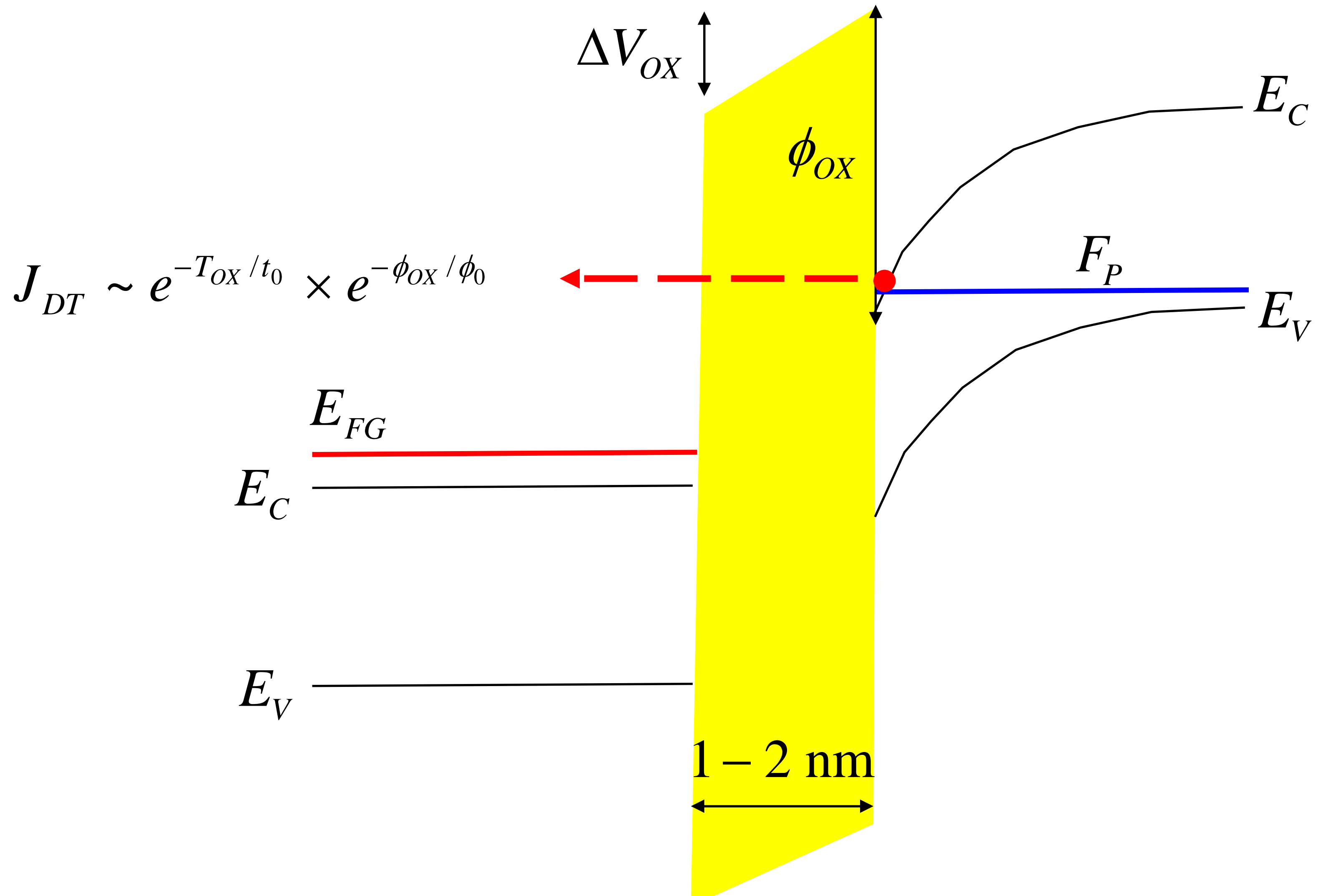
$$J_{FN} = 5 \times 10^{-7} \text{ A/cm}^2$$



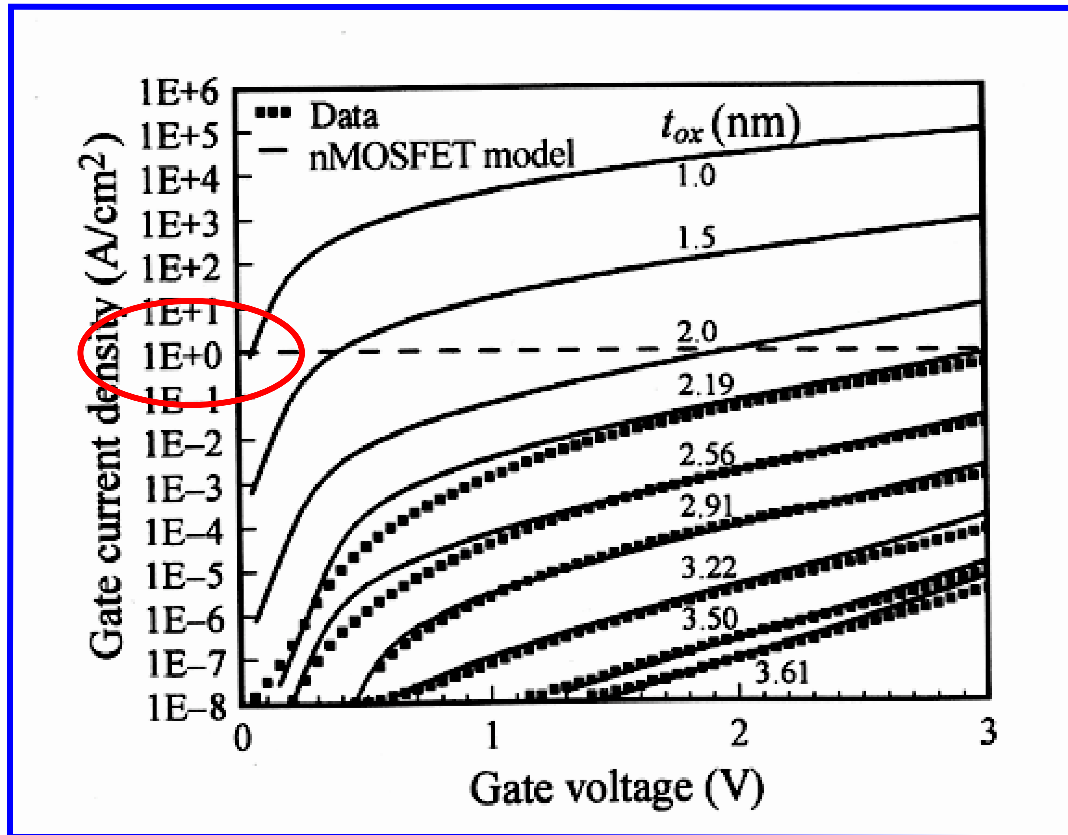
gate leakage (thin oxides)



direct tunneling



direct tunneling in practice



Lo, Buchanan, and Taur, "Modeling and characterization of quantization, polysilicon depletion, and direct tunneling effects in MOSFETs with ultrathin oxides," *IBM J. Res. Develop.*, **43**, pp. 327-337, 1999.

gate leakage at the 2008 node

is gate leakage a problem at the 2008 (59 nm) node?

$$A_{GATE} = WL_{GATE} = 1000 \text{ nm} \times 22 \text{ nm} = 2.2 \times 10^{-10} \text{ cm}^2$$

$$EOT(LSTP) = 1.6 \text{ nm} \qquad V_{DD} = 1.1 \text{ V}$$

(2007 Ed. ITRS)

$$J_G(LSTP) = 10 \text{ A/cm}^2 \quad \text{(from plot on previous slide)}$$

$$I_{GATE} \approx 2200 \, \text{pA}/\mu\text{m}$$

$$I_{SD,leak}(LSTP) = 30 \text{ pA}/\mu\text{m}$$

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ITRS 2007 Ed.

Table PIDS3a Low Standby Power Technology Requirements—Near-term Years

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
L_g: Physical gate length for LSTP [1]									
Extended Planar Bulk and DG (nm)	45	37	32	28	25	22	20	18	16
UTB FD (nm)						22	20	18	17
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	19	16	15	14	13	12	11		
UTB FD (Å)						13	12	11	10
DG (Å)						14	13	12	11
Gate Poly Depletion and Inversion-Layer Equivalent Thickness [3]									
Extended planar bulk (Å)	6.2	3.3	3.4	3.3	3.2	3.1	3.1		
UTB FD (Å)						4	4	4	4
DG (Å)						4	4	4	4
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
Extended planar bulk (Å)	25.2	19.3	18.4	17.3	16.2	15.1	14.1		
UTB FD (Å)						17	16	15	14
DG (Å)						18	17	16	15
$J_{g,limit}$: Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm^2)	6.67E-02	8.11E-02	9.38E-02	1.07E-01	1.20E-01	1.36E-01	1.50E-01		
UTB FD (A/cm^2)						1.36E-01	1.50E-01	1.67E-01	1.76E-01
DG (A/cm^2)						1.36E-01	1.50E-01	1.67E-01	1.88E-01
V_{dd}: Power Supply Voltage (V) [6]									
Extended Planar Bulk (V)	1.1	1.1	1	1	1	1	0.95		

oxide scaling

[2] EOT: for a gate dielectric of thickness Td and relative dielectric constant κ, EOT is defined by: EOT = Td / (κ /3.9), where 3.9 is the relative dielectric constant of thermal silicon dioxide.

It is projected that high-κ gate dielectric will be required by 2008 to control the gate leakage.

high-k gate dielectrics

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad C_{ins} = \frac{\varepsilon_{ins}}{t_{ins}} = \frac{\varepsilon_{ox}}{\varepsilon_{ox}}\frac{\varepsilon_{ins}}{t_{ins}} = \frac{\varepsilon_{ox}}{\left(\varepsilon_{ox} t_{ins} / \varepsilon_{ins}\right)} = \frac{\varepsilon_{ox}}{EOT}$$

$$J_{DT} \sim e^{-t_{ins}/t_0} \times e^{-\phi_{ins}/\phi_0}$$

If κ_{INS} >> κ_{OX}, then we can use a thicker t_{INS}, get a higher C_{INS}, and lower J_{DT}

high-k gate dielectrics (ii)

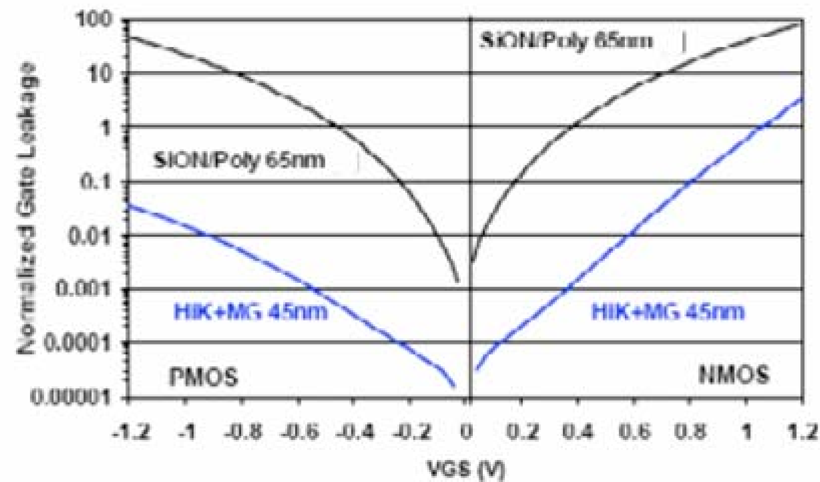

Figure 8: Gate leakage reduction of 25-1000x with use of high-k+metal gate relative to 65nm technology

"45nm High-k + Metal Gate Strain-Enhanced Transistors"

Intel Technology Journal, **12** (2), June 17, 2008

gate leakage

[5] Jg,limit is the maximum allowed gate leakage current density at 25C, and it is measured with the gate biased to Vdd and the source, drain, and substrate all set to ground.

SiO_2 --> SiON

total leakage

[8] **Isd,leak**: subthreshold leakage current is defined as the NMOSFET source current per micron of device width, at 25C, with the drain bias set equal to Vdd and with the gate, source, and substrate biases set to zero volts.

Total NMOS off-state leakage current (Ioff) is the sum of the NMOS subthreshold, gate, and junction leakage current (which includes band-to-band tunneling and gate induced drain leakage [GIDL]) components).

For LSTP, meeting the Isd,leak target of ~30pA/μm is the key scaling goal.

total leakage; 2008

LSTP Isd, leak target: 30pA/μm

LSTP, junction leakage target: 10pA/μm

LSTP, gate leakage target: 8.1e-02 A/cm^2

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leakage challenges

1) Gate leakage has become a major problem because of t_{ox} scaling and is leading to the replacement of SiO_2.

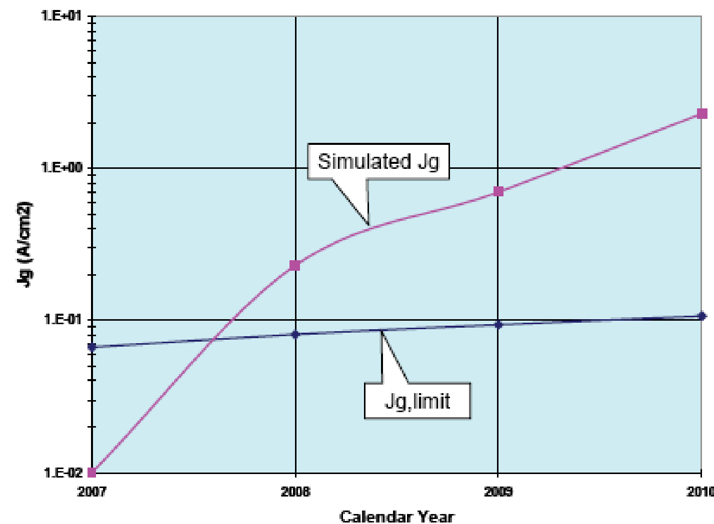

Figure PIDS3 LSTP: $J_{g,limit}$ versus Simulated Gate Leakage Current Density for SiON Gate Dielectric

(2007 Ed. ITRS, PIDS Chapter)

leakage challenges

1) Gate leakage has become a major problem because of t_{ox} scaling and is leading to the replacement of SiO_2.

2) Band-to-band tunneling (and GIDL) are also concerns.

3) And don't forget about the sunthreshold channel current!