EE-612:
Lecture 17:
Gate resistance and Interconnects

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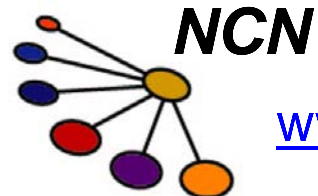

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outline

1) Gate Resistance

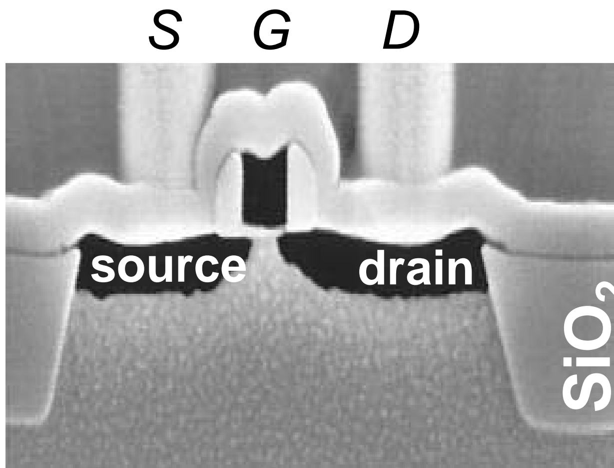
2) Interconnects

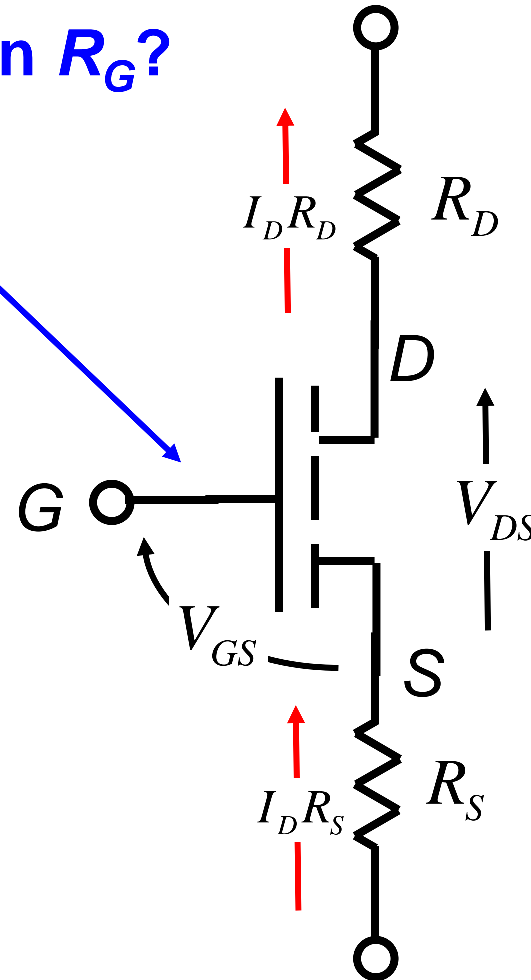
3) ITRS

4) Summary

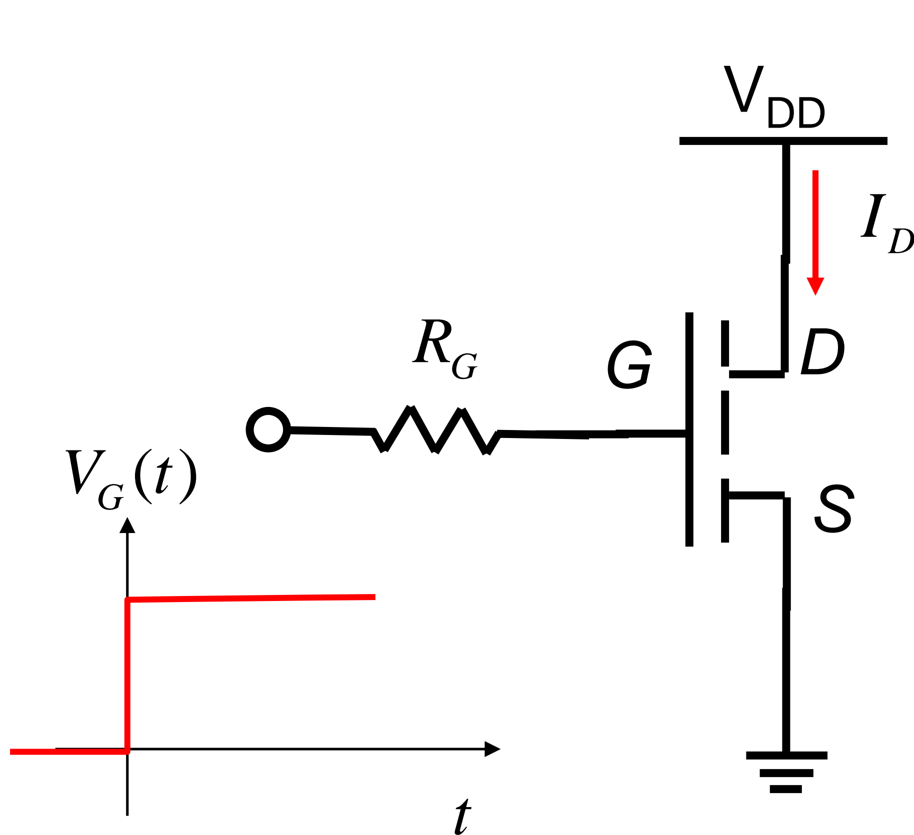
review: parasitic series R

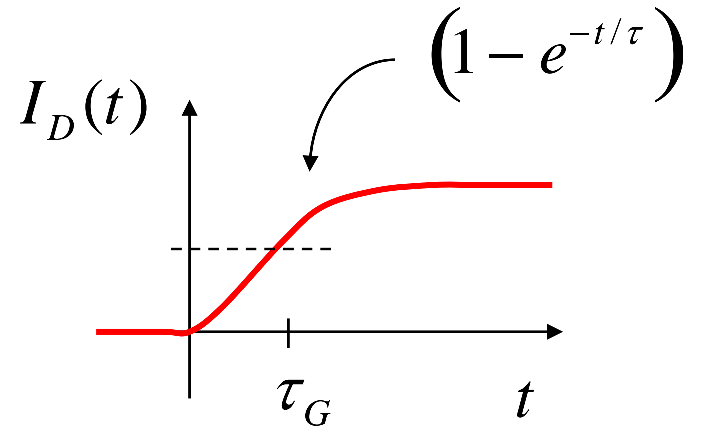
Why did we not consider an R_G?





effect of a gate resistance (AC)



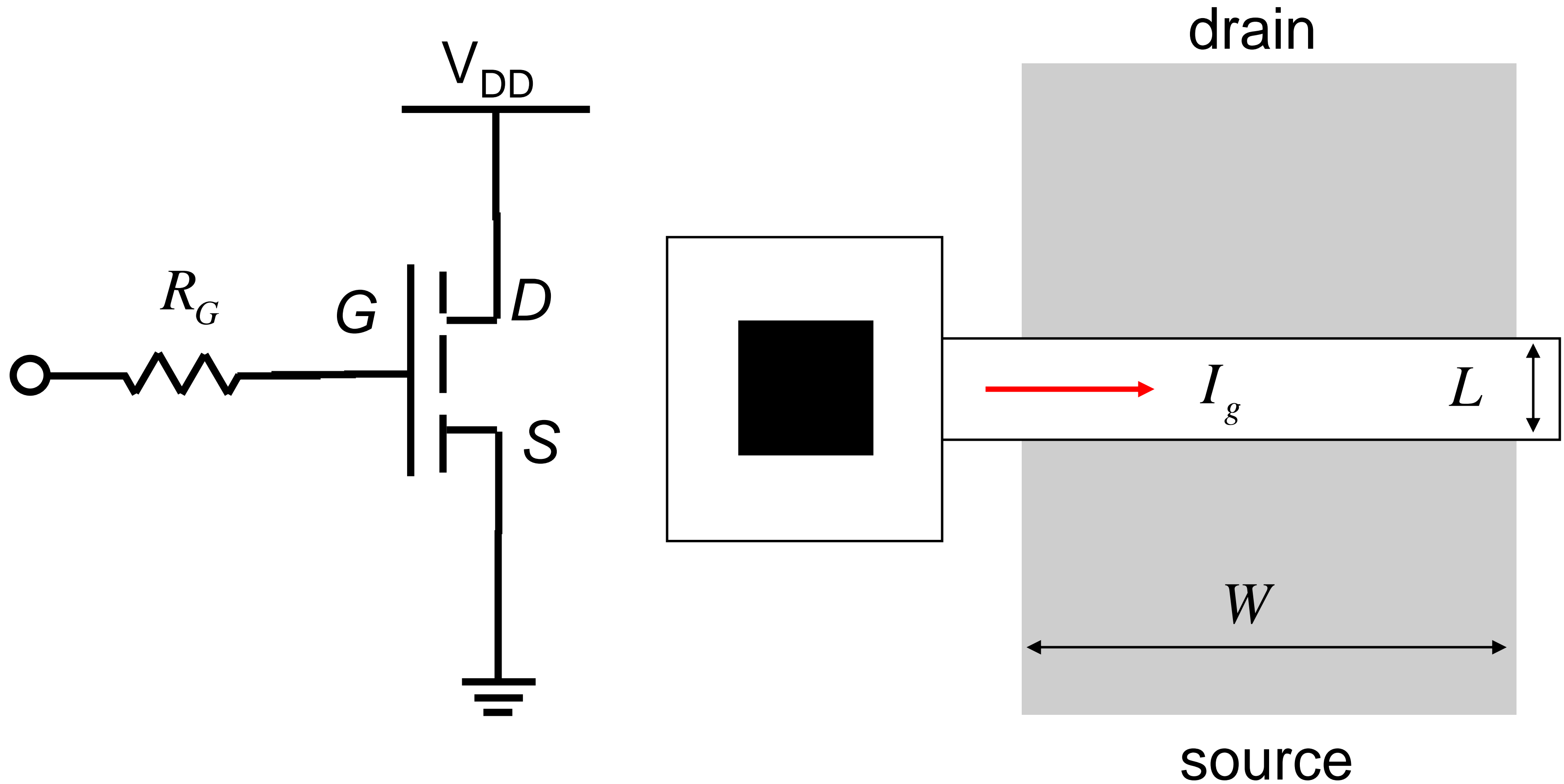


$$\tau = R_G C_G$$

$$0.5 = \left(1 - e^{-\tau_G/\tau}\right)$$

$$\tau_G = 0.69\, R_G C_G$$

gate resistance



gate resistance (ii)

$$R_G = \rho_G \frac{W}{L}$$

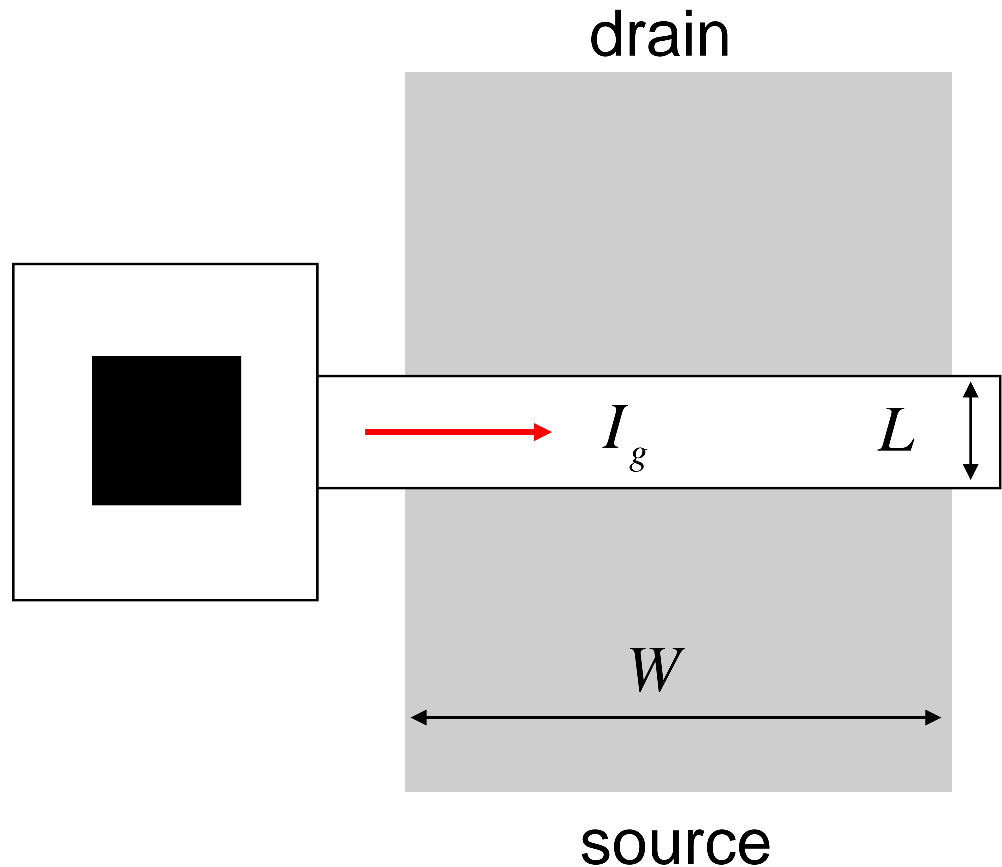
$$R_G = \left(\frac{\rho_G}{L}\right) W = R_L W$$

Ω / cm

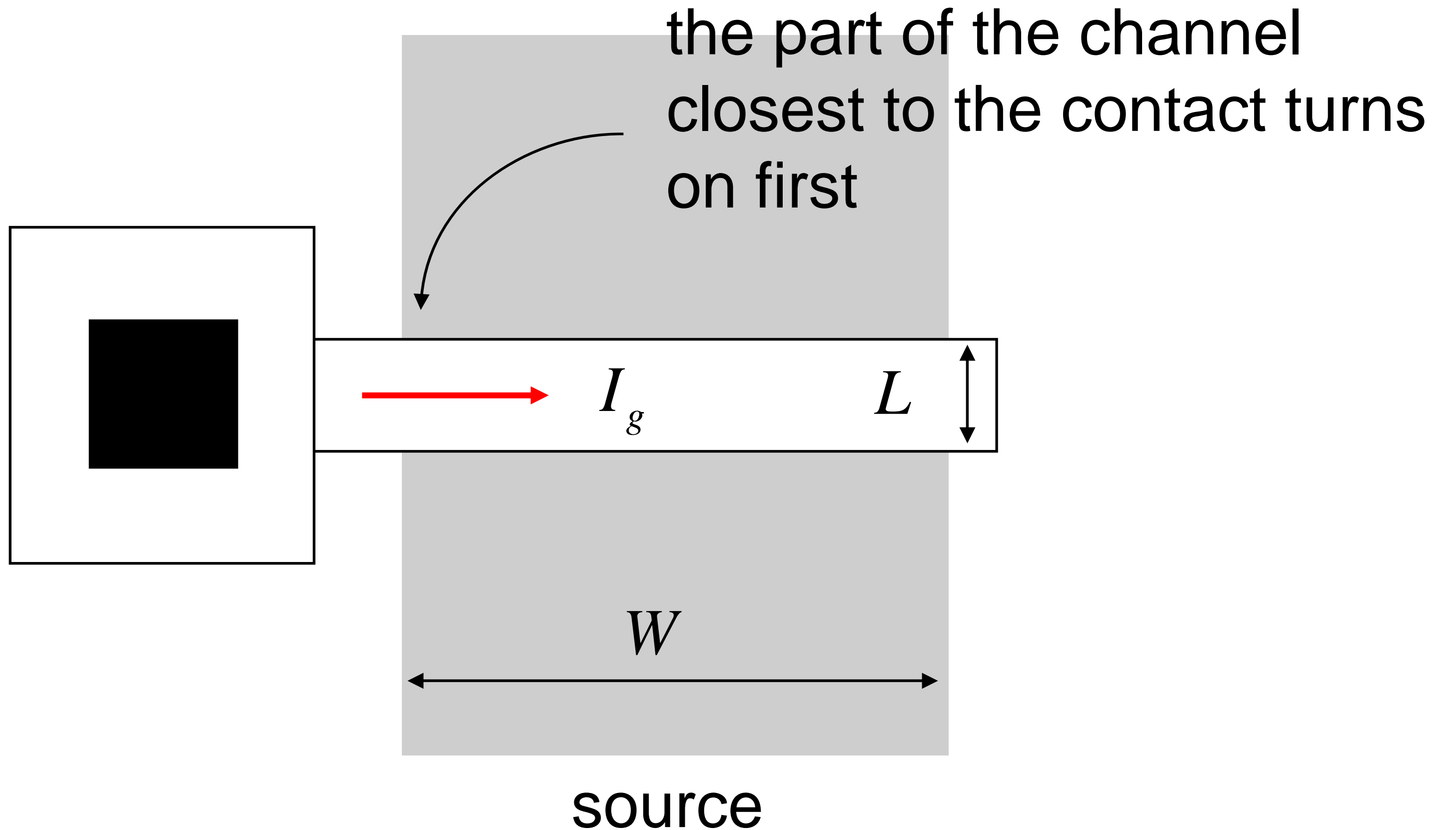
$$C_G = C_{ox} L W$$

$$C_G = \left(C_{ox} L\right) W = C_L W$$

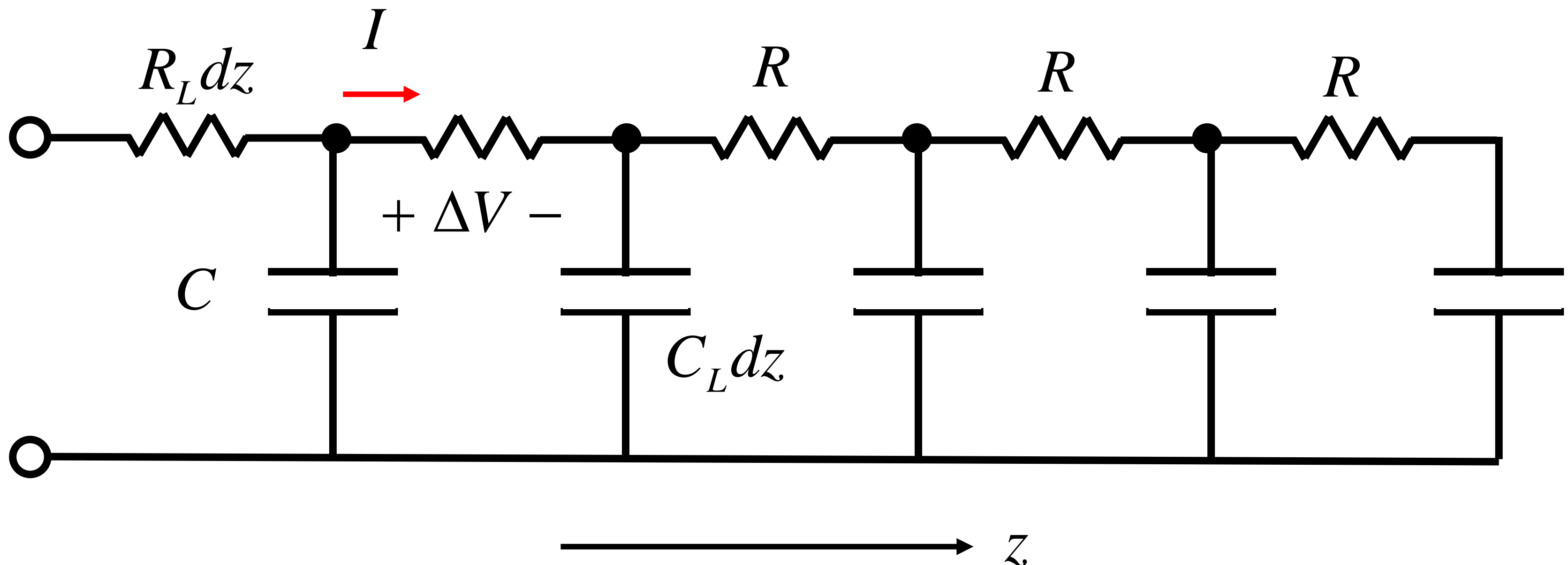
F / cm



distributed gate resistance



distributed gate resistance (ii)

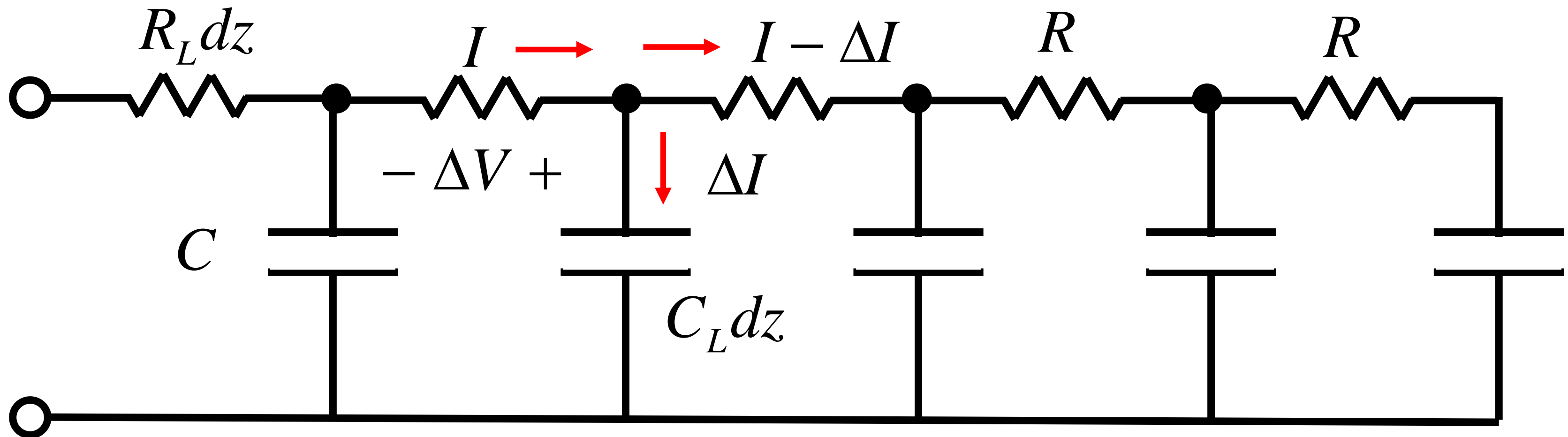


$$\Delta V = I\, R_L dz$$

$$\frac{\Delta V}{dz} = -\frac{\partial V}{\partial z} = I\, R_L$$

$$\frac{\partial V}{\partial z} = -I\, R_L \qquad (1)$$

distributed gate resistance (iii)



$$\Delta I = C_L dz \frac{\partial V}{\partial t}$$

$$\frac{\Delta I}{dz} = -\frac{\partial I}{\partial z} = C_L \frac{\partial V}{\partial t}$$

$$\frac{\partial I}{\partial z} = -C_L \frac{\partial V}{\partial t} \qquad (2)$$

distributed gate resistance (iv)

$$\frac{\partial V}{\partial z} = -I\,R_L \qquad (1)$$

$$\frac{\partial I}{\partial z} = -\,C_L \frac{\partial V}{\partial t} \qquad (2)$$

$$\frac{\partial^2 V}{\partial z^2} = -\,R_L \frac{\partial I}{\partial z}$$

$$\frac{\partial^2 V}{\partial z^2} = R_L C_L \frac{\partial V}{\partial t}$$

$$\frac{\partial V(z,t)}{\partial t} = \frac{1}{R_L C_L} \frac{\partial^2 V(z,t)}{\partial z^2}$$

distributed gate resistance (v)

recall: $$\frac{\partial n(z,t)}{\partial t} = D_n \frac{\partial^2 n(z,t)}{\partial z^2}$$

"minority carrier diffusion equation"

$$\frac{\partial V(z,t)}{\partial t} = \frac{1}{R_L C_L} \frac{\partial^2 V(z,t)}{\partial z^2} = D_{eff} \frac{\partial^2 V(z,t)}{\partial z^2}$$

$$D_{eff} = \frac{1}{R_L C_L}$$

units: $$\frac{1}{\Omega/\mathrm{cm} \times \mathrm{F/cm}} = \frac{\mathrm{cm}^2}{\mathrm{V/A} \times \mathrm{C/V}} = \frac{\mathrm{cm}^2}{\mathrm{C/A}} = \frac{\mathrm{cm}^2}{\mathrm{sec}}$$

distributed gate resistance (iv)

recall: $\tau_B = W_B^2 / 2D_n$ "base transit time"

$$\tau_g = 0.5 R_L C_L W^2$$

distributed gate resistance and scaling

$$\tau_g = 0.5 R_L C_L W^2$$

$$R_L = \rho_G / L$$

$$C_L = C_{ox} L$$

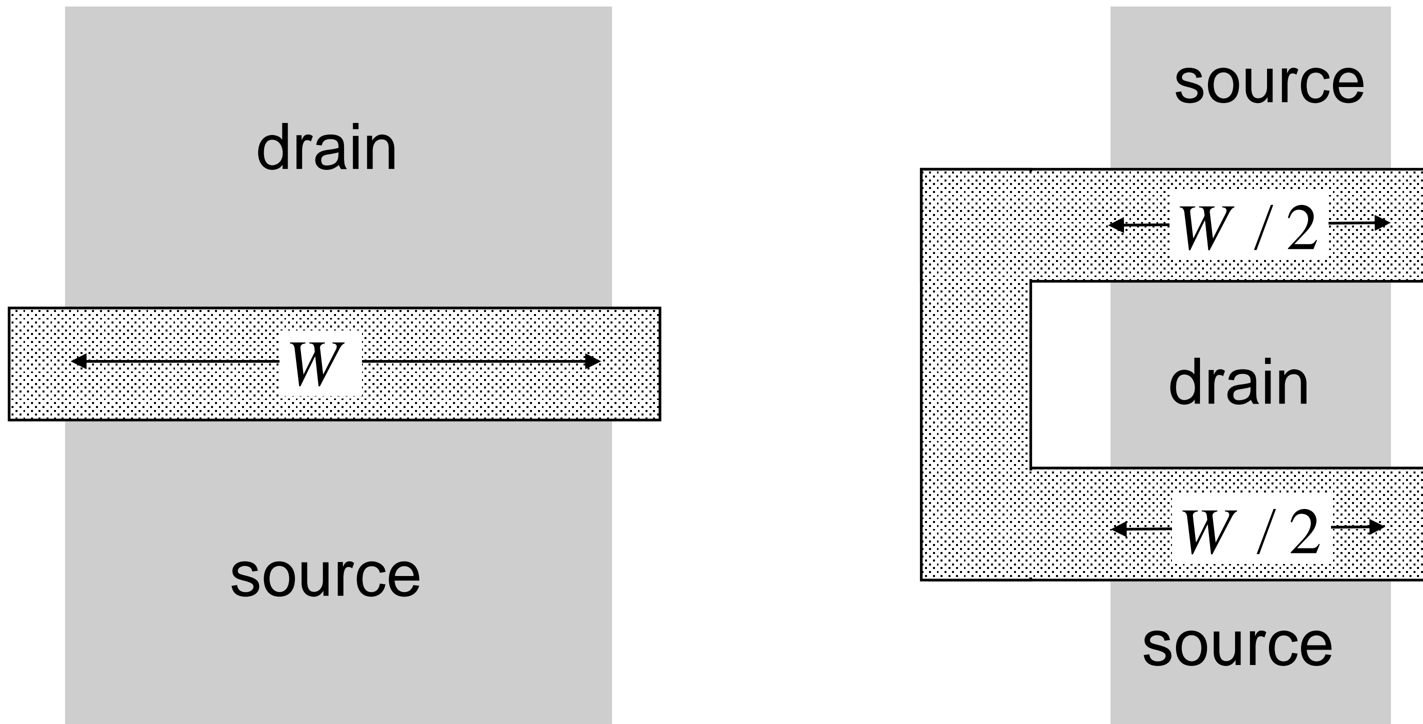
$\rho_G \sim 2 - 10$ ž /sq.

$$\tau_g = 0.5 \rho_G C_{ox} W^2$$

device delay:

$$\tau \rightarrow \tau / \kappa$$

‘folded’ layout

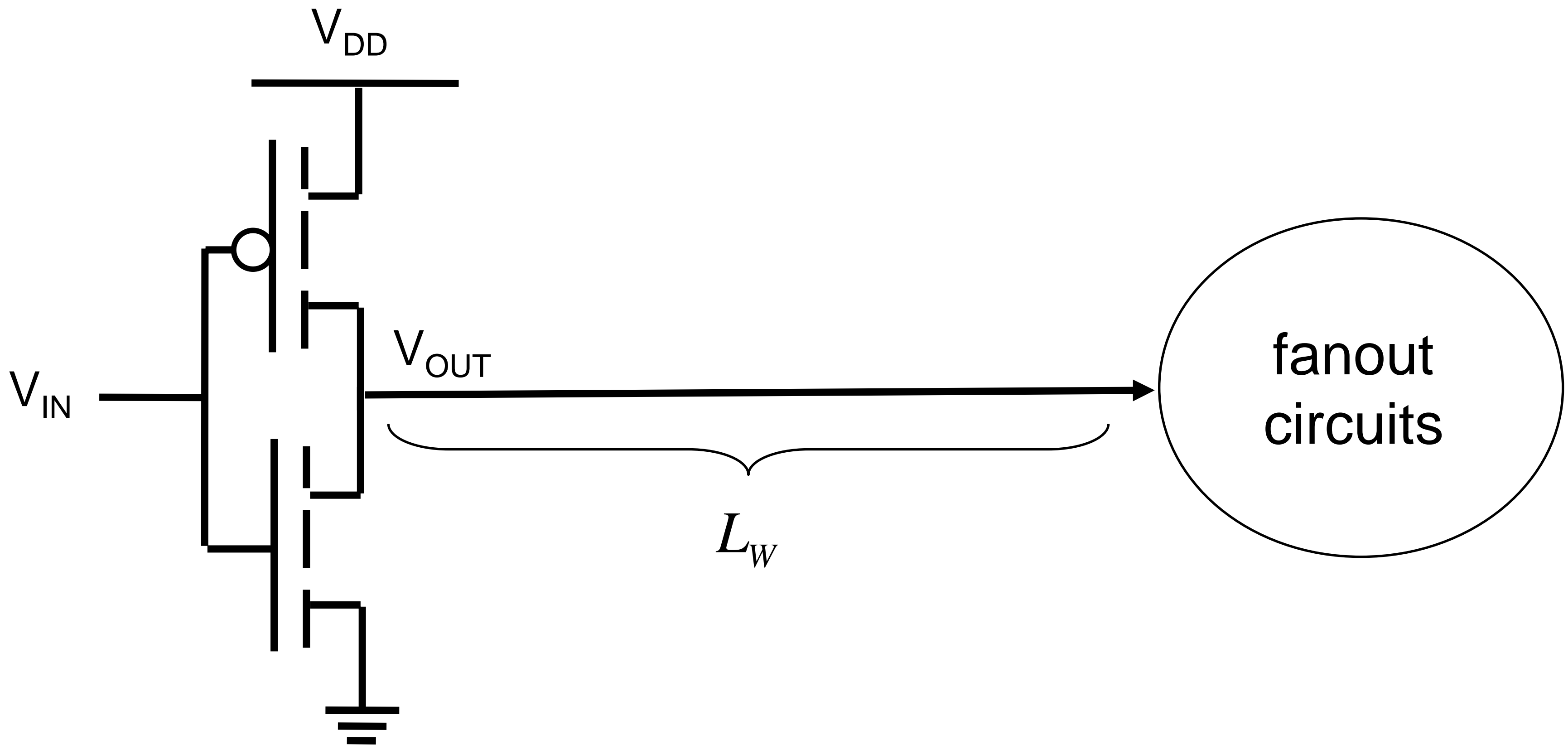


see Taur and Ning, Fig. 5.11

outline

1) Gate Resistance
2) **Interconnects**
3) ITRS
4) Summary

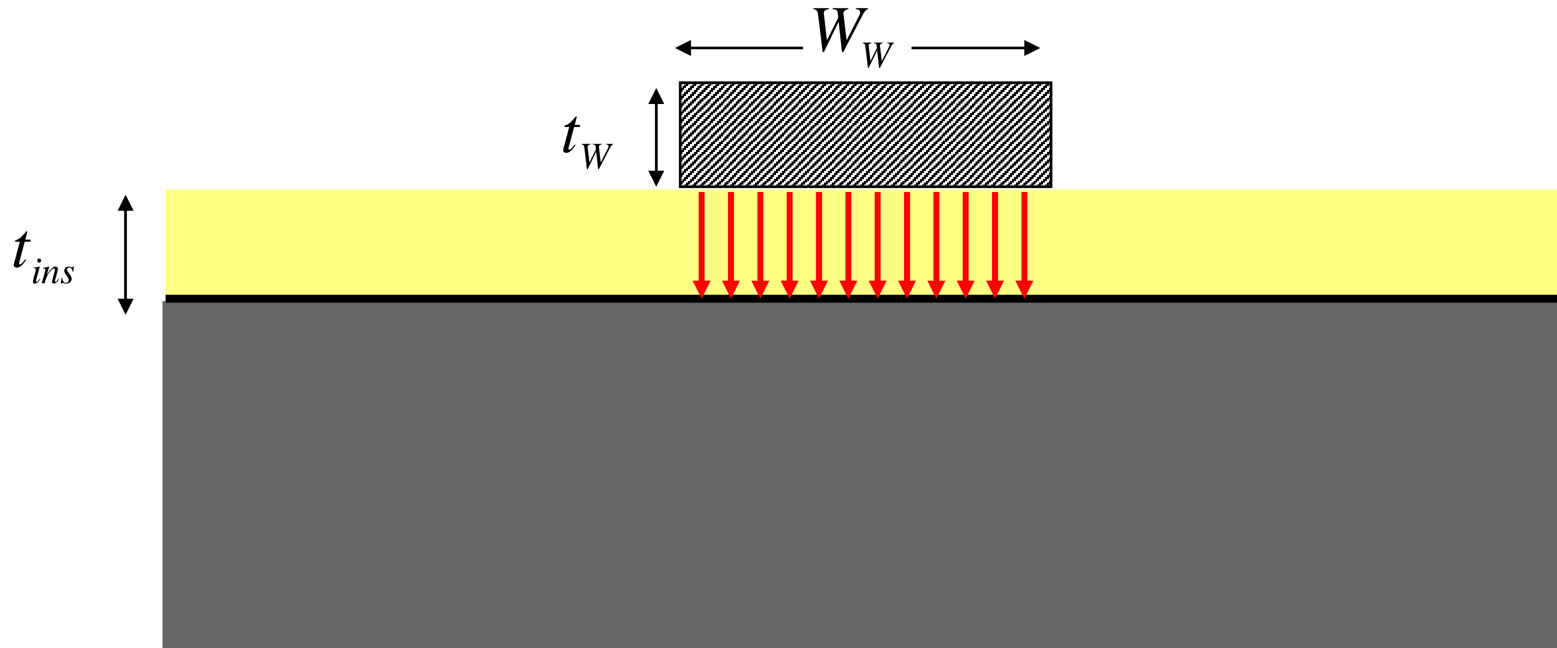
interconnects



interconnect capacitance

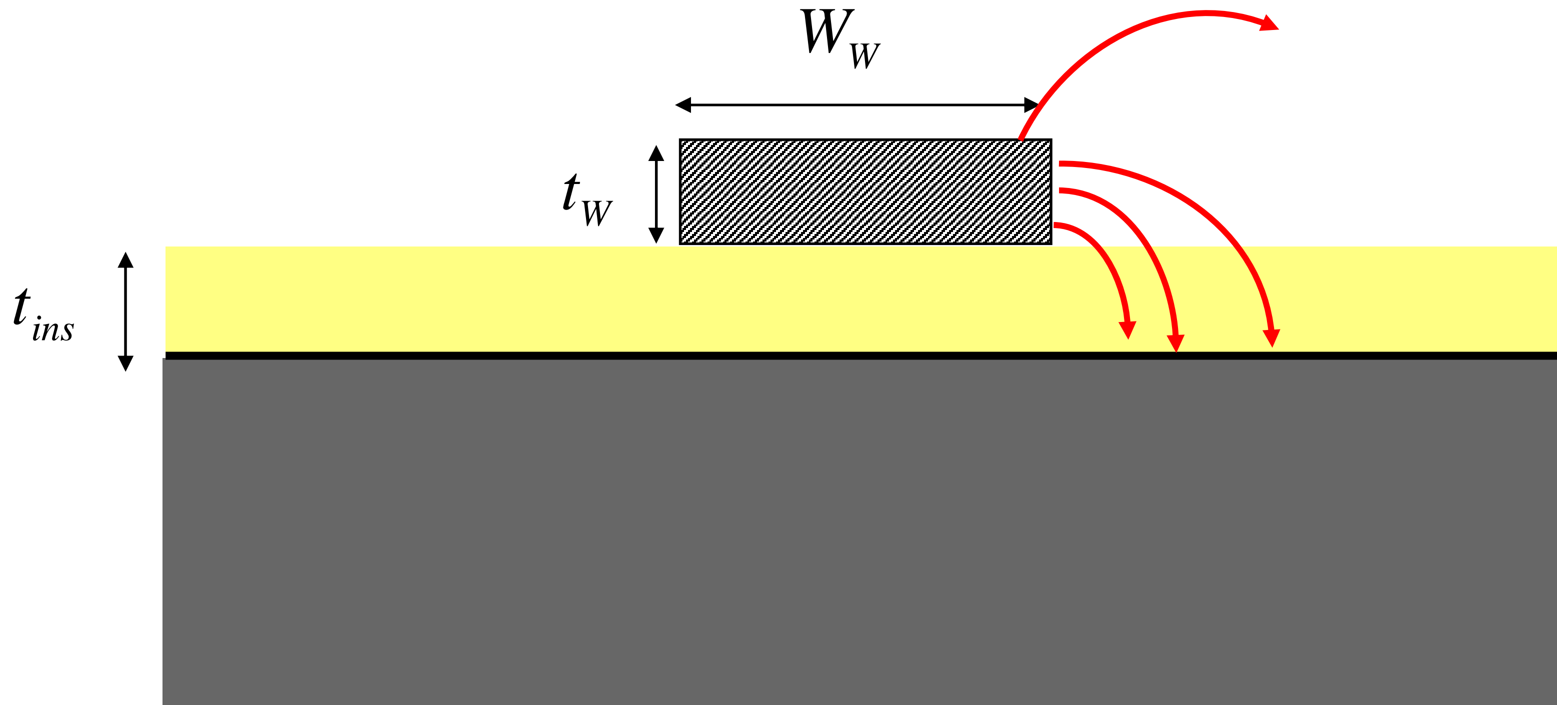
$$C_{Wire} = C_{ins} W_w L_w \qquad C_{ins} = \varepsilon_{ins} / t_{ins}$$

$$C_{Wire} = \left(C_{ins} W_w\right) L_w = C_W \left(\mathrm{PP}\right) L_W$$

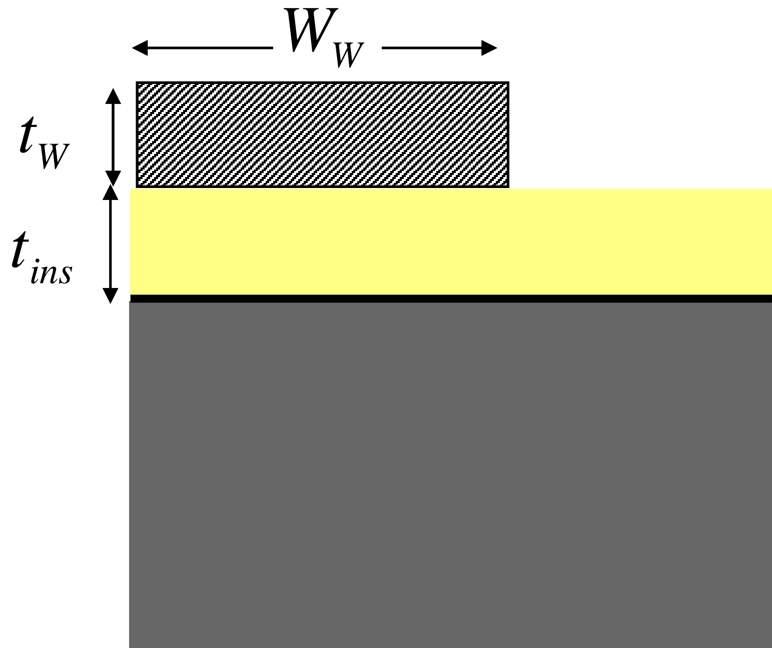


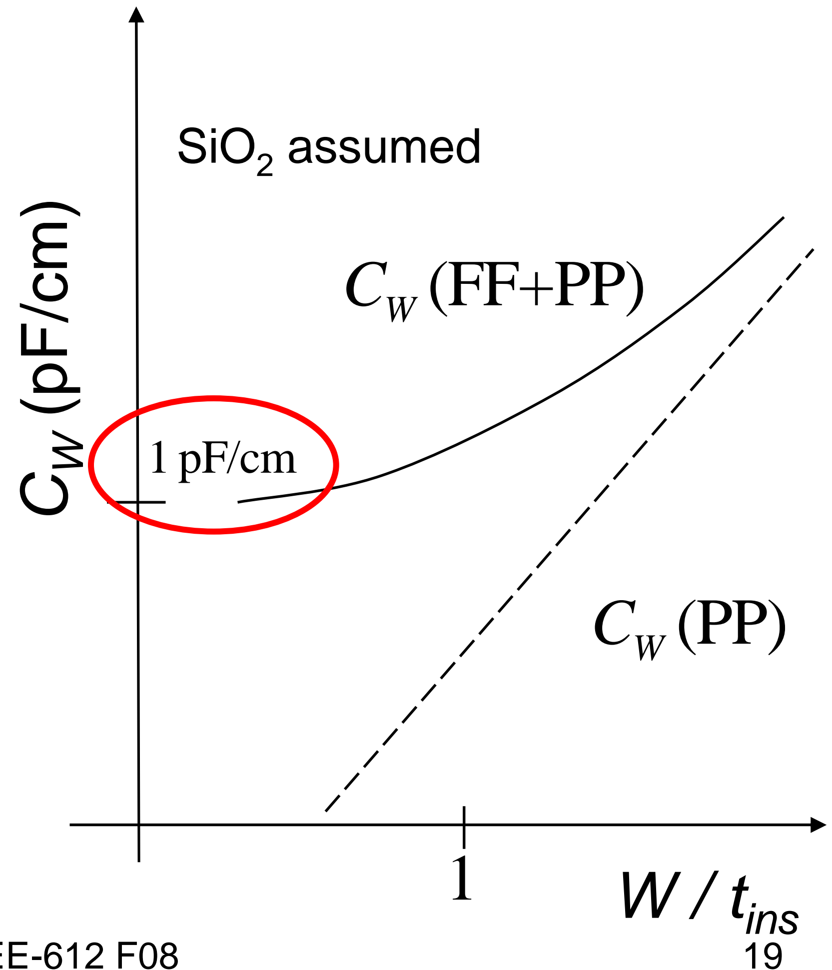
interconnect capacitance (ii)

$$C_{Wire} = \left[C_W(\text{PP}) + C_W(\text{FF}) \right] L_W$$



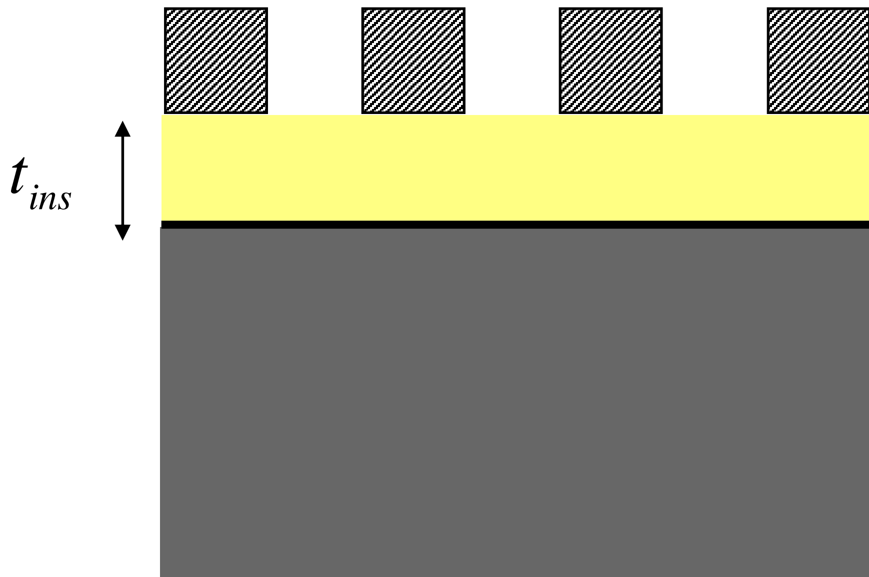
interconnect capacitance (iii)





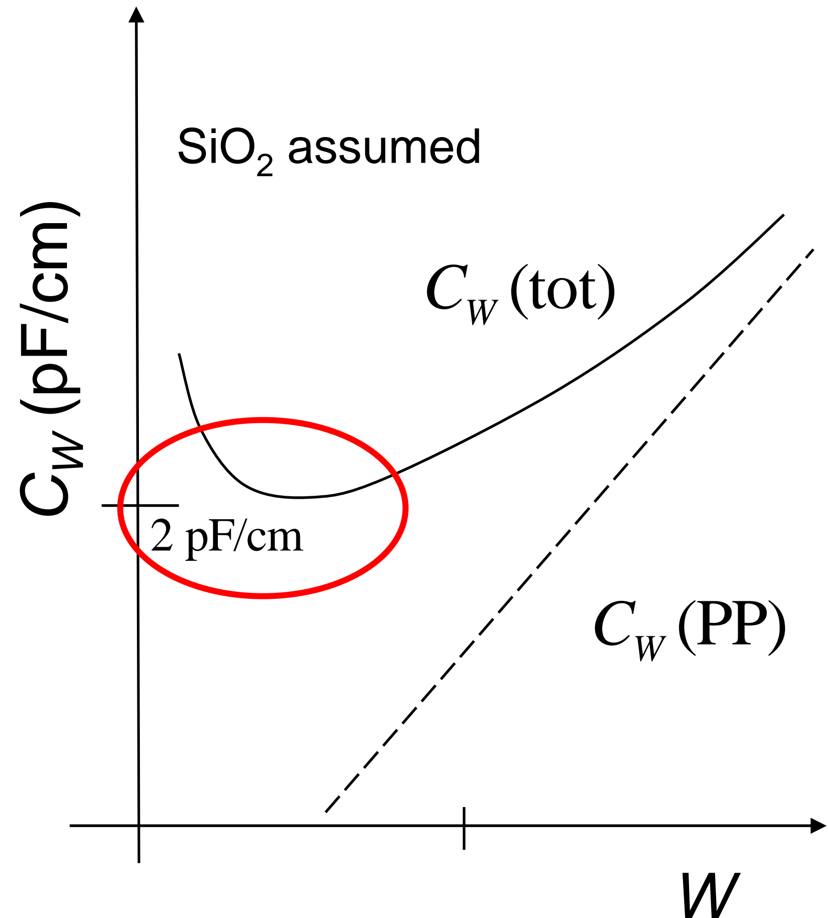
(see Fig. 5.21, Taur and Ning)

wire-wire capacitance

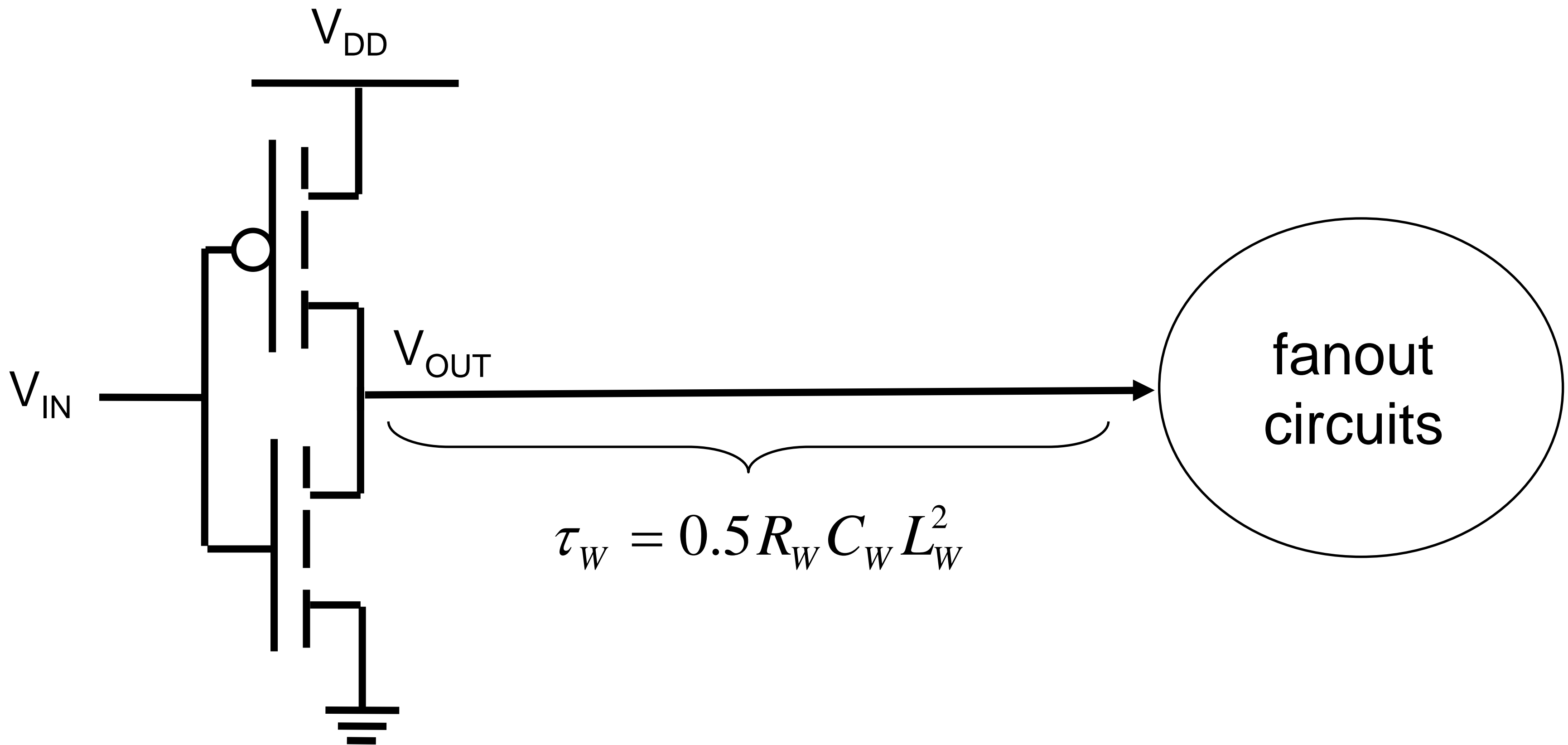


$$C_{Wire} = \left[C_W(\text{PP}) + C_W(\text{FF}) + C(\text{WW}) \right] L_W$$

(see Fig. 5.22, Taur and Ning)



interconnect delay



interconnect scaling

$$\tau_W = 0.5 R_W C_W L_W^2$$

$$C_W = C_W(\text{PP}) + C_W(\text{FF}) + C_W(\text{WW})$$

$$R_W = \frac{\rho_W}{W_w t_w}$$

$$\rho_{Al} \approx 3 \times 10^{-6}\ \Omega\text{-cm}$$

$$\rho_{Cu} \approx \rho_{Al} / 1.5$$

scaling by factor, $\kappa > 1$

$$C_W = C_{ins} W_w + C_W(\text{FF}) \rightarrow C_W$$

$$R_W = \rho_W / \left(W_w t_w\right) \rightarrow \kappa^2 R_W$$

$$J_W = I / \left(W_w t_w\right) \rightarrow \kappa J_W \ (\text{A/cm}^2)$$ (electromigration)

$$\tau_W = 0.5 R_W C_W L_W^2 \rightarrow \tau_W$$ (device τ is decreasing)

local interconnects

$$L_W \to L_W / \kappa \qquad \tau_W = 0.5 R_W C_W L_W^2 \to \tau_W$$

Is this an issue? Assume:

$$C_W \approx 2\pi \varepsilon_{ins} \quad \text{F/cm}$$ Eqn. (5.27) Taur and Ning

$$\tau_W \approx \pi \varepsilon_{ins} \rho_w \frac{L_W^2}{W_w t_w} \approx \left(3 \times 10^{-18} \text{ s}\right) \frac{L_W^2}{W_w t_w}$$ Eqn. (5.29) (5.30)

for $W_w = t_w = 0.25\ \mu\text{m}$ and $L_W = 100\,\mu\text{m}$, $\tau_W = 0.5\text{ps}$

for a 0.25 micron technology, an inverter delay is ~ 20 ps

local interconnect delays are not an issue

global interconnects

$L_W \to L_W$ (approximately the size of the chip)

$\tau_W = 0.5 R_W C_W L_W^2 \to \kappa^2 \tau_W$

Is this an issue?

for a 0.25 micron technology:

$$\tau_W \approx \pi \varepsilon_{ins} \rho_w \frac{L_W^2}{W_w t_w} \approx \left(3 \times 10^{-18}\ \text{s}\right) \frac{L_W^2}{W_w t_w} \approx 1\ \text{ns}$$

$$\tau_W >> \tau_{Gate} >> \tau_{Device}$$

global interconnect delays are a very big issue

global interconnect scaling solutions

$$\tau_W = 0.5 R_W C_W L_W^2$$

$$C_W = C_W(\mathrm{PP}) + C_W(\mathrm{FF}) + C_W(\mathrm{WW})$$

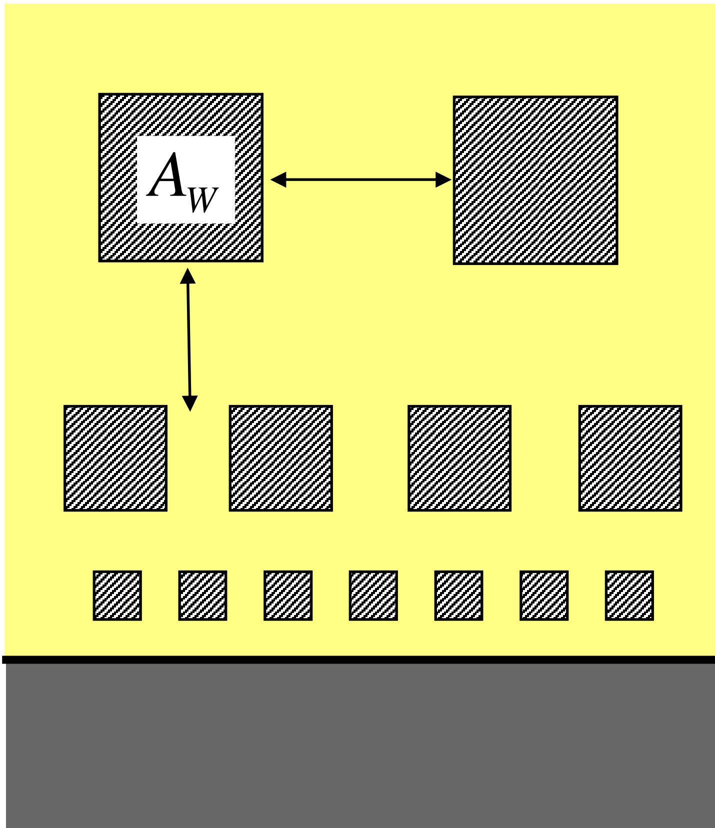
(low-k dielectrics)

$$R_W = \frac{\rho_W}{W_w t_w}$$

1) switch from Al metal to Cu $\rho_{Cu} \approx \rho_{Al}/1.5$

2) increase cross-sectional area $A_W = W_w t_w$

wiring hierarchy



after Fig. 5.24, Taur and Ning

$$\tau_W = 0.5 R_W C_W L_W^2$$

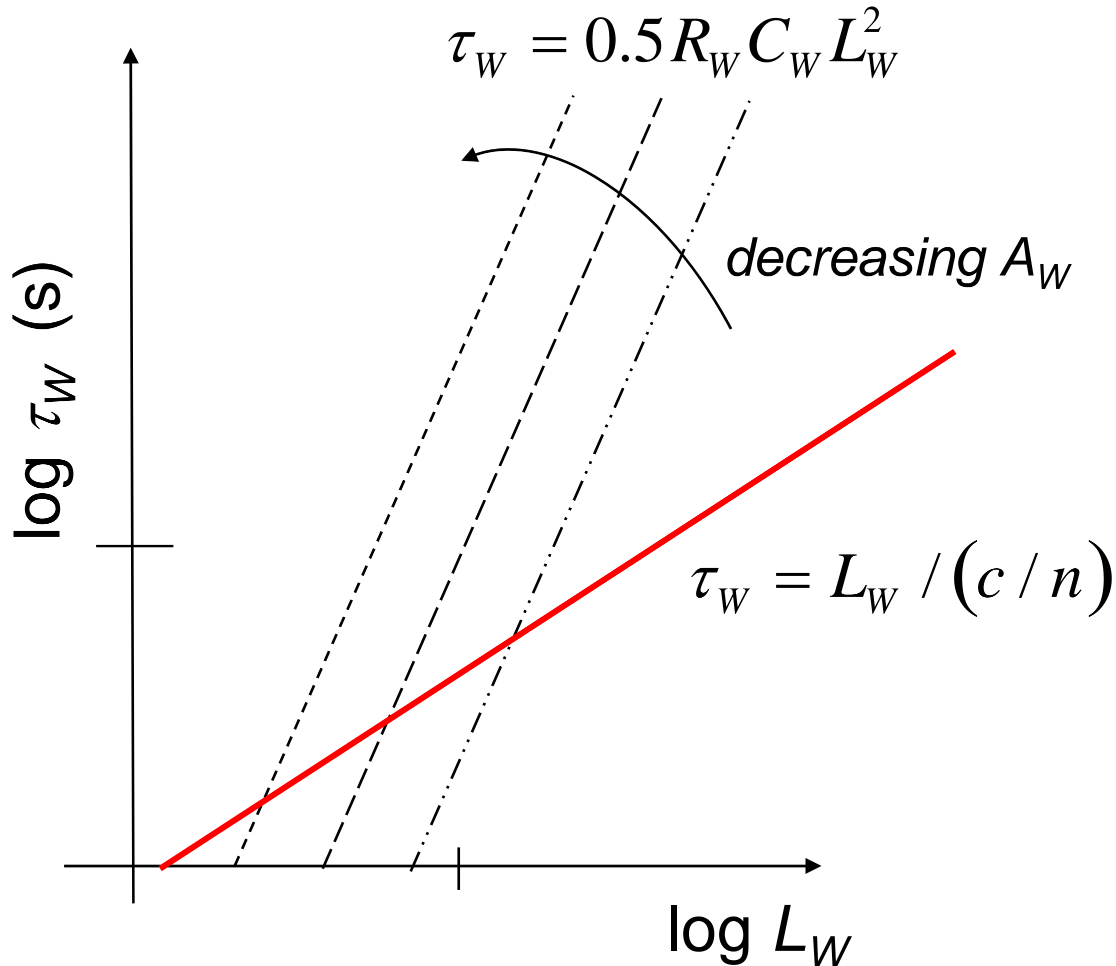
$$\tau_W = \frac{L_W}{2 / R_W C_W L_W}$$

$$\tau_W = \frac{L_W}{\upsilon_{Diff}}$$

$$\upsilon_{Diff} = 2 D_{eff} / L_W$$

velocity that signal diffuses down the *RC* transmission line

inductance



$$\tau_W = L_W / \upsilon_{Signal}$$

RC line:

$$\upsilon_{Signal} = 2D_{eff} / L_W$$

RLC line:

$$\upsilon_{Signal} < c / n$$

outline

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copper resistivity trends

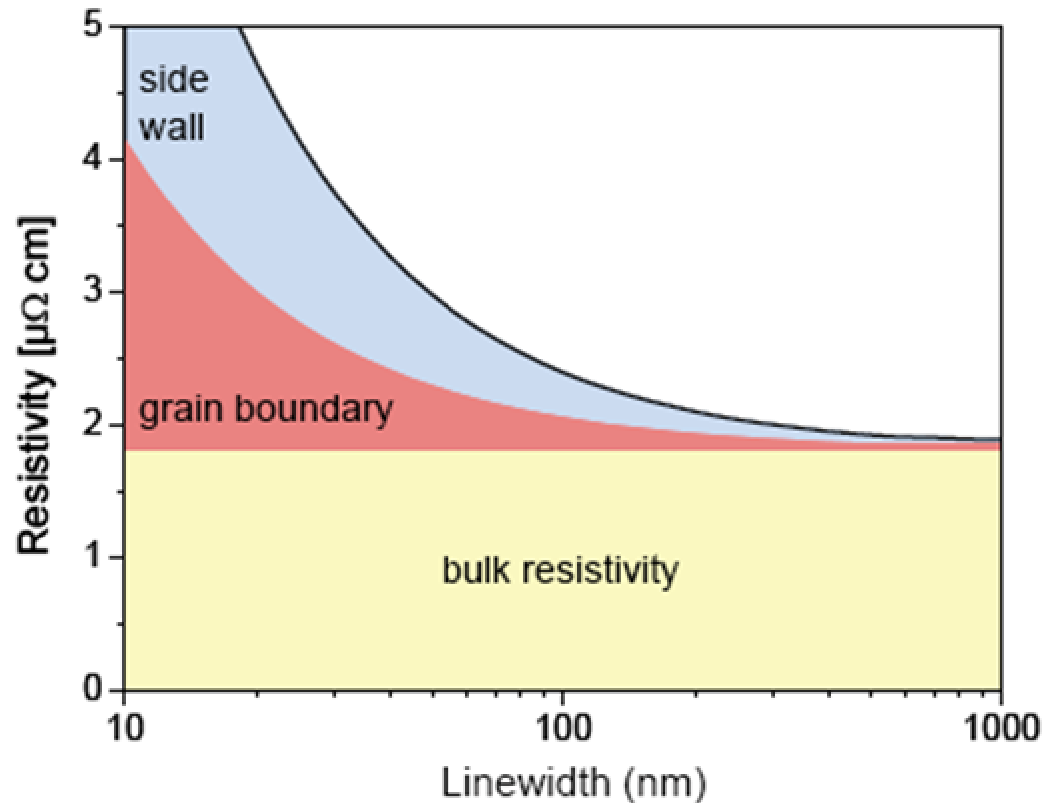


Figure INTC1 Cu Resistivity

ITRS (2007 edition)

hierarchical wiring

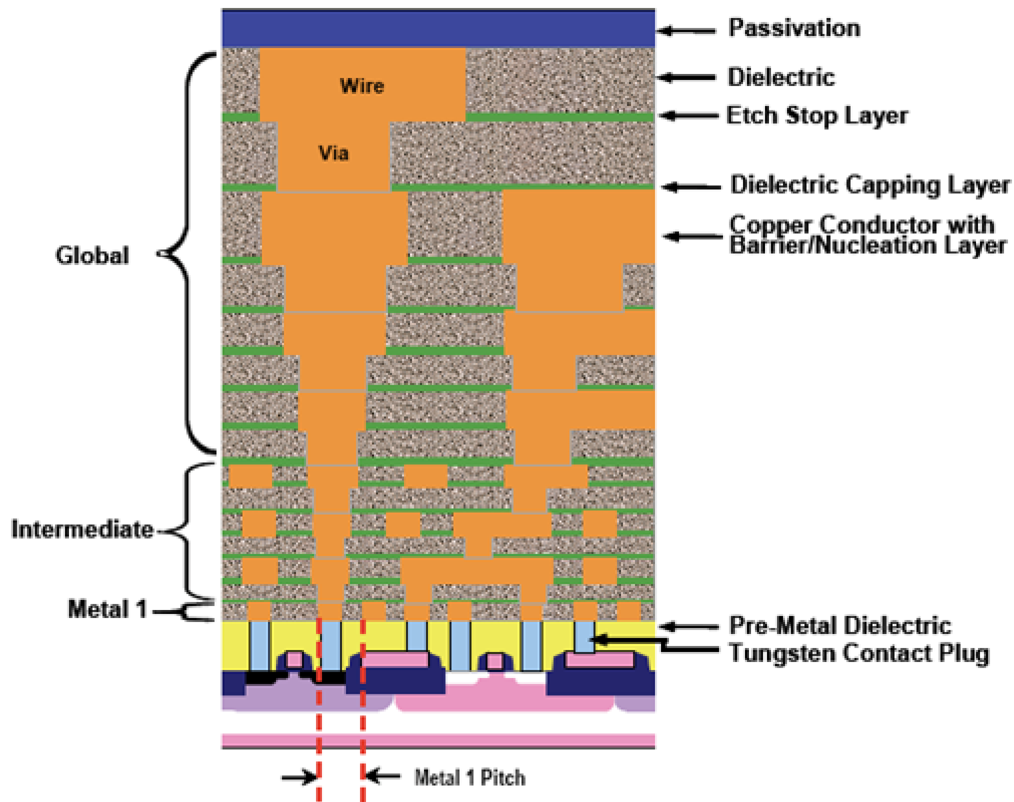


Figure INTC2 Cross-section of Hierarchical Scaling—MPU Device

ITRS (2007 edition)

2008 node

12 layers

$2.9 < k < 3.3$

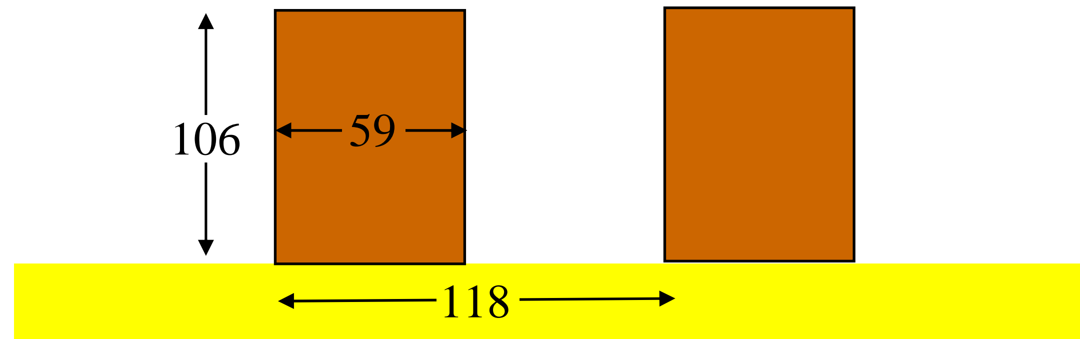
Tot length (1-5) =1.7 km

$\rho = 3.6\ \mu\Omega\text{-cm}$

$J_{MAX} = 1.2 \times 10^{6}\ \text{A/cm}^{2}$

metal 1 (2008 node)

Metal 1 pitch:	118 nm
Metal 1 A/R:	1.8
C_L	1.9 - 2.1 pF/cm
R_L variability	29%
τ_W for L_W = 1mm metal 1:	1183 ps
L_W for τ = RC delay (0.6ps)	27 μm



ITRS (2007 edition)

interconnect trends

The increasing RC delay is one of the most crucial parameters especially for high performance products. While **scaled wires in the local and intermediate wiring levels are less critical** and show only a moderate increase in RC, the fixed length interconnects in the **semiglobal and global wiring levels are much more sensitive** and need the introduction of repeating inverters to keep the RC delay within viable limits. However, the introduction of these repeaters requires additional chip area and increases the power consumption.

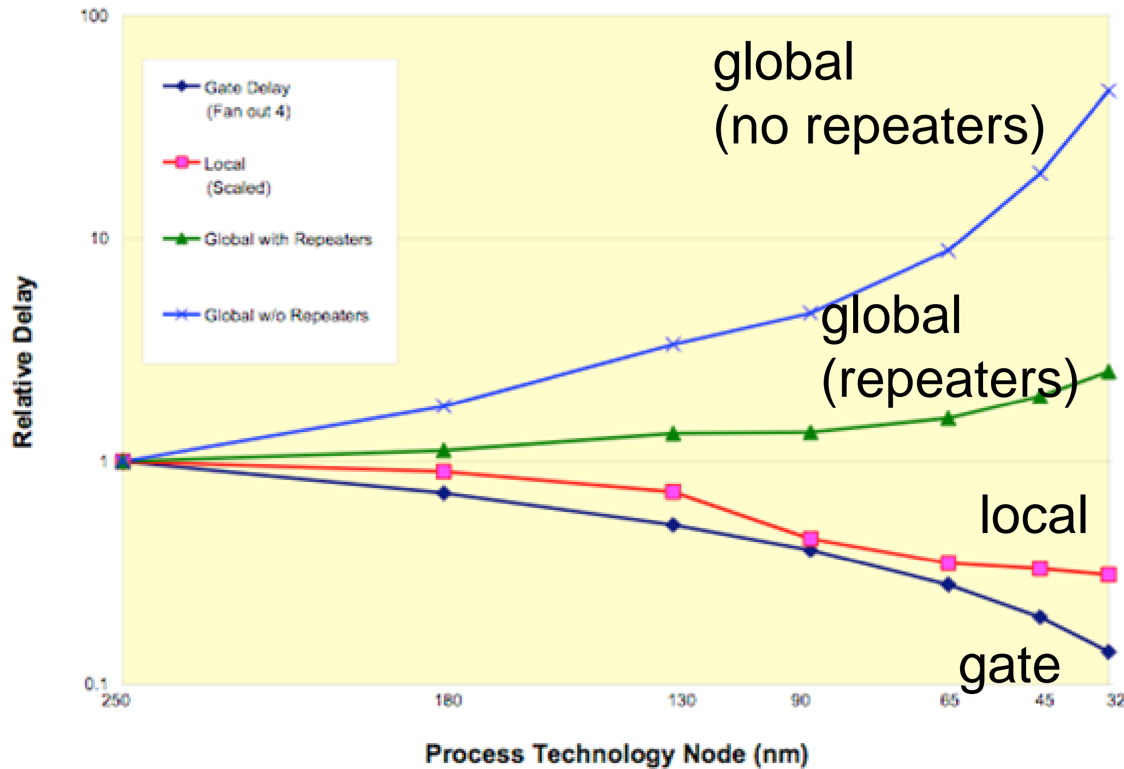
1 micron Al/SiO_2:	
device delay:	20 ps
1 mm line delay:	1 ps

35nm Cu/low k:	
device delay:	1 ps
1 mm line delay:	250 ps

Al --> Cu / low-k / interconnect centric design

ITRS (2007 edition)

interconnects trends



ITRS (2005 edition)

outline

1) Gate Resistance
2) Interconnects
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summary

1) Interconnect delays (and power) have become major issues because of transistor scaling.
2) Copper, low-k, and improved design have helped.
3) In the future, we may need new materials (carbon nanotubes? optical interconnects?) and better design techniques.