EE-612:
Lecture 22:

CMOS Circuit Essentials

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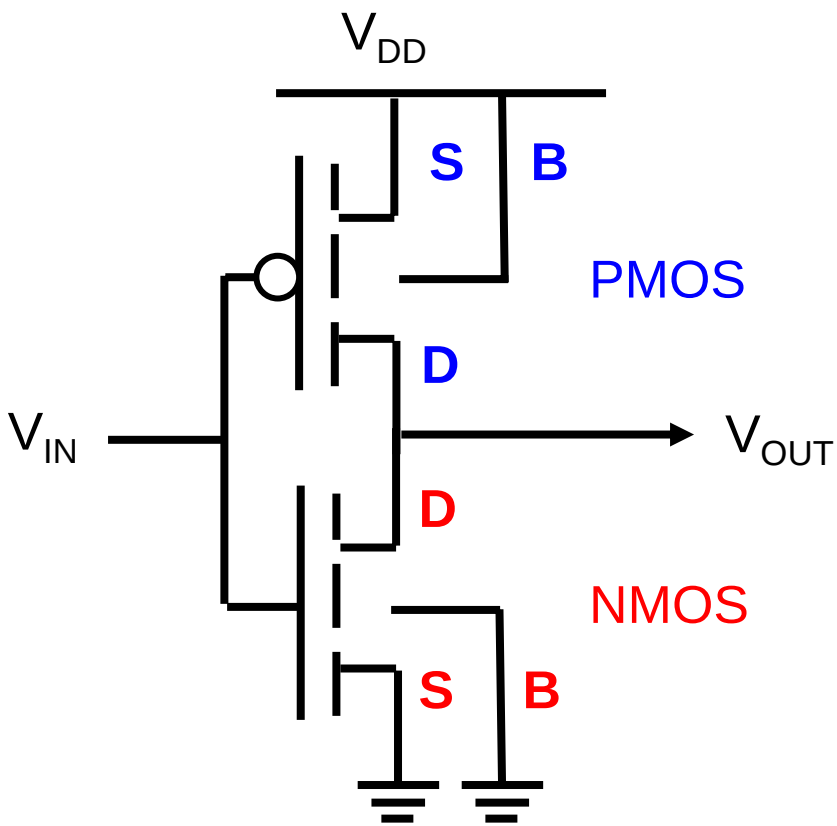
This lecture is a summary of some key points on the relation of device performance to circuit performance.

I assume that you have already viewed Lectures 24, 25, and 26 from the Fall 2006 EE-612 class.

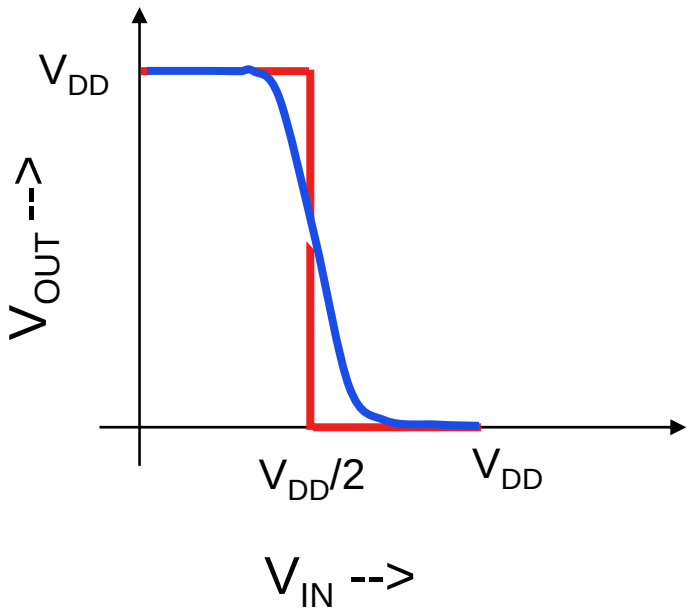
Outline

1) **The CMOS inverter**
2) Speed
3) Power
4) Circuit performance
5) Metrics
6) Limits

ideal CMOS inverter

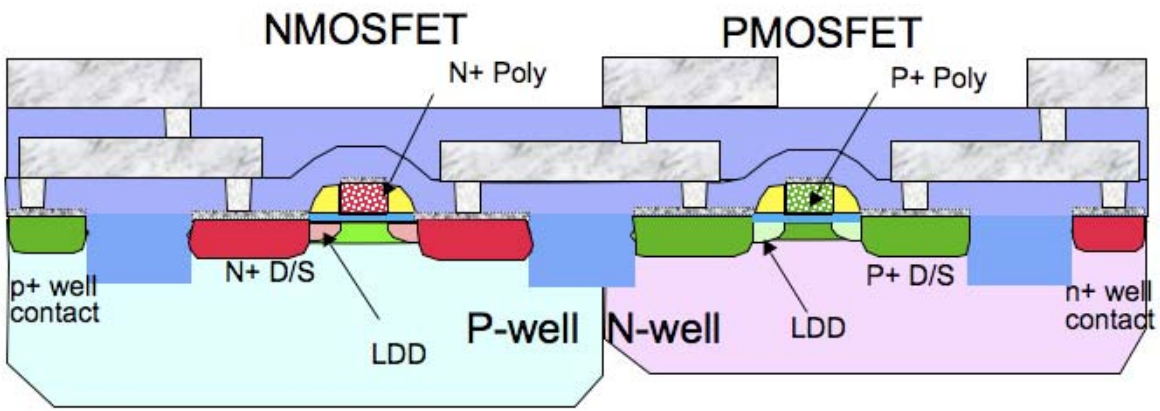


transfer characteristic

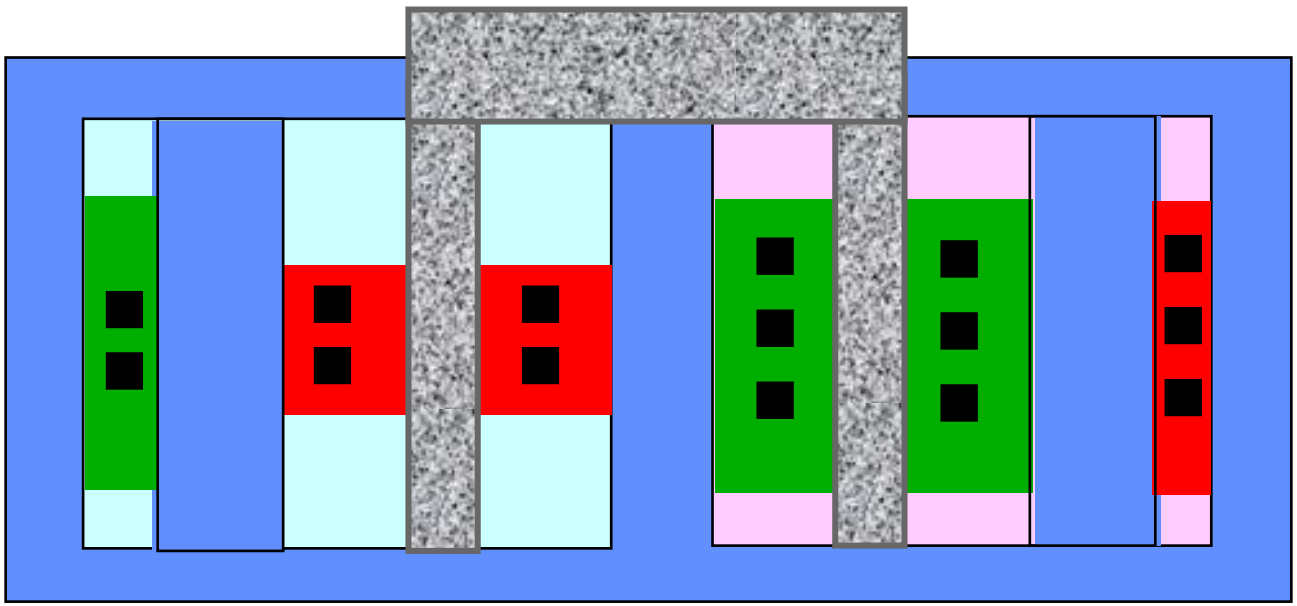


CMOS inverter (top view)

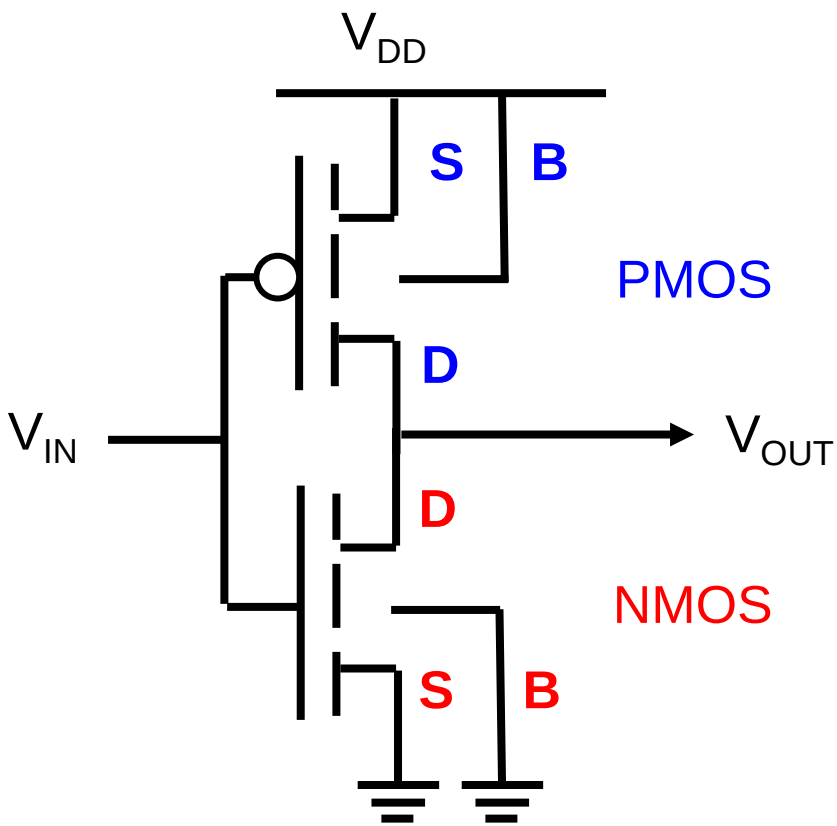
side view



top view



CMOS inverter: voltages



$$I_{DN} = -I_{DP}$$

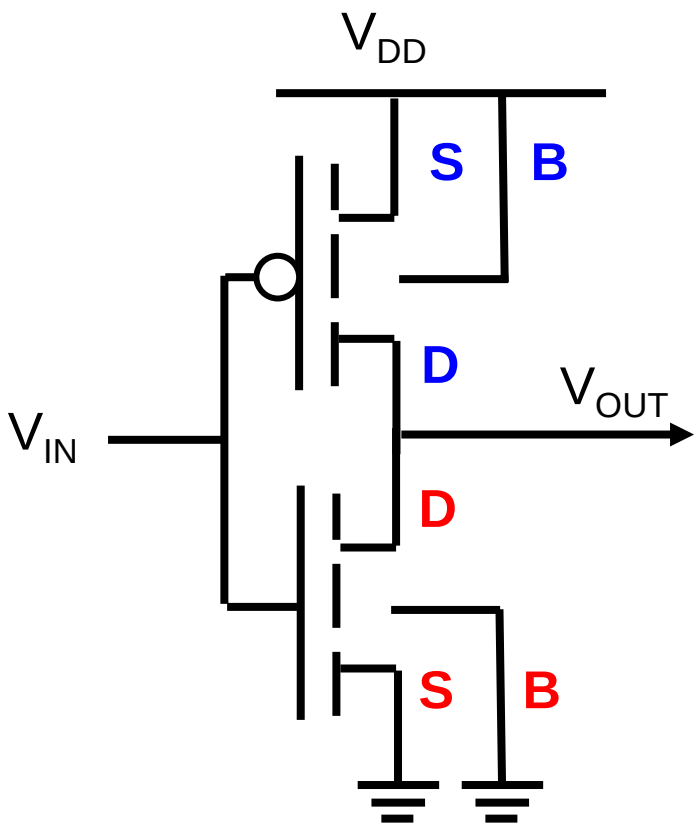
$$V_{gs} = V_{in} - V_{DD}$$

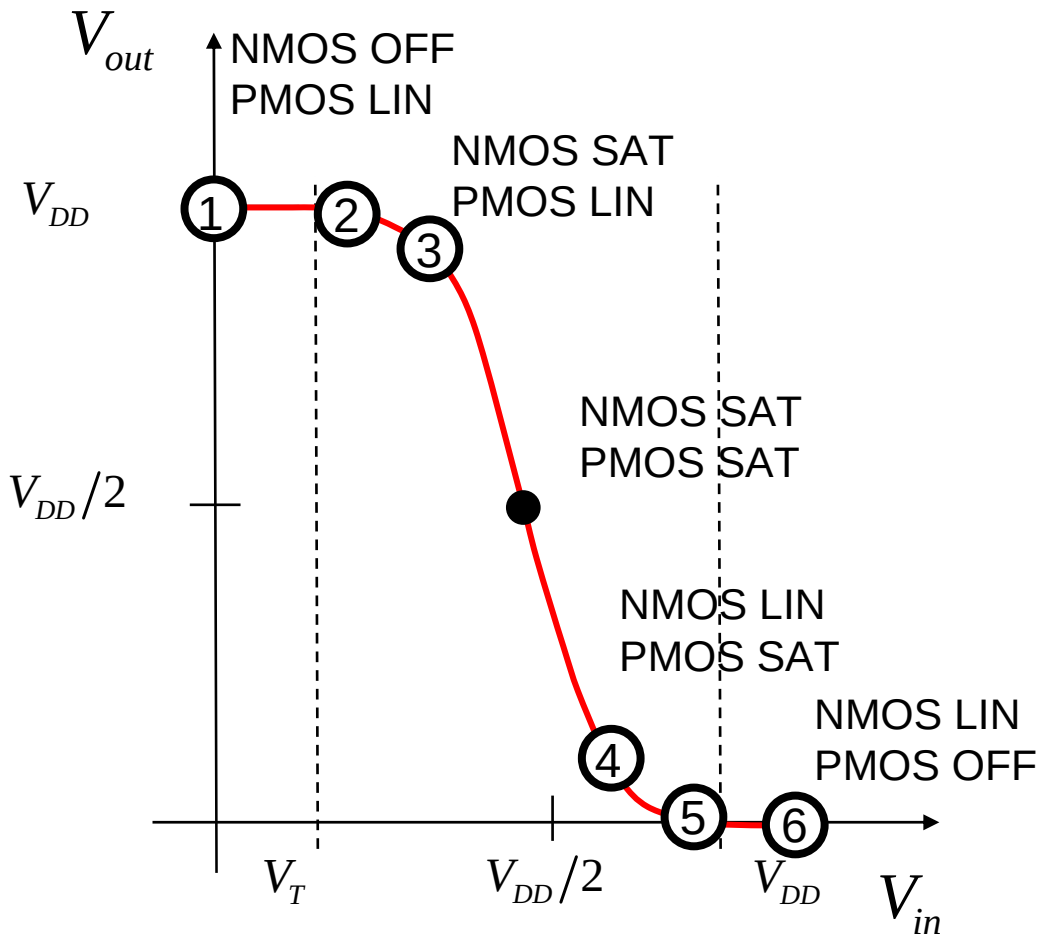
$$V_{ds} = V_{out} - V_{DD}$$

$$V_{gs} = V_{in}$$

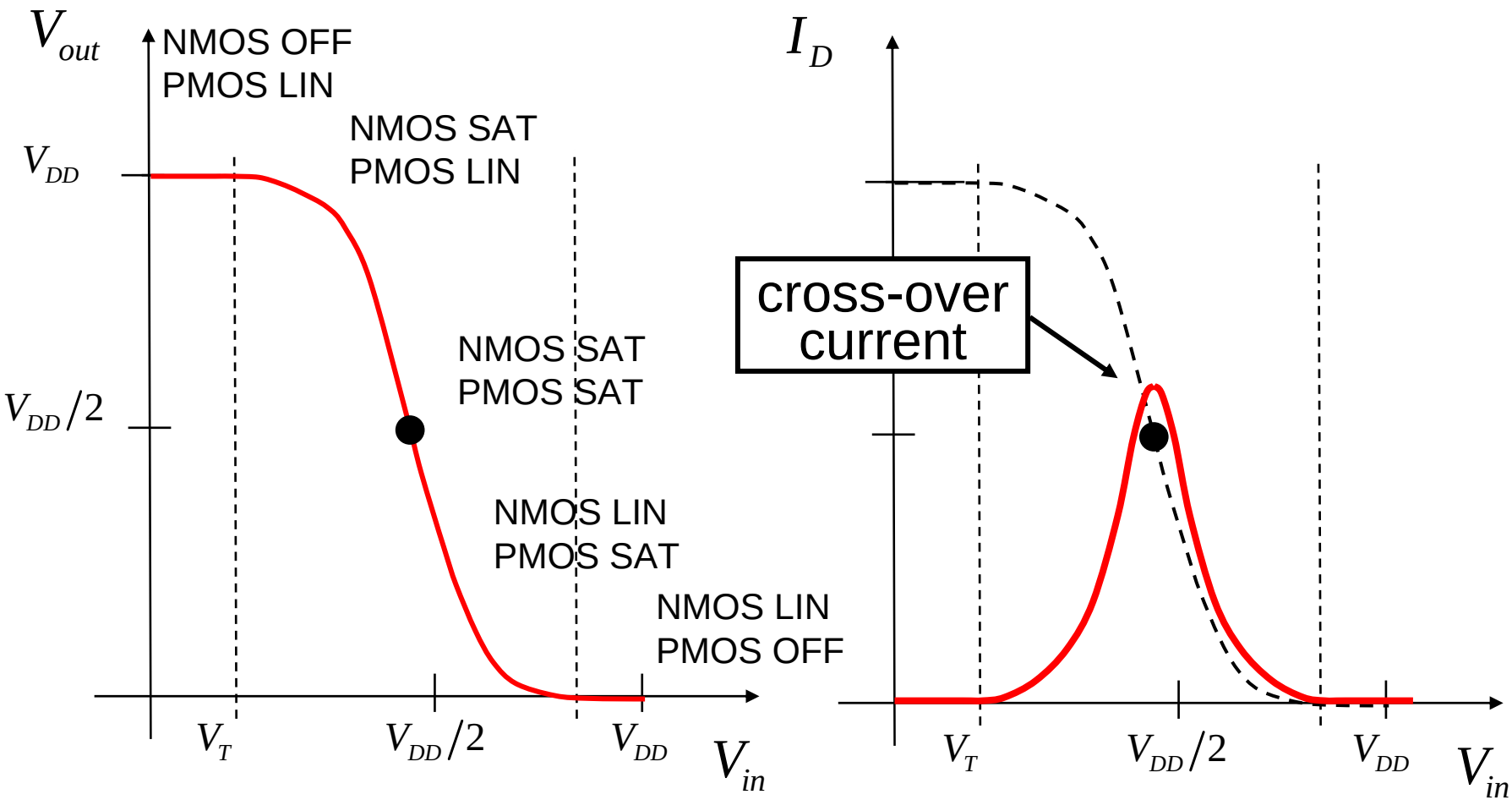
$$V_{ds} = V_{out}$$

CMOS VTC

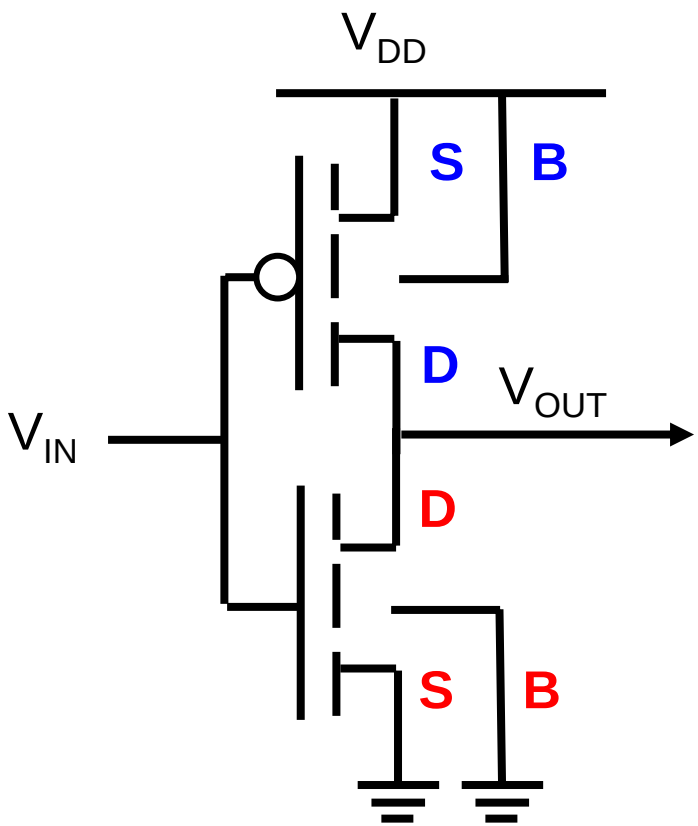

V_DD
S
B
D
V_OUT
V_IN
D
S
B

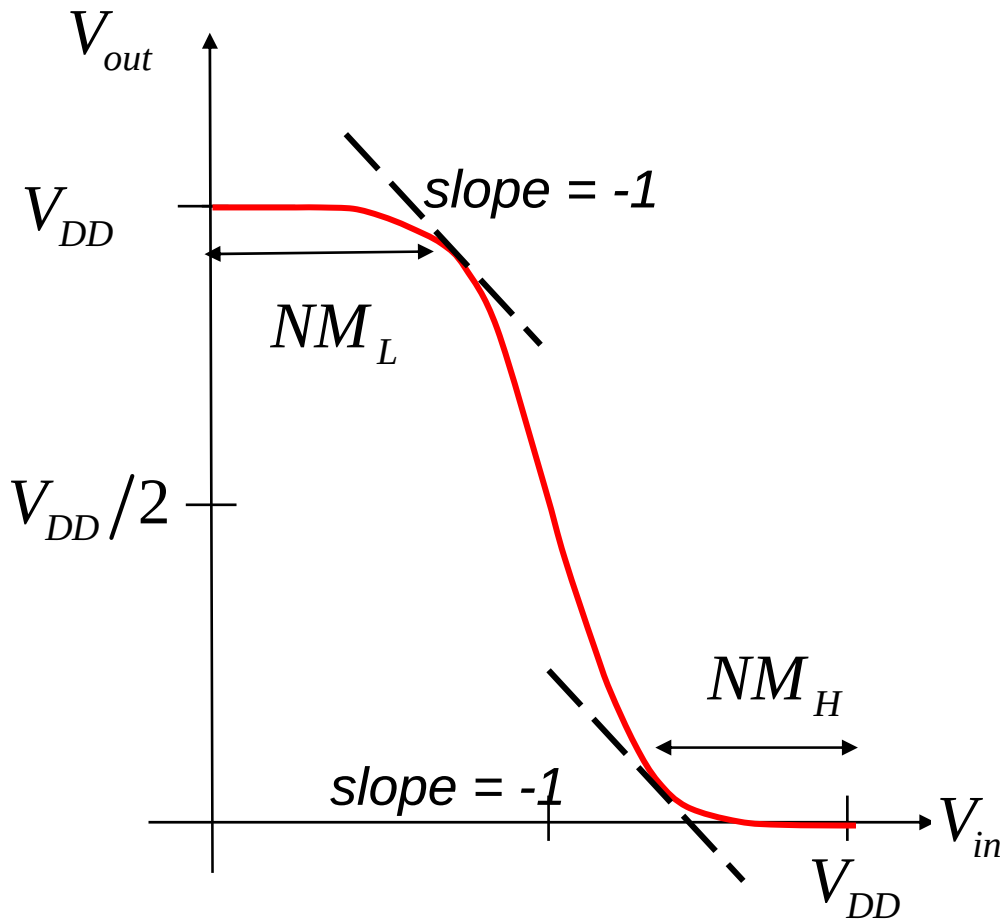

V_out
NMOS OFF
PMOS LIN
NMOS SAT
PMOS LIN
V_DD
1
2
3
NMOS SAT
PMOS SAT
V_DD/2
NMOS LIN
PMOS SAT
NMOS LIN
PMOS OFF
4
5
6
V_T
V_DD/2
V_DD
V_in

CMOS inverter: current



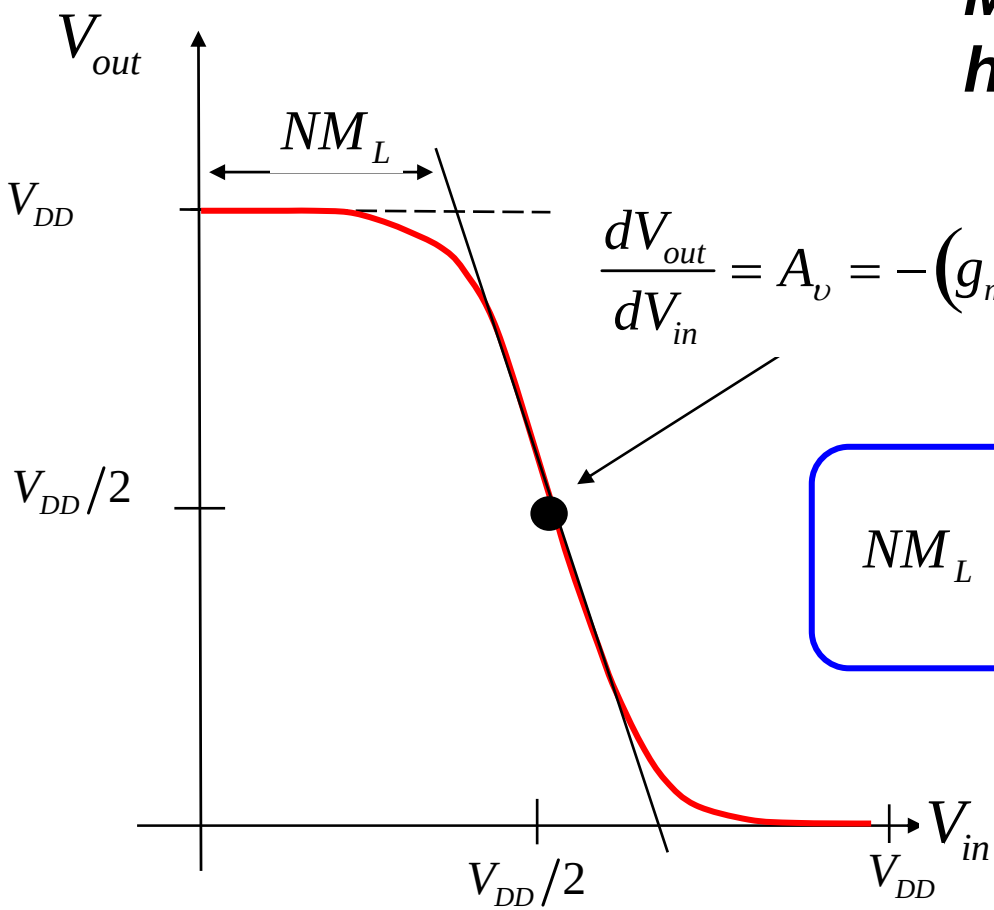
CMOS inverter: noise margins





approximate noise margins

Must have gain to have noise margins!



$$\frac{dV_{out}}{dV_{in}} = A_\upsilon = -\left(g_{mn} + g_{mp}\right)\left(r_{on} \parallel r_{op}\right)$$

$$NM_L \approx NM_H \approx \frac{V_{DD}}{2}\left(1 - \frac{1}{|A_\upsilon|}\right)$$

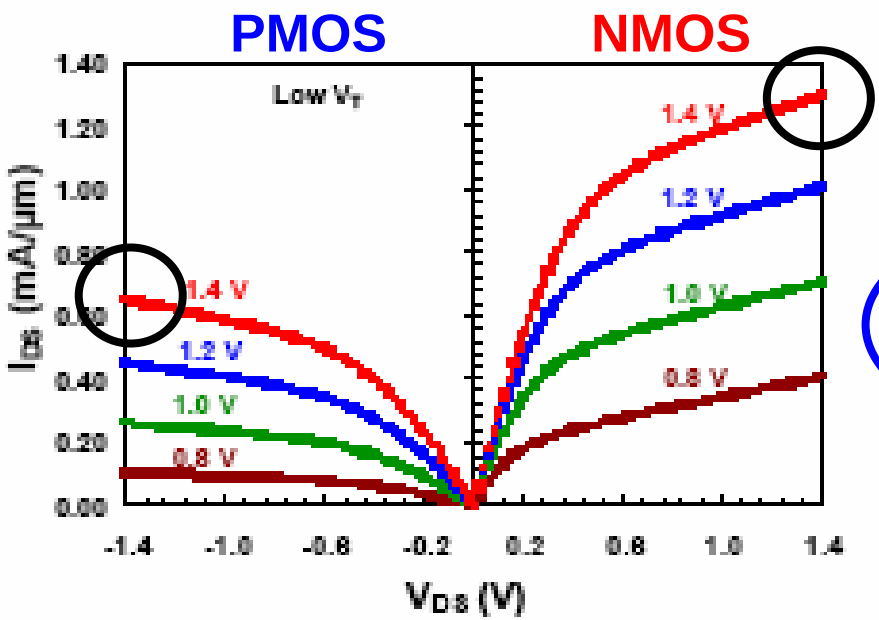
sizing the transistors

For maximum noise margin: $I_N = I_P$.

But NMOS and PMOS transistors are different.

sizing the P-MOSFET

130 nm technology (L_G = 60 nm)



$$W_P \approx 2W_N$$

I-V curves for low V_T device

Intel Technical J., Vol. 6, May 16, 2002.

strained silicon technology

Intel 45 nm, metal gate, high-k, 3rd generation stained Si

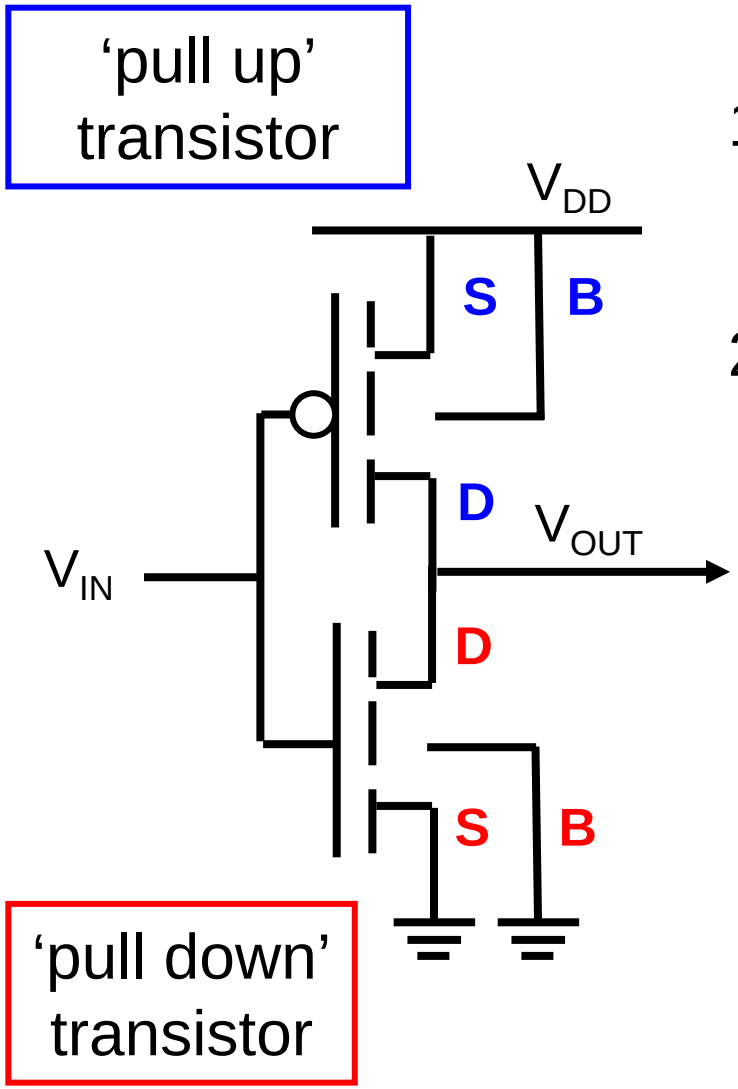
I_{ON} (NMOS) = 1.36 μA/μm

I_{ON} (PMOS) = 1.07 μA/μm

I_N(ON) / I_P(ON) = 1.3

From “Overcoming the Red Brick Walls, by P. Gargini, Intel avaliable at http://www.intel.com/technology/silicon/research.htm?iid=tech_sil+rd

CMOS inverter: summary



1) little current flow (power dissipation) unless switching

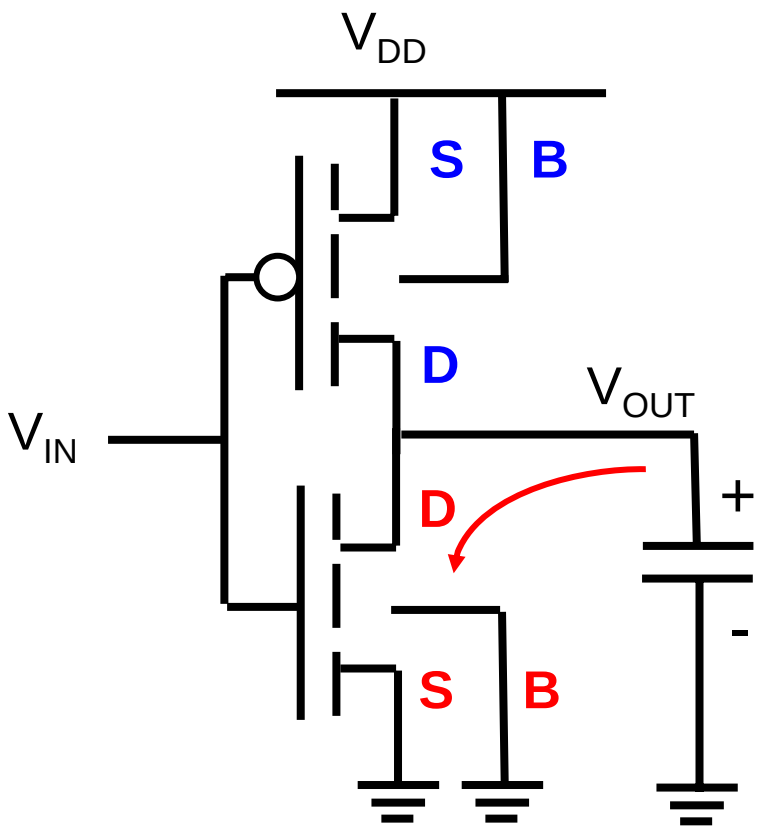
2) good noise margins if device has adequate gain

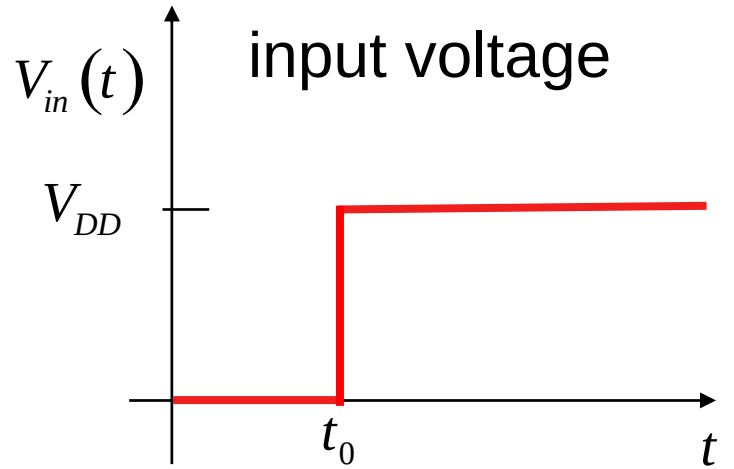
next: *understand speed and power*

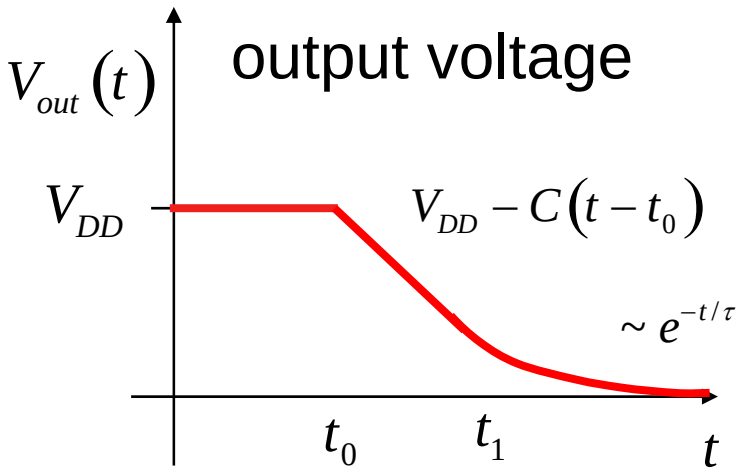
Outline

1) The CMOS inverter
2) **Speed**
3) Power
4) Circuit performance
5) Metrics
6) Limits

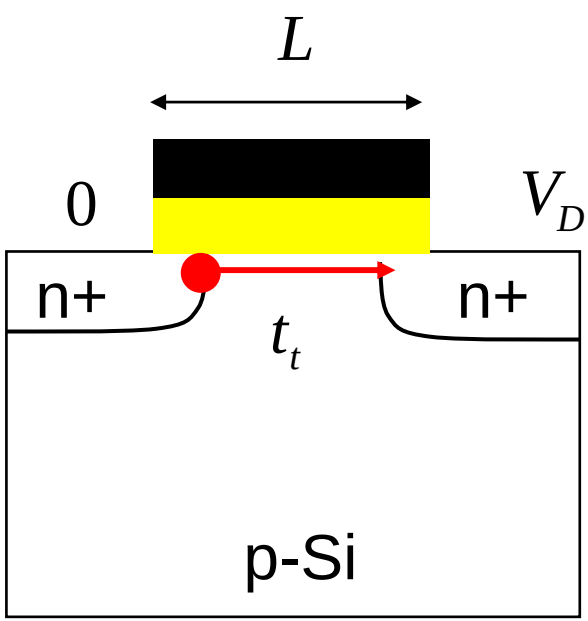
CMOS inverter







transistor speed

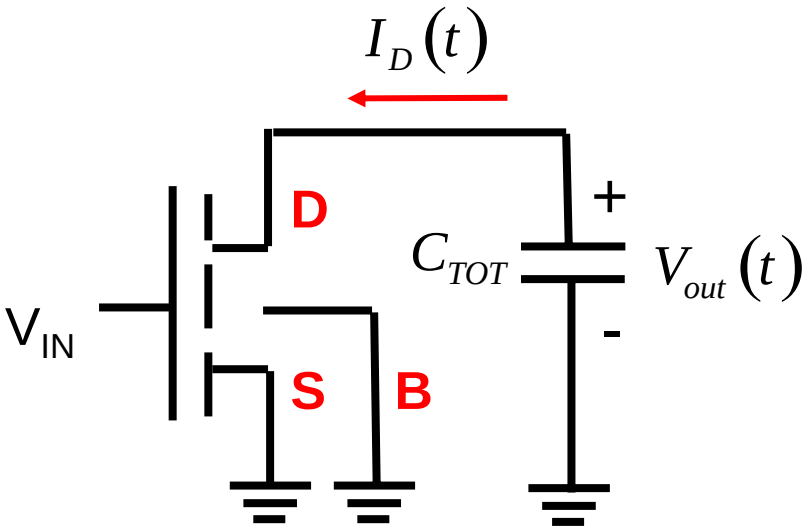


$$t_t = \frac{L}{\langle \upsilon \rangle}$$

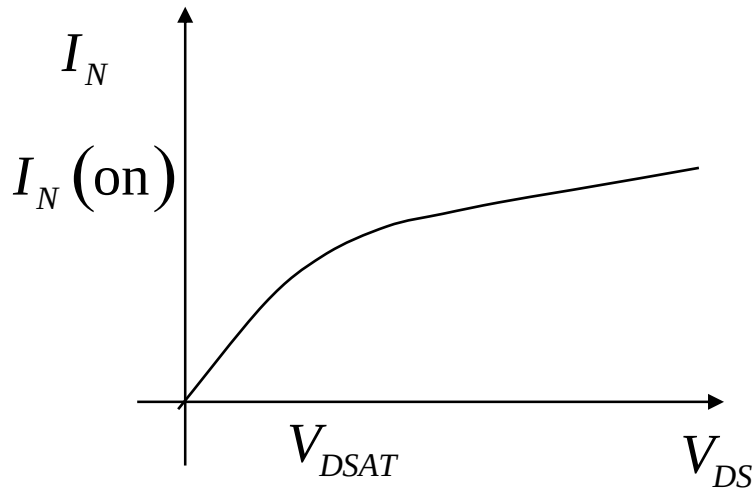
$$t_t \approx \frac{50 \times 10^{-7}\ \text{cm}}{1 \times 10^{7}\ \text{cm/s}} = 0.5\ \text{psec}$$

$$f = \frac{1}{2\pi t_t} \approx 0.3\,\text{THz}$$

discharging time



quasi-static assumption
simplified I_D - V_{DS}

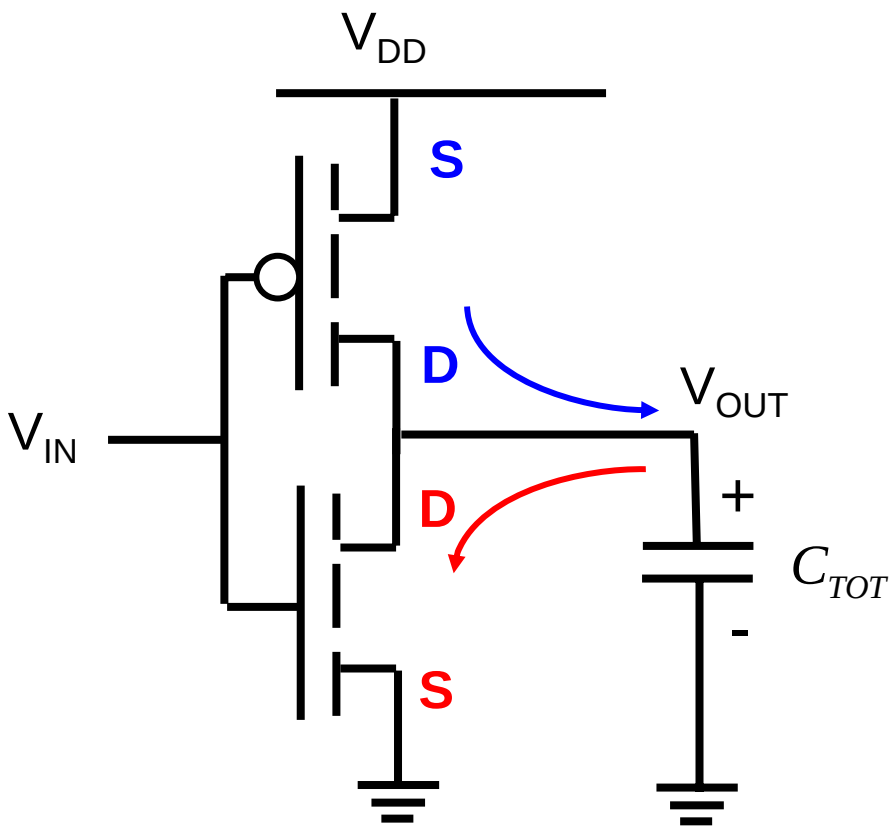


$$\tau_n = \frac{C_{TOT} V_{DD}}{2 I_N(\text{eff})} \equiv R_{swn} C_{TOT}$$

$$I_d(t) = -C_{TOT} \frac{dV_{out}(t)}{dt}$$

$$R_{swn} \approx k_n \frac{V_{DD}}{I_N(\text{on})} \qquad k_n = \frac{1}{2}$$ (first order)

CMOS inverter speed



$$\tau = \frac{1}{2}\left(\frac{C_{TOT}V_{DD}}{2I_N(\text{on})} + \frac{C_{TOT}V_{DD}}{2I_P(\text{on})}\right)$$

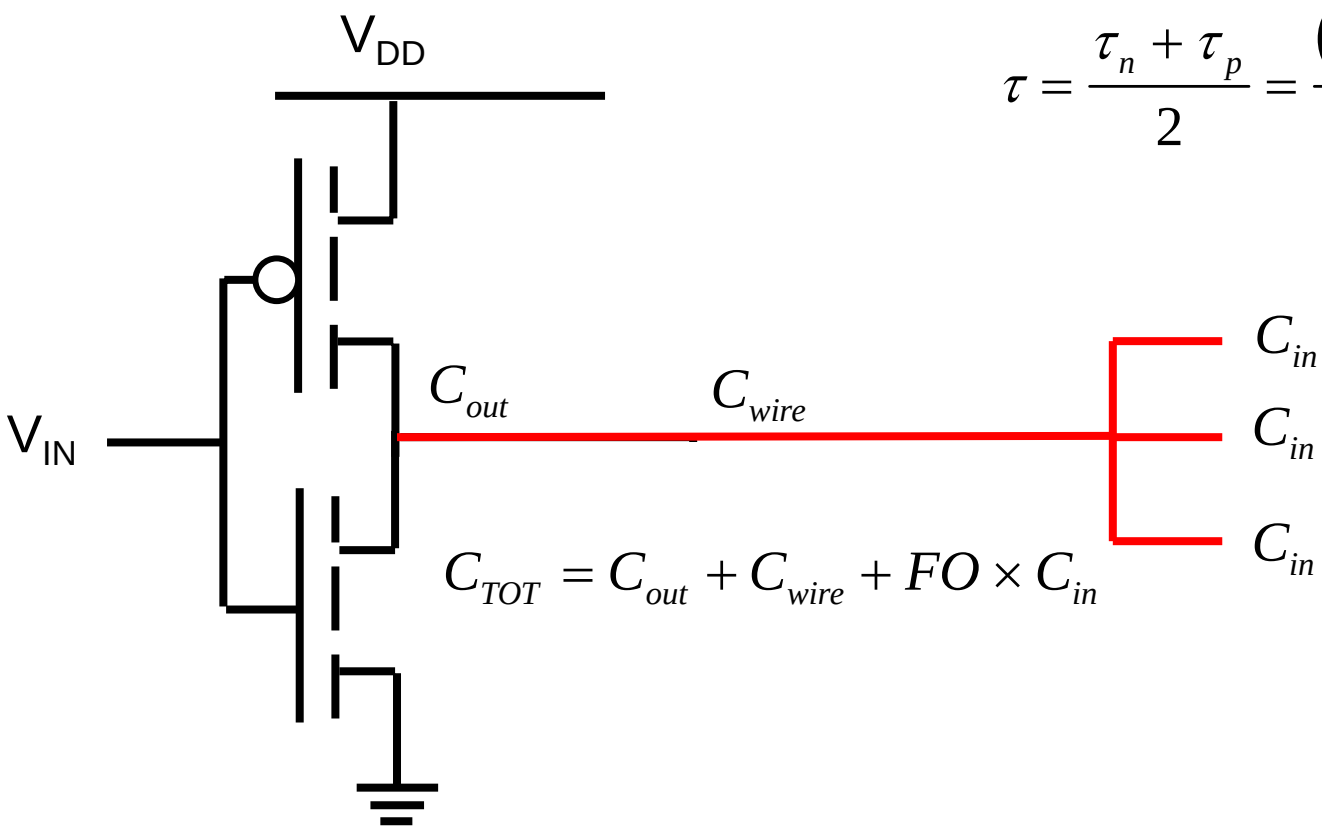
$$\tau = \frac{\left(R_{swN} + R_{swP}\right)}{2}C_{TOT}$$

$$\tau = R_{sw}C_{TOT}$$

$$R_{swn} = k_n \frac{V_{DD}}{I_N(\text{on})} \qquad k_n > \frac{1}{2}$$

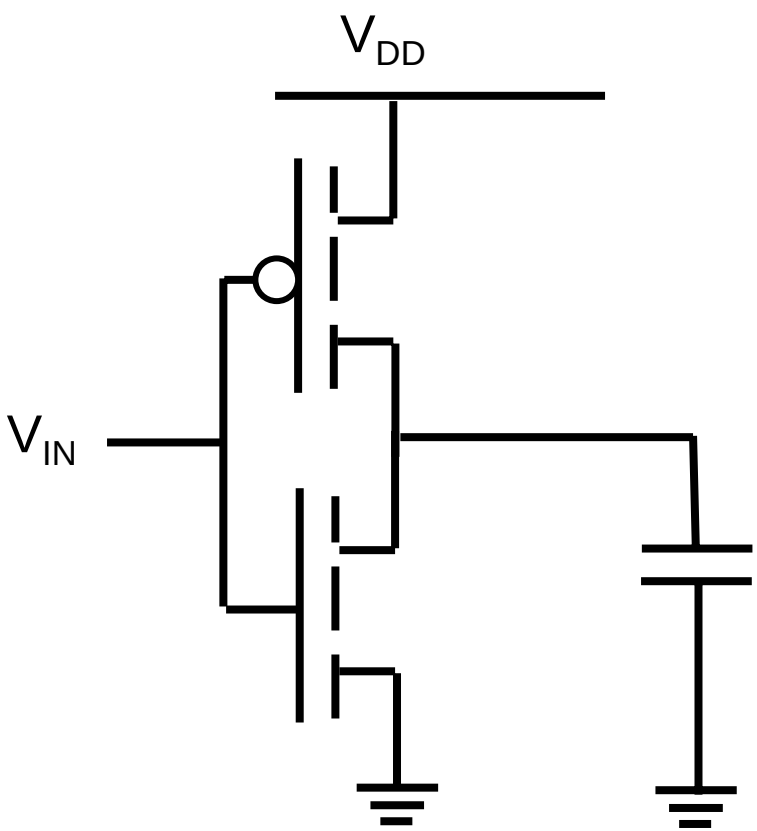
loaded propagation delay

$$\tau = \frac{\tau_n + \tau_p}{2} = \frac{\left(R_{swn} + R_{swp}\right)}{2} C_{TOT}$$



$$C_{TOT} = C_{out} + C_{wire} + FO \times C_{in}$$

use of buffers

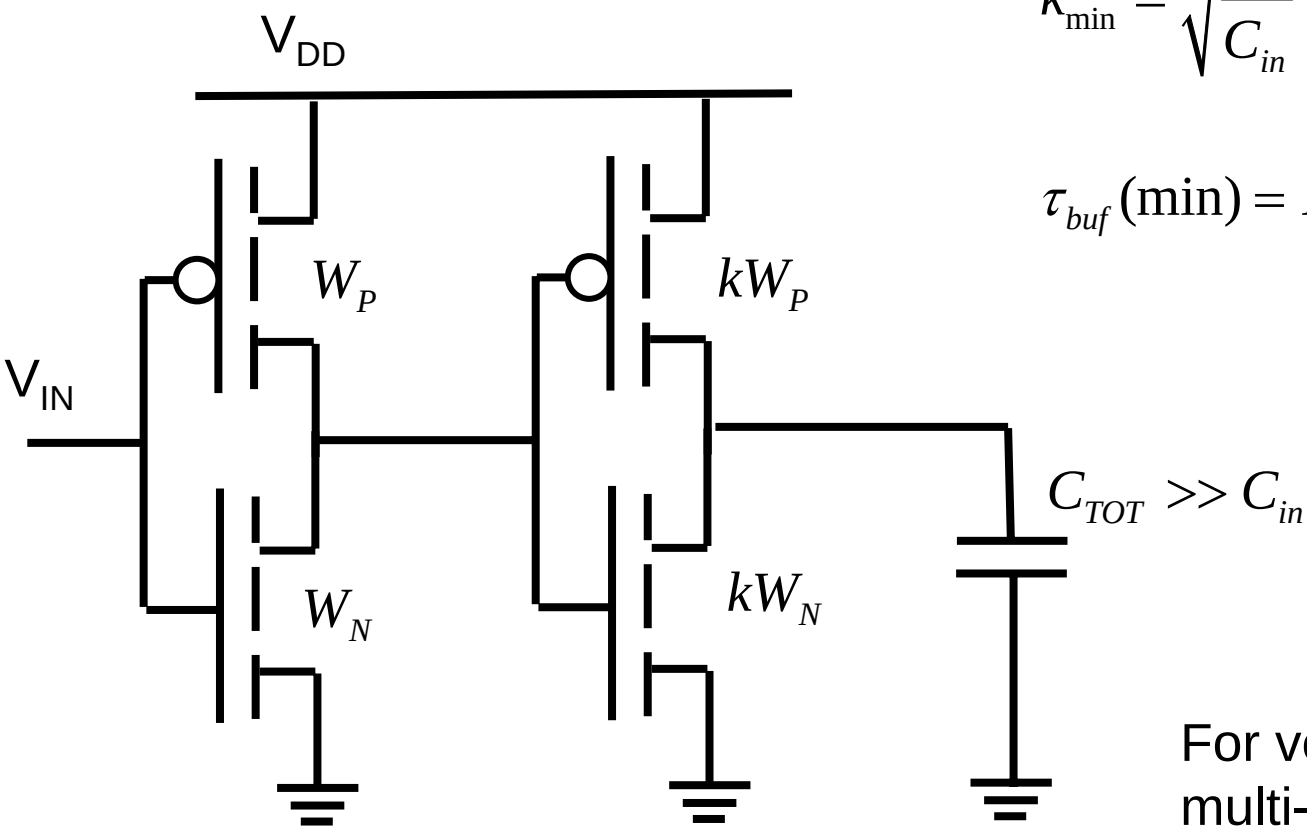


$$\tau = R_{sw}\left(C_{out} + C_L\right)$$

Can we do better?

$$C_{TOT} >> C_{in}$$

delay with buffers



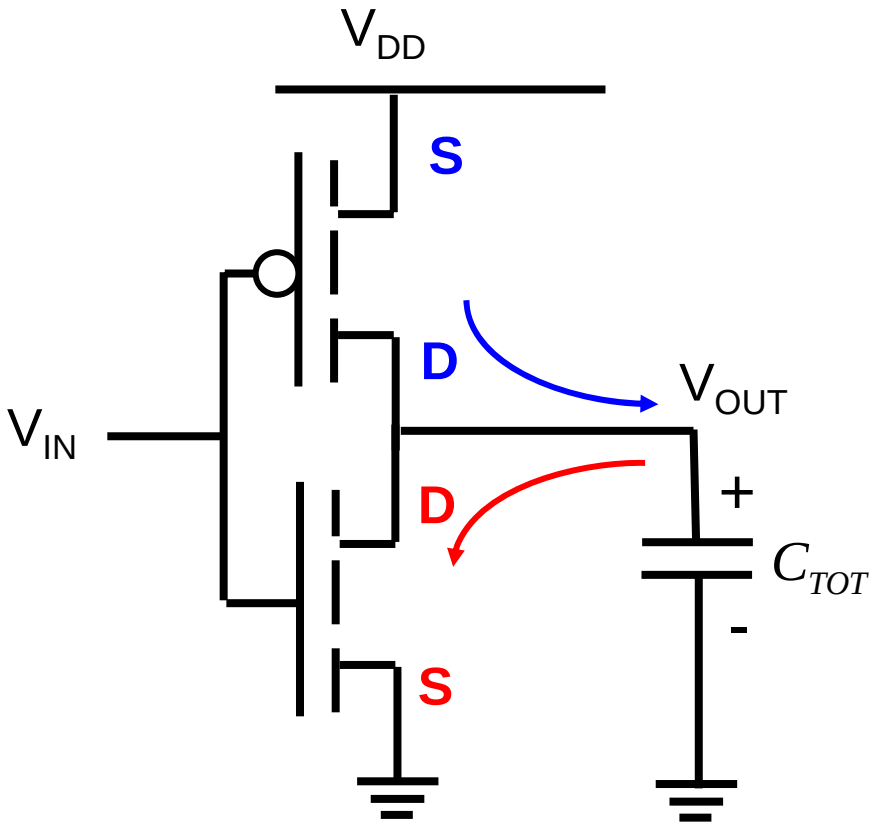
$$k_{\min} = \sqrt{\frac{C_L}{C_{in}}}$$

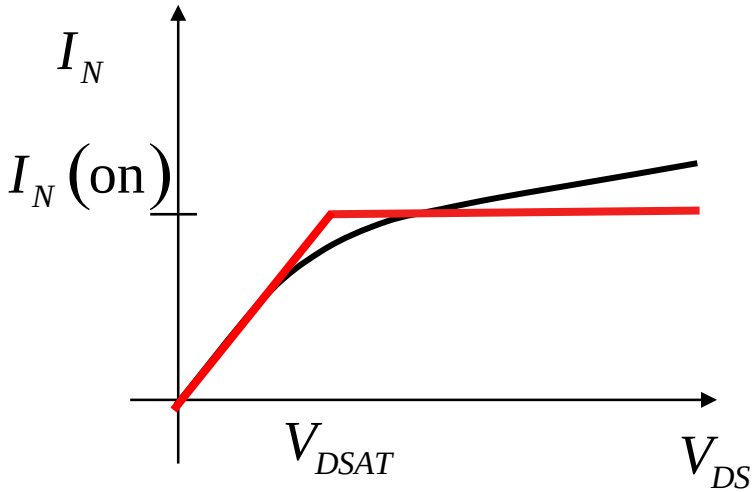
$$\tau_{buf}(\min) = R_{sw}\left(2C_{out} + 2\sqrt{C_{in}C_L}\right)$$

For very heavy loads, use multi-stage buffers.
See Taur and Ning, HW probs. 5.7 - 5.10

on-current determines circuit speed

$$\tau = R_{sw} C_{TOT} \qquad R_{sw} \sim V_{DD} / I_{ON} \qquad \tau \sim C_{TOT} V_{DD} / I_{ON}$$





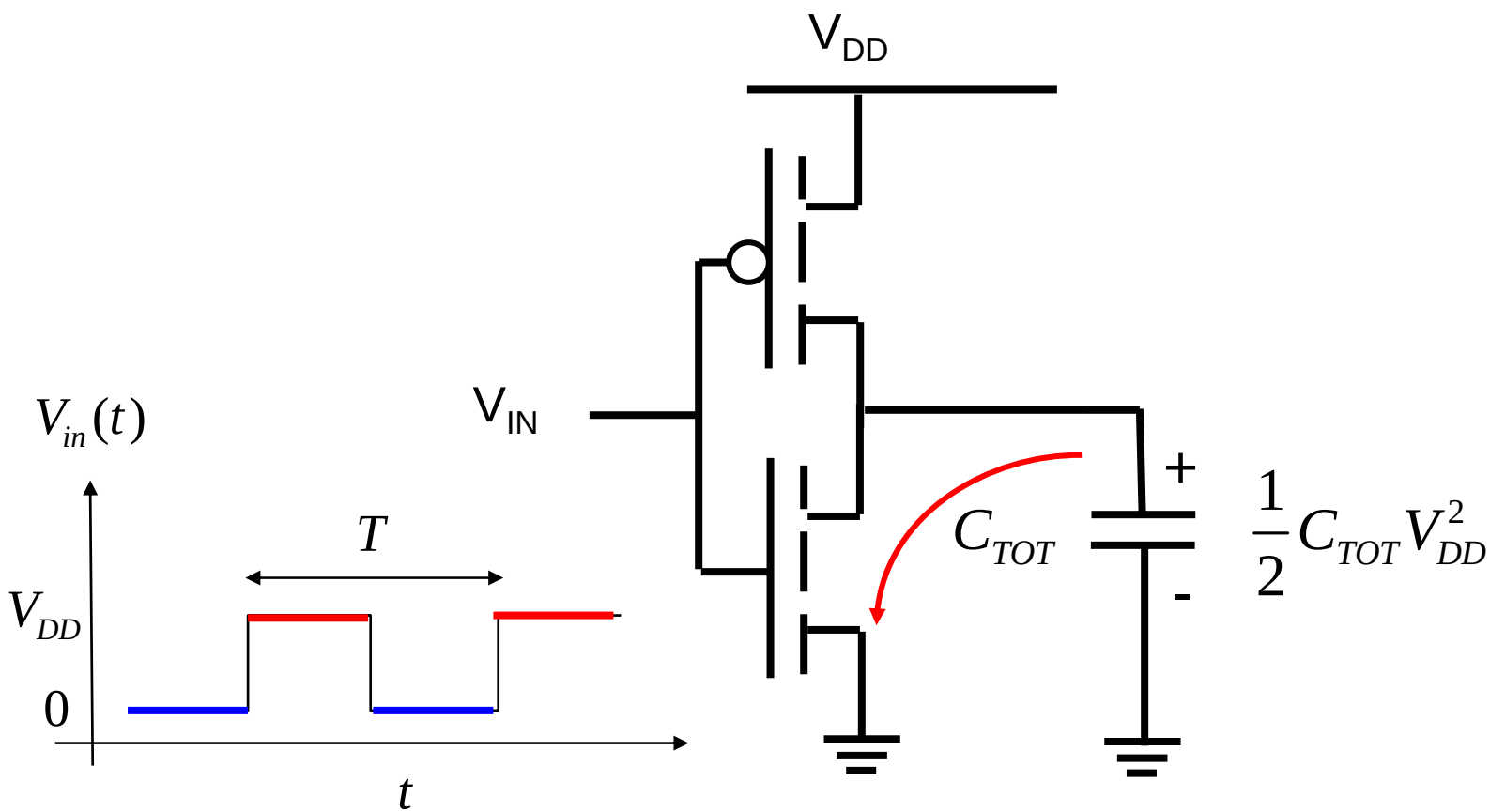
1) quasi-static assumption

2) simplified I_D - V_{DS}

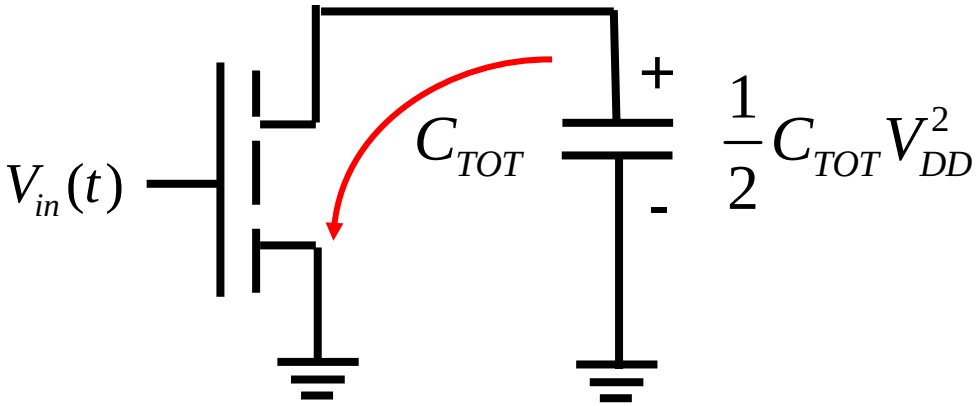
Outline

1) The CMOS inverter
2) Speed
3) **Power**
4) Circuit performance
5) Metrics
6) Limits

power



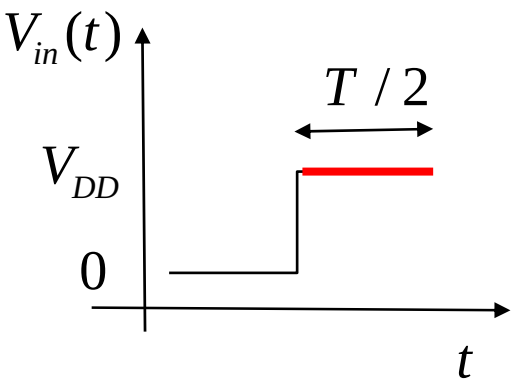
discharge cycle



$$E_C(0) = \frac{1}{2}C_{TOT}V_{DD}^2$$

$$E_C(T/2) = 0$$

$$P_{dynamic} = \frac{\Delta E}{T/2} = \frac{C_{TOT}V_{DD}^2}{T}$$

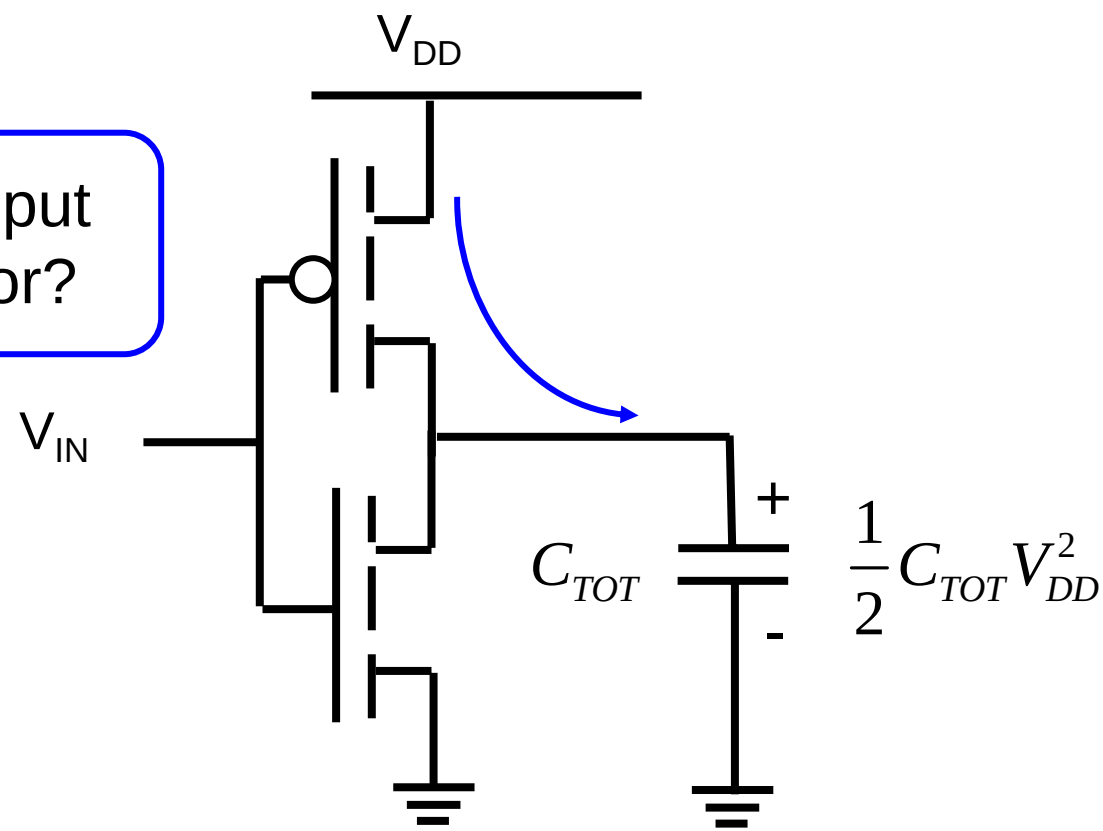


$$P_{dynamic} = \alpha f C_{TOT}V_{DD}^2$$

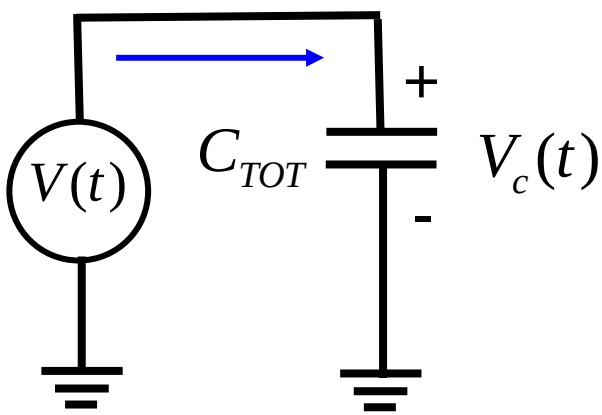
switching activity

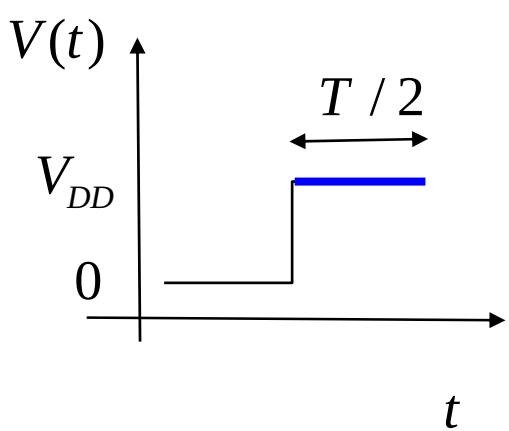
charging cycle

does it take power to put energy in the capacitor?



charging cycle (ii)





$$E_C(0) = 0$$

$$E_C(T/2) = \frac{1}{2} C_{TOT} V_{DD}^2$$

$$E_B = \int_0^{T/2} V_{DD} i(t) dt$$

$$E_B = V_{DD} \int_0^{T/2} i(t) dt = V_{DD} Q$$

$$E_B = V_{DD} Q = C_{TOT} V_{DD}^2$$

$$E_{diss} = \frac{1}{2} C_{TOT} V_{DD}^2$$

outline

1) The CMOS inverter
2) Speed
3) Power
4) **Circuit performance**
5) Metrics
6) CMOS circuit metrics

device impact on circuit performace

Question:

Given a technology, how does circuit performance depend on transistor design (W, T_{OX}, V_{DD}, etc.)

Taur and Ning assume a 250nm technology and explore this question by Spice simulation (see pp. 264 - 279). Can we understand the major trends simply?

effect of transistor *W* on delay

$$\tau = R_{sw} C_{TOT} \sim C_{TOT} V_{DD} / I_{ON}$$

$$C_{TOT} = C_{out} + C_{wire} + FO \times C_{in}$$

$$C_{out} \sim W \qquad I_{ON} \sim W$$

$$C_{in} \sim W$$

loaded vs. unloaded delay

$$\tau \sim C_{TOT} V_{DD} / I_{ON} = \left(C_{out} + FO \times C_{in} + C_{wire} \right) V_{DD} / I_{ON}$$

i) ***unloaded:***
C_{in} and C_{out} dominate, $C_{TOT} \sim W$
--> <u>*τ independent of W*</u>

ii) ***loaded:***
C_L dominates, $C_{TOT} \sim$ *independent of W*
--> <u>*$\tau \sim 1/W$*</u>

effect of T_{OX} on delay

$$\tau \sim C_{TOT} V_{DD} / I_{ON} = \left(C_{out} + FO \times C_{in} + C_{wire}\right) V_{DD} / I_{ON}$$

i) **unloaded delay** (C_L = 0)

$$\left.\begin{array}{l} I_{ON} \sim 1/T_{OX} \\ C_{in} \sim 1/T_{OX} \\ C_{out} \quad \text{constant} \end{array}\right\} \quad \tau_{unloaded} \sim \text{constant}$$

ii) **loaded delay** (C_L > 0)

$$\left.\tau_{loaded} \approx C_L V_{DD} / I_{ON}\right\} \quad \tau_{loaded} \downarrow \quad \text{as} \quad T_{OX} \downarrow$$

(see Fig. 5.32 of Taur and Ning)

effect of *L* on delay

$$\tau \sim C_{TOT} V_{DD} / I_{ON} = \left(C_{out} + FO \times C_{in} + C_{wire}\right) V_{DD} / I_{ON}$$

$$\left.\begin{array}{l} I_{ON} = W C_{OX} \upsilon(0)\left(V_{GS} - V_T\right)\downarrow \quad \text{as } L\uparrow \\ C_{in} \sim L \\ C_{out}, C_L \quad \text{constant} \end{array}\right\} \quad \tau\uparrow \quad \text{as} \quad L\uparrow$$

(see Fig. 5.31 of Taur and Ning)

effect of V_{DD} on delay

$$\tau \sim C_{TOT} V_{DD} / I_{ON} = \left(C_{out} + FO \times C_{in} + C_{wire}\right) V_{DD} / I_{ON}$$

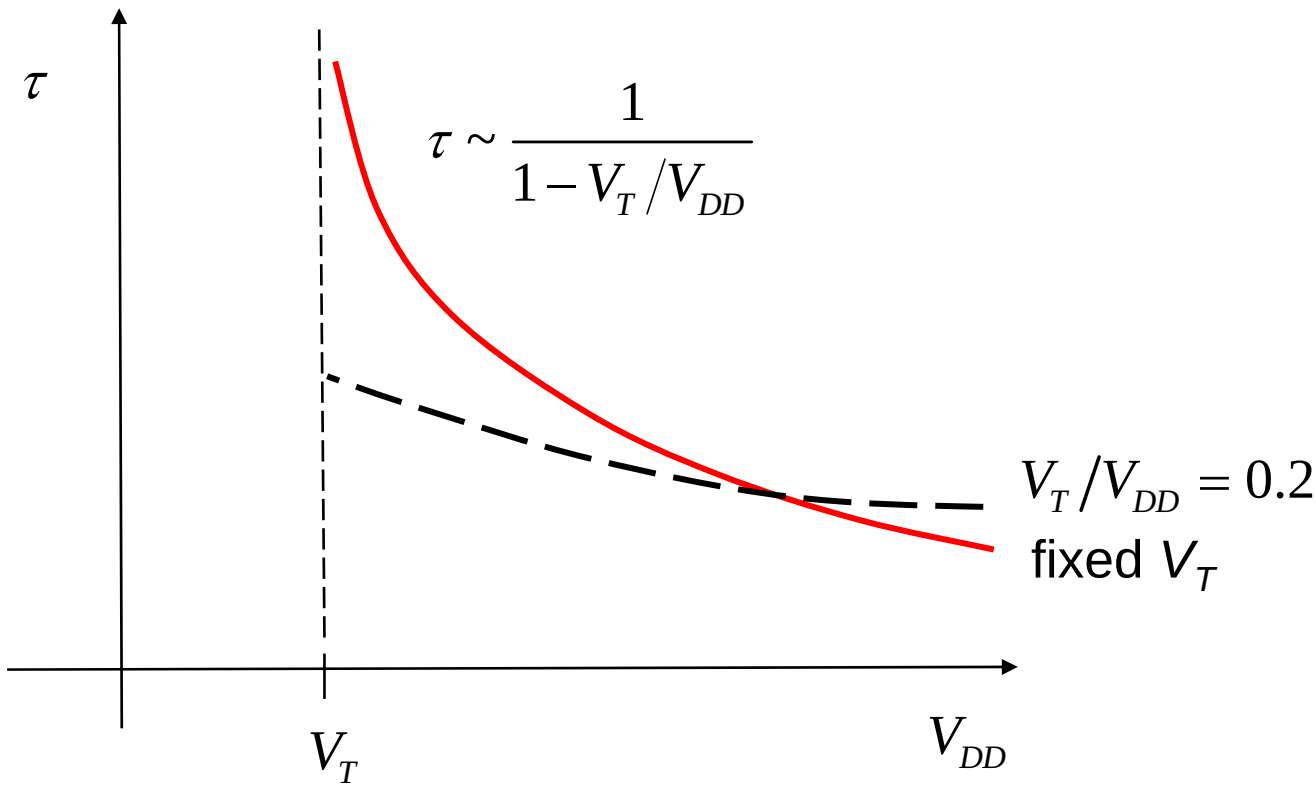
$$I_{ON} = W C_{ox} \langle \upsilon(0) \rangle \left(V_{DD} - V_T\right)$$

$$\tau \sim C_{TOT} / \left(1 - V_T / V_{DD}\right)$$

$$C_{out} = \varepsilon_{Si} / W_D \sim 1 / \sqrt{V_{DD} + V_{bi}}$$

$$\tau \sim \frac{1}{1 - V_T / V_{DD}}$$

delay vs. V_{DD}



$$I_D(\text{off}) \sim e^{-qV_T / mk_{BT}}$$

(see Fig. 5.33 of Taur and Ning)

power-delay trade-off

circuit speed:

$$\tau \sim 1/\left(1 - V_T / V_{DD}\right) \qquad f \sim \left(1 - V_T / V_{DD}\right)$$

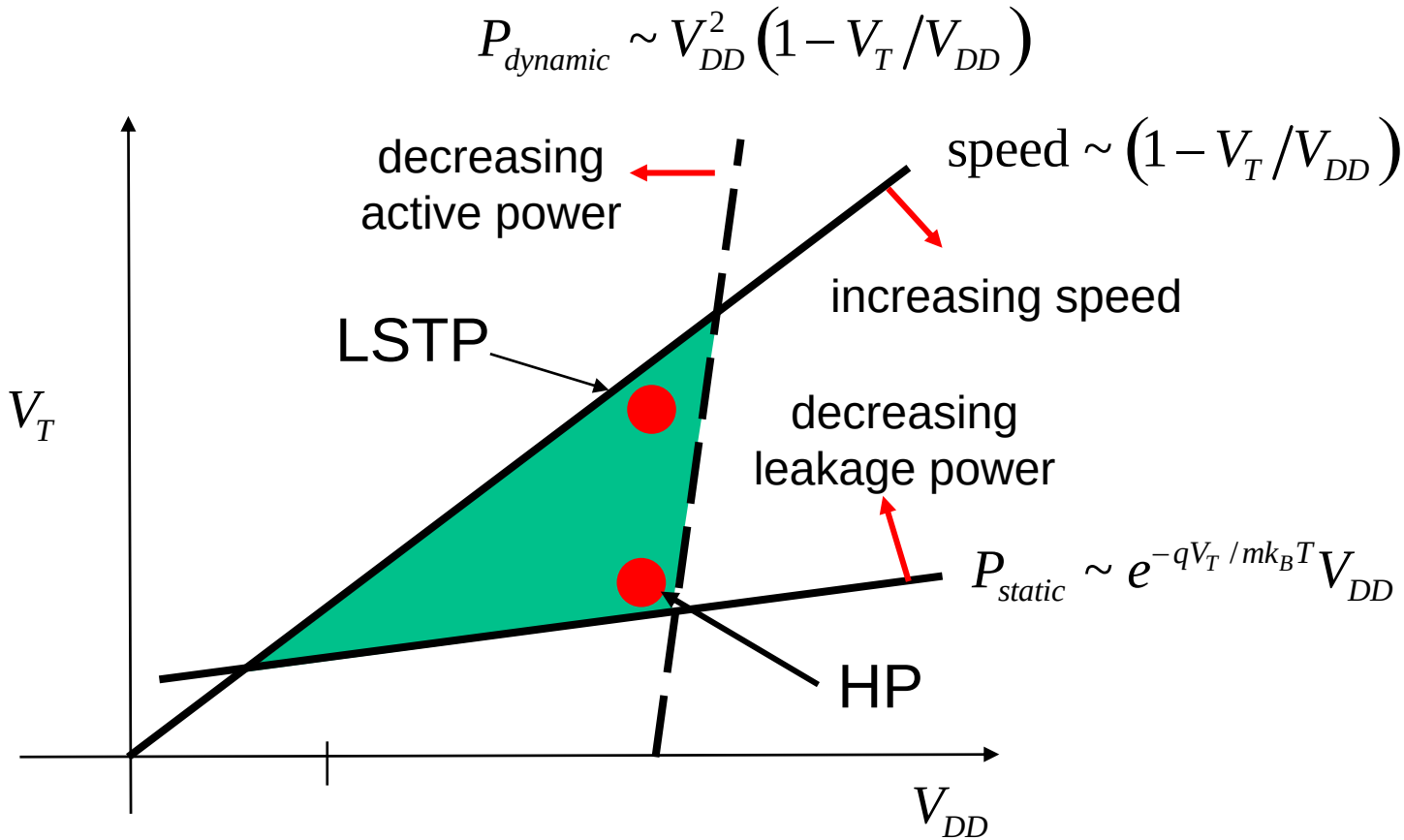
dynamic (switching) power:

$$P_{dynamic} = \alpha f C_{TOT} V_{DD}^2 \sim V_{DD}^2 \left(1 - V_T / V_{DD}\right)$$

static (leakage) power:

$$P_{static} \sim I_{OFF} V_{DD} \sim e^{-qV_T / mk_B T} V_{DD}$$

power-delay trade-off



(see Fig. 5.34 of Taur and Ning)

Outline

1) The CMOS inverter
2) Speed
3) Power
4) Circuit performance
5) **Metrics**
6) Limits

key metrics

1) Switching energy: $$E_S = \frac{1}{2} C V_{DD}^2$$

2) Switching delay: $$\tau_S = \frac{C V_{DD}}{I_{ON}}$$

3) Dynamic power: $$P_D = \alpha f C V_{DD}^2$$

4) Energy-delay product: $$E_S \tau = \frac{1}{2} \frac{C^2 V_{DD}^3}{I_{ON}}$$

device vs. circuit

1) Device: $C = C_{DEV}$

2) Device: $C = C_{TOT}$

$$E_S = \frac{1}{2} C V_{DD}^2$$

$$\tau_S = \frac{C V_{DD}}{I_{ON}}$$

$$P_D = \alpha f C V_{DD}^2$$

$$E_S \tau = \frac{1}{2} \frac{C^2 V_{DD}^3}{I_{ON}}$$

device metrics for 65 nm technology node

1) Switching energy: $$E_S = \frac{1}{2} C_{DEV} V_{DD}^2 \approx 21 \text{ aJ}$$

2) Switching delay: $$t_t = \frac{C_{DEV} V_{DD}}{I_{ON}} = 0.64 \text{ ps}$$

3) Dynamic power: $$P_D = \alpha f C_{DEV} V_{DD}^2$$

4) Energy-delay product: $$E_S \tau = \frac{1}{2} \frac{C^2 V_{DD}^3}{I_{ON}} = 1.4 \times 10^{-29} \text{ J-s}$$

circuit metrics for 65 nm technology node

2-input, FO4 NAND:

C_{TOT} ~ 3 fF

V_{DD} ~ 1.2V

$$E_S = \frac{1}{2} C_{TOT} V_{DD}^2 \approx 2 \ \ \text{fJ}$$

(100 X device)

$$t_t = \frac{C_{TOT} V_{DD}}{I_{ON}} = 20 \ \ \text{ps}$$

(30X device)

Outline

1) CMOS Inverter
2) Speed
3) Power
4) Circuit performance
5) Metrics
6) **Limits**

   -device

   -circuit

acknowledgment

The approach that I take here is similar to the work of V.V. Zhirnov, R.K. Cavin, J.A. Hutchby, and G. Bourianoff, “Limits to Binary Logic Switch Scaling - A Gedankan Model,” *Proc. IEEE*, Special Issue on Nanoelectronics and Nanoscale Processing, Nov. 2003.

results: limits of MOSFETs

1) Switching energy: $E_S > k_B T \ln(2)$

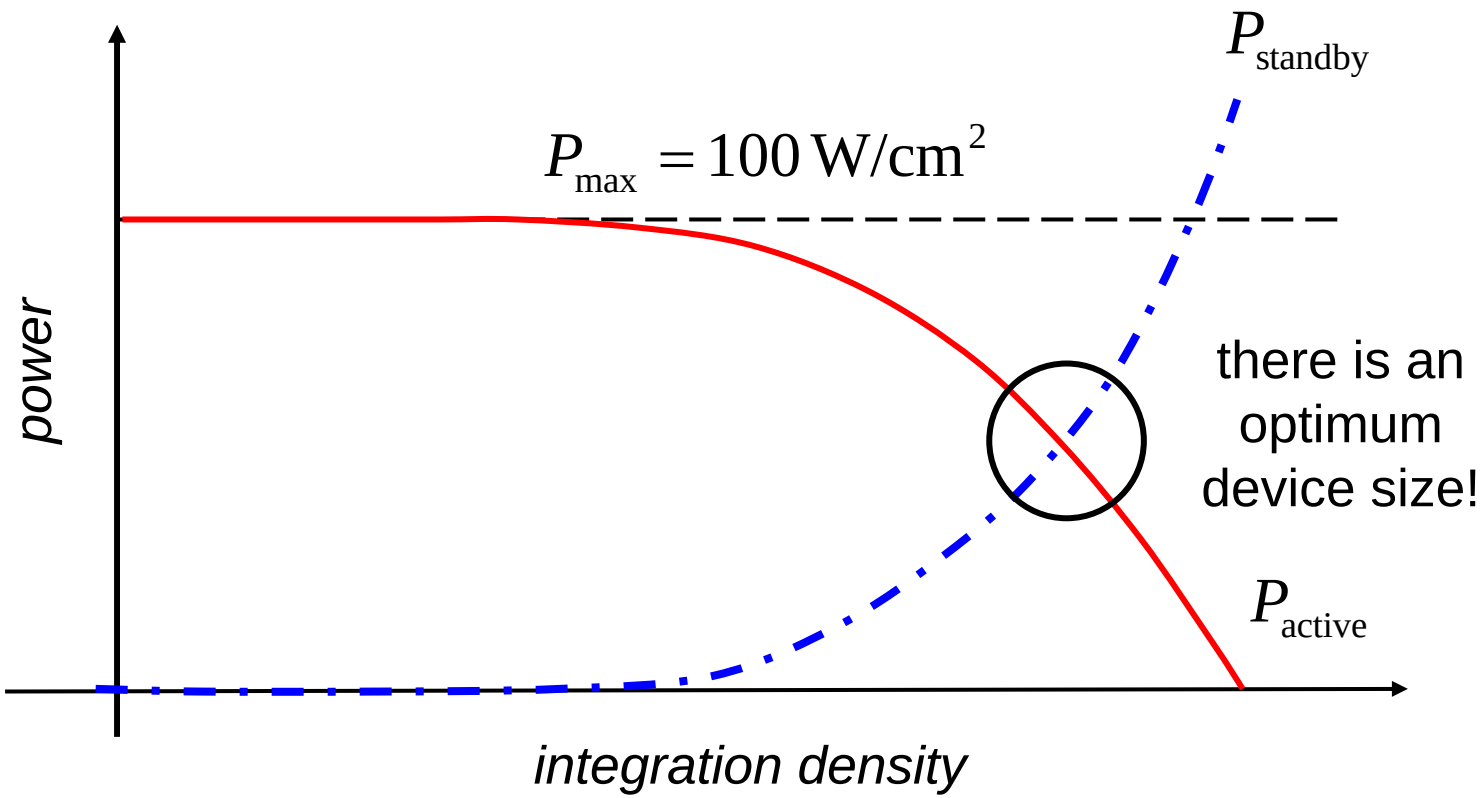
2) Switching delay: $t_S > \mathrm{h}/E_S(\min)$

3) Device size: $L_{\min} > \mathrm{h}/\sqrt{2mE_S(\min)}$

4) Device density: $\hat{n}_D < P_{\max} t_S(\min)/E_S(\min)$

5) Energy-delay: $E\tau > \mathrm{h}$

power-constrained design



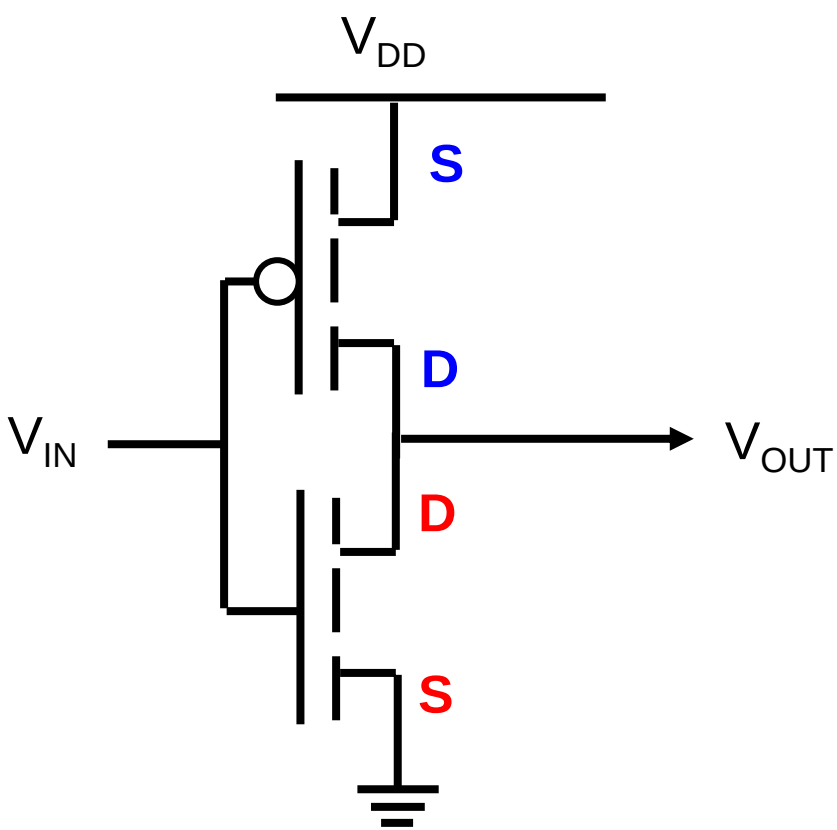
(Dave Frank, IBM)

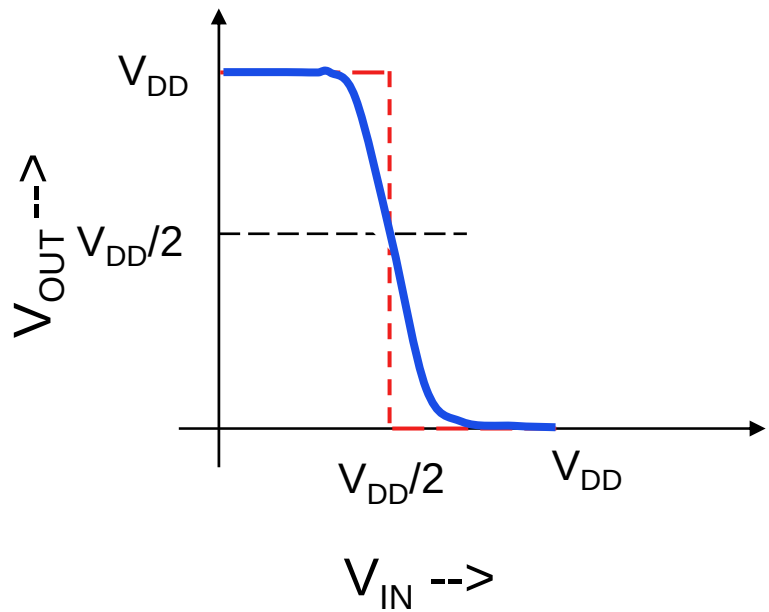
comparison to 65nm CMOS

parameter	65nm ITRS	Limit	65nm /Limit
E_s (aJ)	23	0.003	8000
τ (fs)	640	40	16
L (nm)	25 nm	1.5 nm	17
$\hat{n}_S$ (cm^{-2})	0.8 x 10^9	1.5 x 10^9	0.5
$E\tau$ (J-s)	1.5 x 10^{-29}	1.1 x 10^{-34}	136,000

circuit limits

minimum V_{DD}





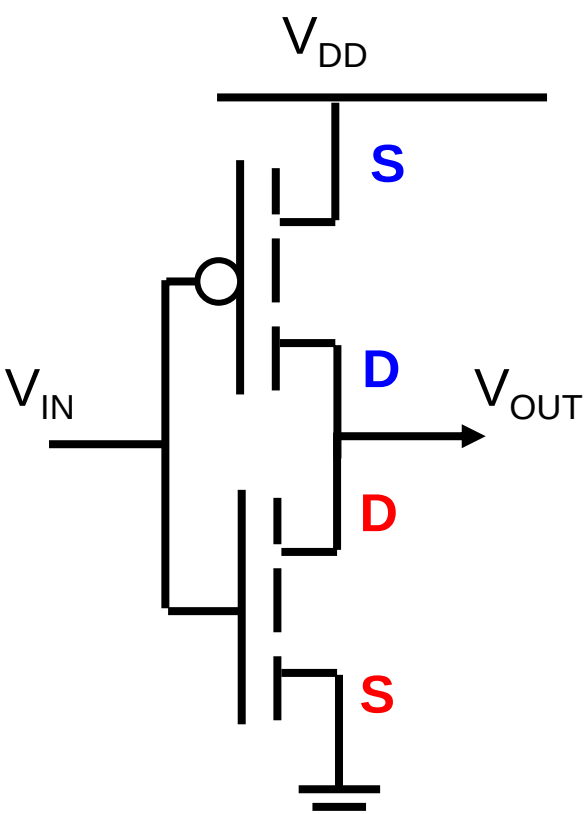
Question: What is the smallest V_{DD} for a CMOS inverter?

Answer: The smallest V_{DD} *that gives a gain > 1*

reference

J.D. Meindl and J.A. Davis, "*The* Fundamental Limit on Binary Switchin Energy for Terascale Integration, *IEEE J. Solid-State Circuits*, **35**, pp. 1515-1516, 2000.

minimum V_{DD}



assume subthreshold operation:

$$I_D = Ke^{q(V_{GS}-V_T)/mk_BT}\left(1-e^{-qV_{DS}/k_BT}\right)$$

$$I_{DN} = I_{DP} \rightarrow V_{out}\left(V_{in}\right)$$

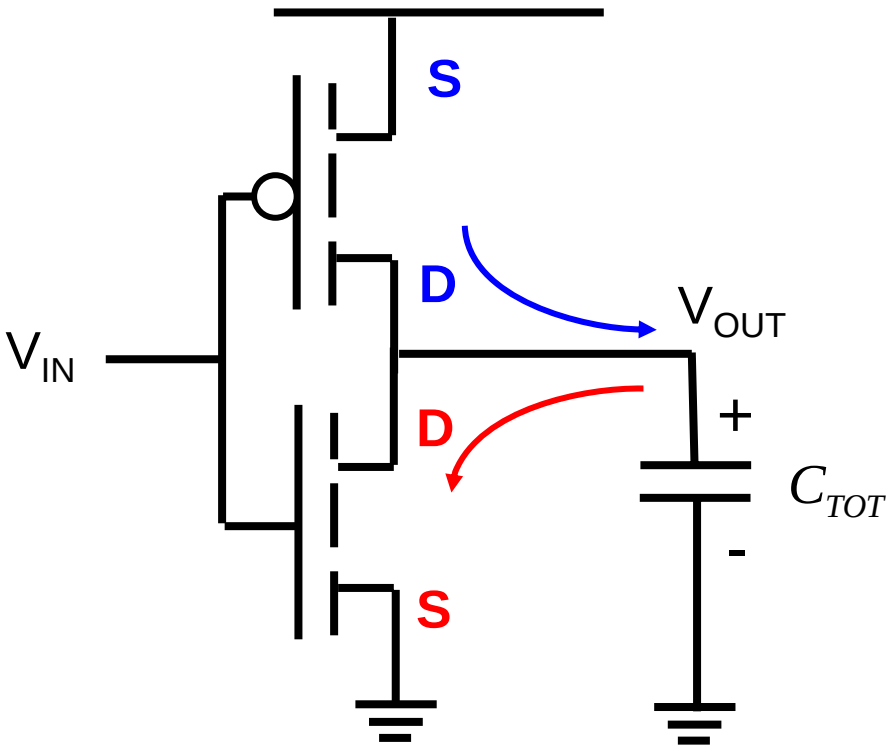
solve for $$A_V = \frac{dV_{out}}{dV_{in}} = f\left(V_{DD}\right)$$

$$\left|A_V\right| > 1 \Rightarrow V_{DD} > 2\ln(2)\frac{k_BT}{q}$$

$$V_{DD}\Big|_{\min} = 2\ln(2)\frac{k_BT}{q}$$

minimum switching energy

$$V_{DD}\big|_{\min} = 2\ln(2)k_B T / q$$



$$E_S = \frac{1}{2} C_{TOT} V_{DD}^2$$

$$E_S = \frac{1}{2} Q V_{DD}$$

$$Q\big|_{\min} = q$$

$$E_S = \frac{1}{2} Q\big|_{\min} V_{DD}\big|_{\min}$$

$$E_S = k_B T \ln(2)$$

outline

1) CMOS inverter
2) Speed
3) Power
4) Circuit performance
5) Metrics
6) Limits

   -device

   -circuit

summary

1) The CMOS inverter is a remarkable circuit
2) Speed is controlled by the on-current
3) Power is controlled by frequency and V_{DD}
4) Today, design is power-constrained.