EE-612:
Lecture 23:
RF CMOS

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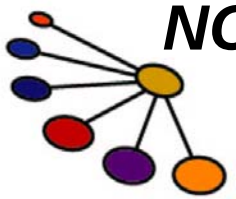

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why analog /RF why CMOS?

many applications involve analog / rf signals:

1) many natural signals are analog (sensors)
2) disk drive electronics
3) wireless receivers
4) optical receivers
5) microprocessors / memories

CMOS:

1) many systems are both analog and digital
2) CMOS is the dominate technology for digital electronics
3) CMOS performance has recently become suitable for analog

Reference: B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.

CMOS device metrics (digital)

1) on-current: I_{ON}

2) off-current: I_{OFF}

3) subthreshold swing: $S = \partial\left(\log_{10} I_D\right)\Big/\partial V_{GS}\Big|_{V_{DS}}$

4) device delay: $\tau = C_G V_{DD} / I_{ON}$

5) DIBL, etc.

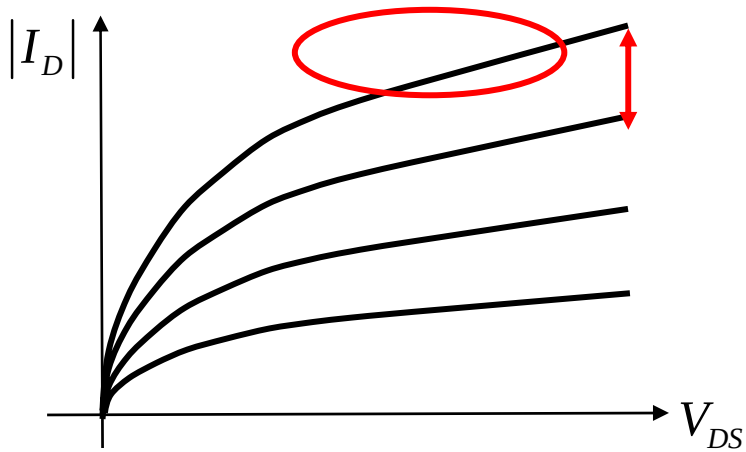
CMOS device metrics (analog)

1) transconductance: $g_m = \partial I_D / \partial V_{GS}\big|_{V_{DS}}$

2) output resistance: $r_o = \partial I_D / \partial V_{DS}\big|_{V_{GS}}$

3) f_T and f_{max}: $f_T = 1/2\pi\tau$

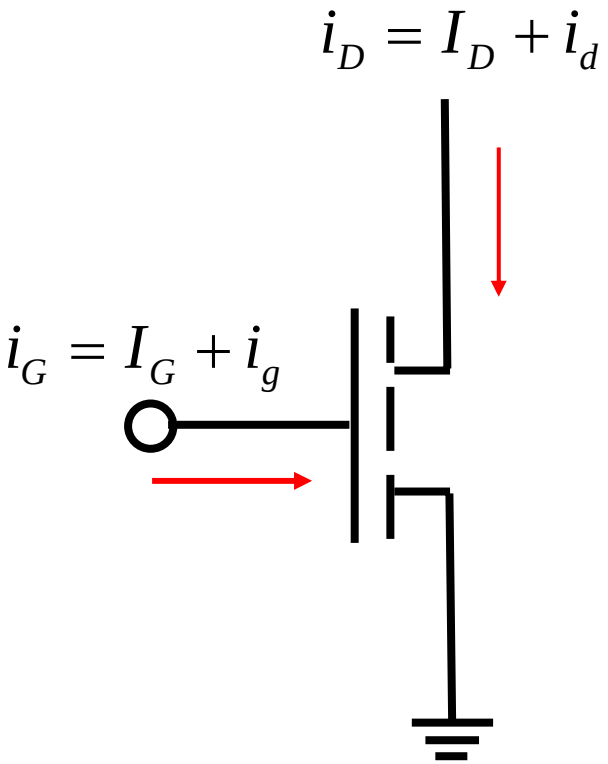
4) noise, mismatch, linearity, etc.

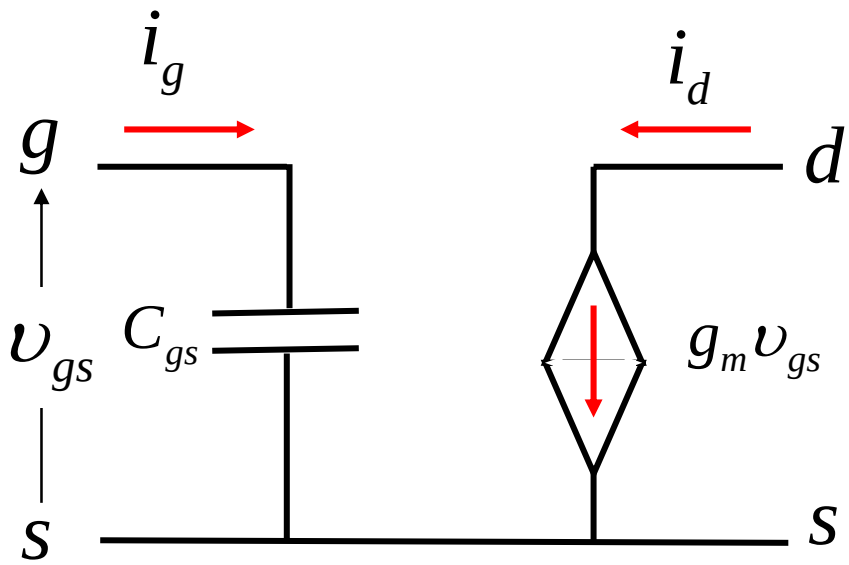


outline

1) Introduction
2) **Small signal model**
3) Transconductance
4) Self-gain
5) Gain bandwidth product
6) Unity power gain
7) Noise, mismatch, linearity…
8) Examples

small signal model

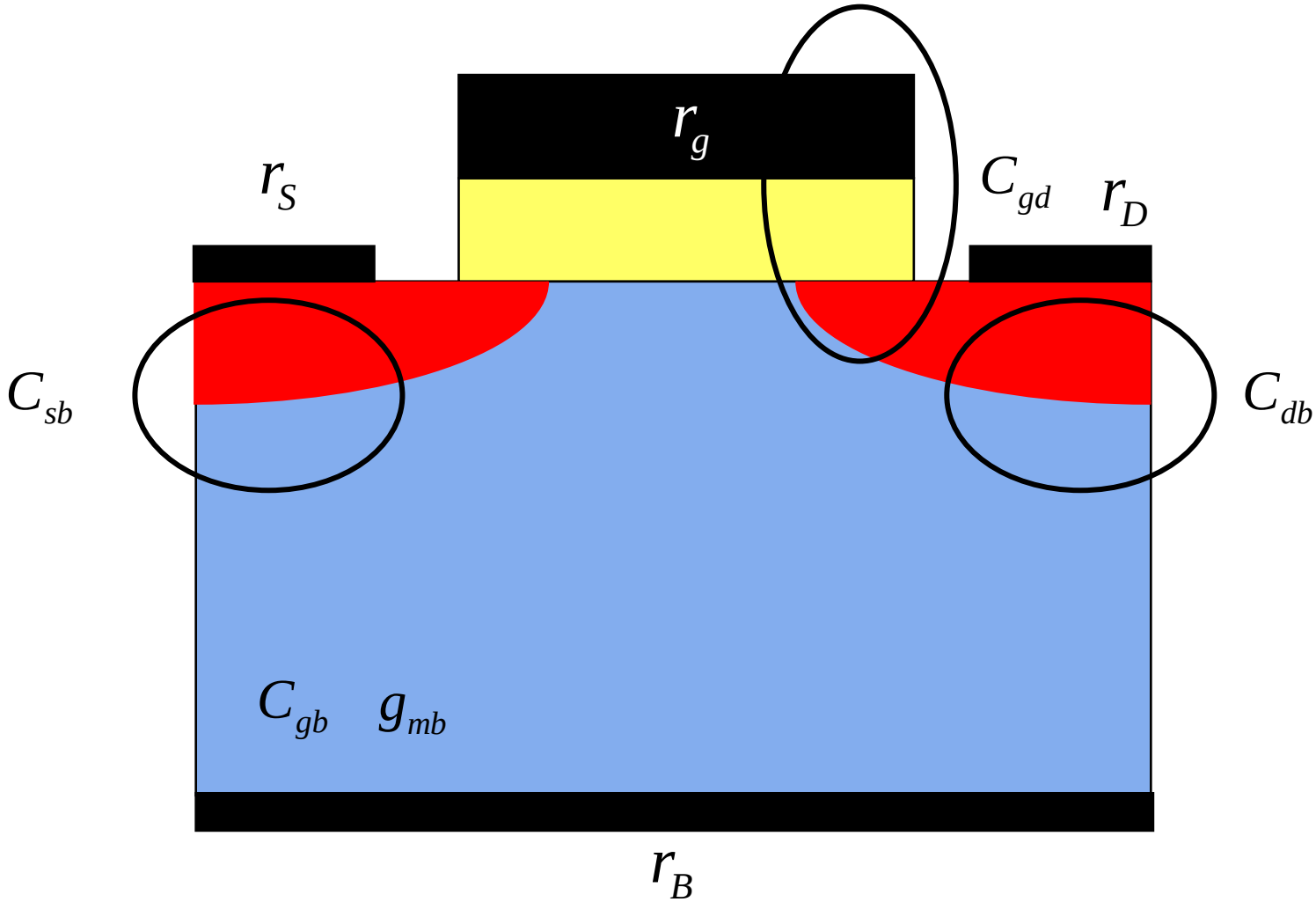




$$i_d = g_m \upsilon_{gs} \qquad g_m = \frac{i_d}{\upsilon_{gs}} \approx \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}}$$

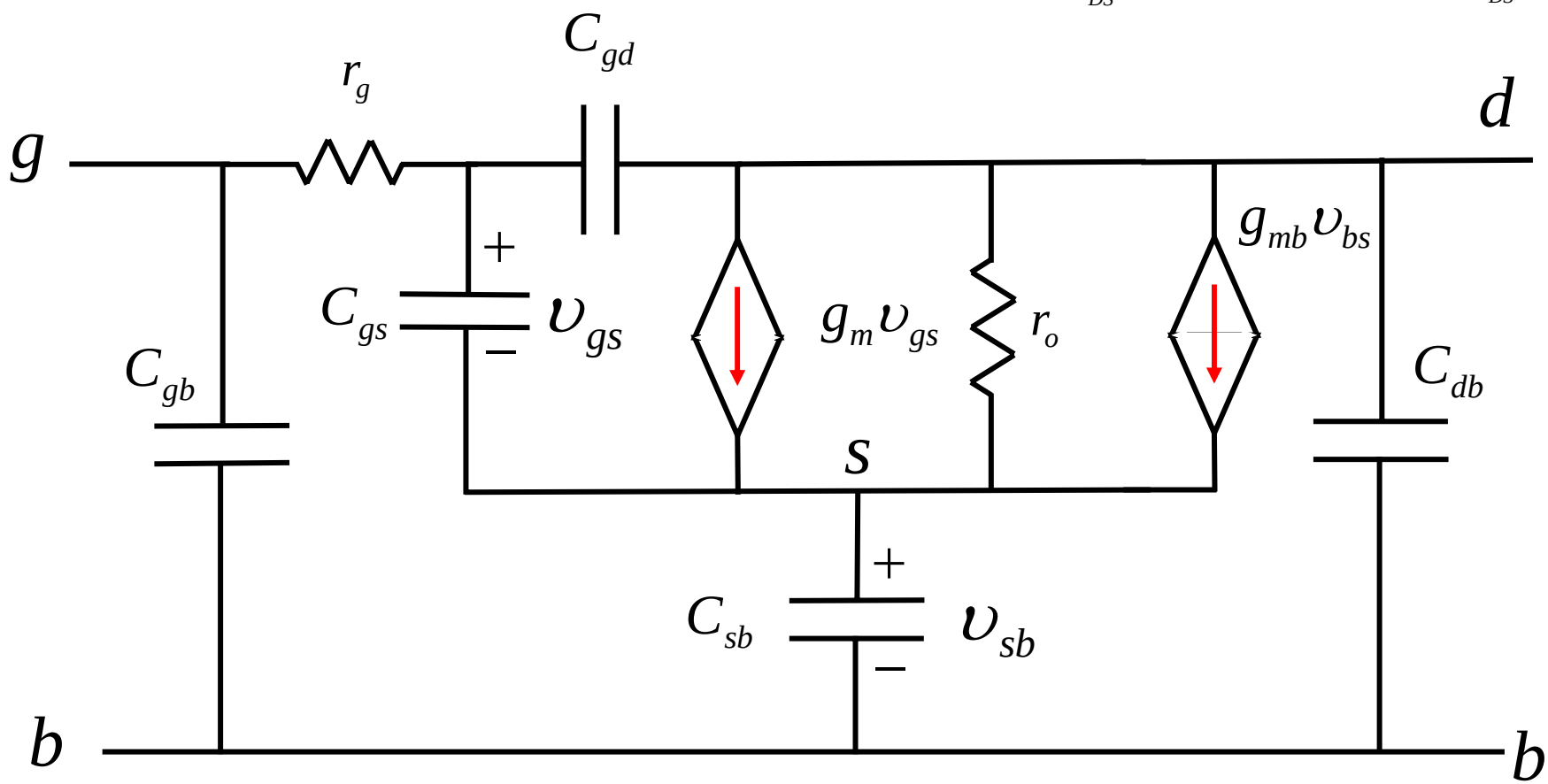
(quasi-static assumption)

additional parameters in the s.s. model



small signal model (ii)

$$r_o = \partial I_D / \partial V_{DS}\big|_{V_{DS}} \qquad g_{mb} = \partial I_D / \partial V_{BS}\big|_{V_{DS}}$$



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transconductance

MOS (above V_T, saturated)

$$g_m = \partial I_D / \partial V_{GS}\big|_{V_{DS}}$$

$$I_D = WC_{ox}\upsilon_{sat}\left(V_{GS} - V_T\right)$$

$$g_m = WC_{ox}\upsilon_{sat}$$

$$g_m / I_D = 1/\left(V_{GS} - V_T\right)$$

$$g_m / I_D = 1/\left(1.1 - 0.17\right) \approx 1 \text{ V}^{-1}$$

(65 nm HP)

bipolar

$$g_m = \partial I_C / \partial V_{BE}\big|_{V_{CE}}$$

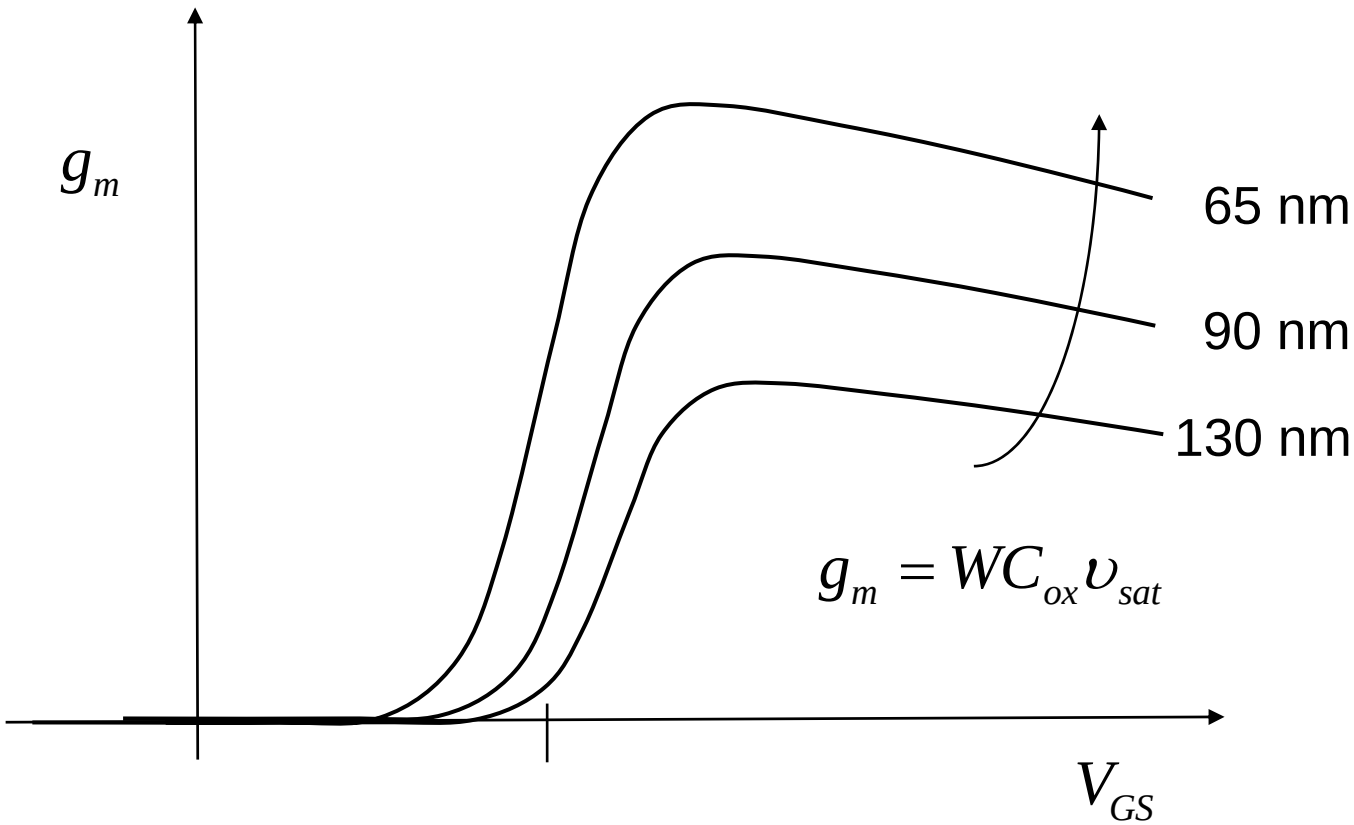
$$I_C = I_{C0} e^{qV_{BE}/k_B T}$$

$$g_m = I_C / \left(k_B T / q\right)$$

$$g_m / I_C = 1/\left(k_B T / q\right)$$

$$g_m / I_C = 1/\left(0.026\right) \approx 40 \text{ V}^{-1}$$

MOSFET transconductance



T_{ox} scaling, high-k, mobility improvements (e.g. strain) increase g_m.

transconductance (subthreshold)

MOS (below V_T, saturated)

$$g_m = \partial I_D / \partial V_{GS}\big|_{V_{DS}}$$

$$I_D = I_{OFF} e^{qV_{GS}/mk_BT}$$

$$g_m = I_D / \left(mk_BT / q\right)$$

$$g_m / I_D = 1 / \left(mk_BT / q\right)$$

$$g_m / I_D = 1 / 1.3\left(0.026\right) \approx 30 \text{ V}^{-1}$$

bipolar

$$g_m = \partial I_C / \partial V_{BE}\big|_{V_{CE}}$$

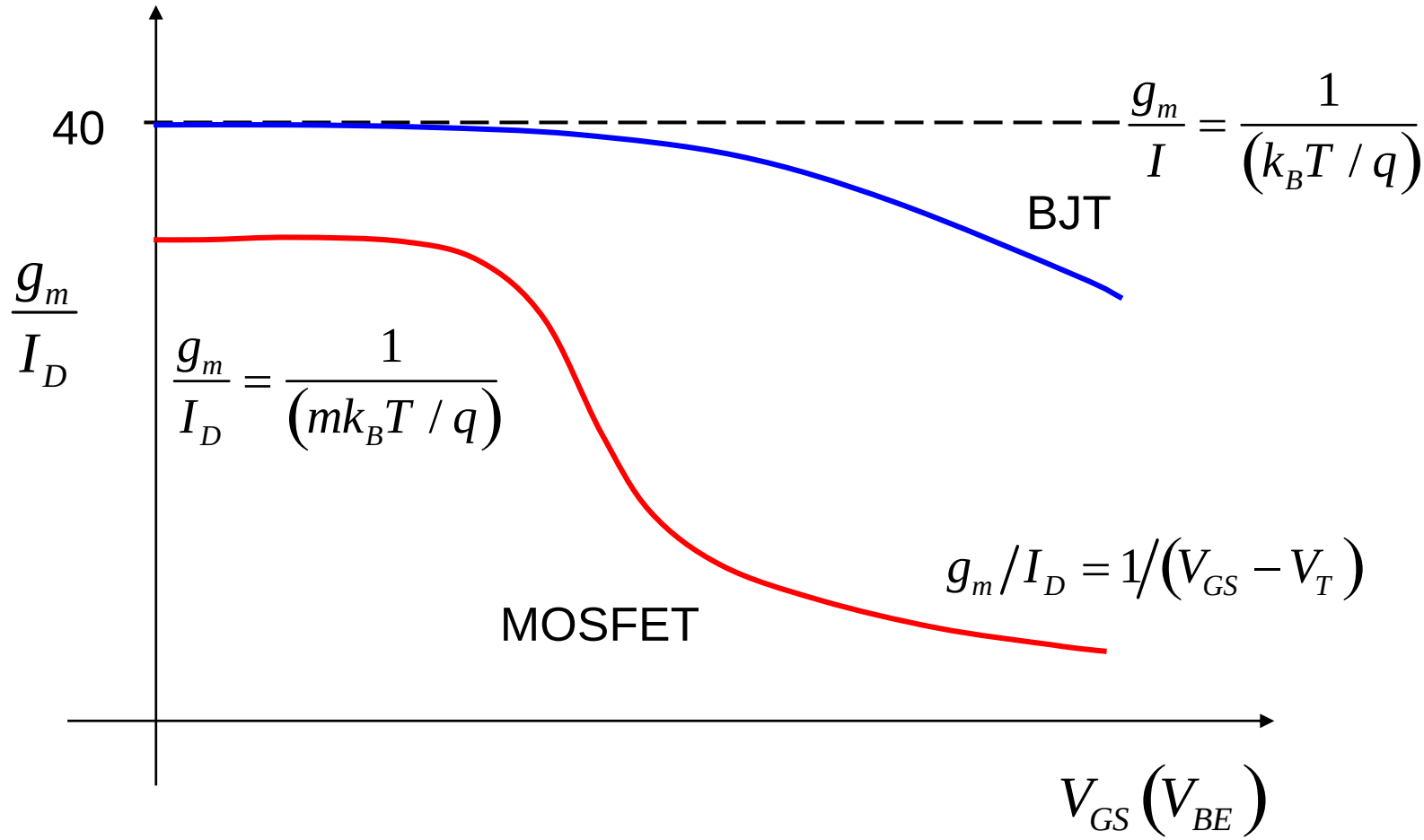
$$I_C = I_{C0} e^{qV_{BE}/k_BT}$$

$$g_m = I_C / \left(k_BT / q\right)$$

$$g_m / I_C = 1 / \left(k_BT / q\right)$$

$$g_m / I_C = 1 / \left(0.026\right) \approx 40 \text{ V}^{-1}$$

g_m / I_D figure of merit



B. Murmann, P. Nikaeen, D.J. Connelly, and R. W. Dutton, “Impact of Scaling in Analog Performance and Associated Modeling Needs, *IEEE Trans. Electron Dev*., 2006.

Outline

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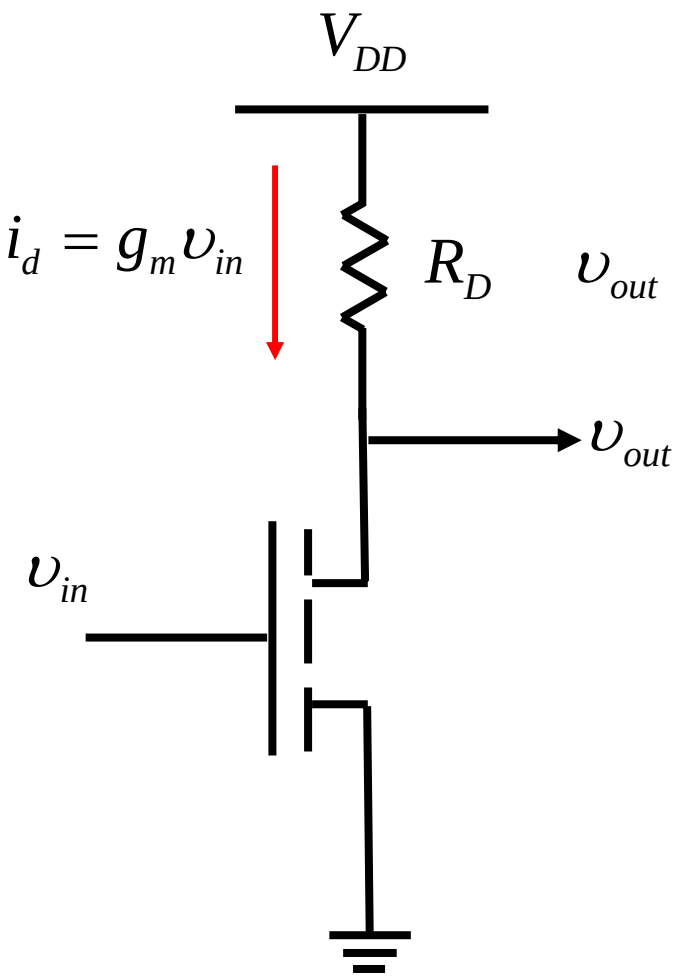
4) **Self-gain**
5) Gain bandwidth product
6) Maximum power gain
7) Noise, mismatch, linearity
8) Examples

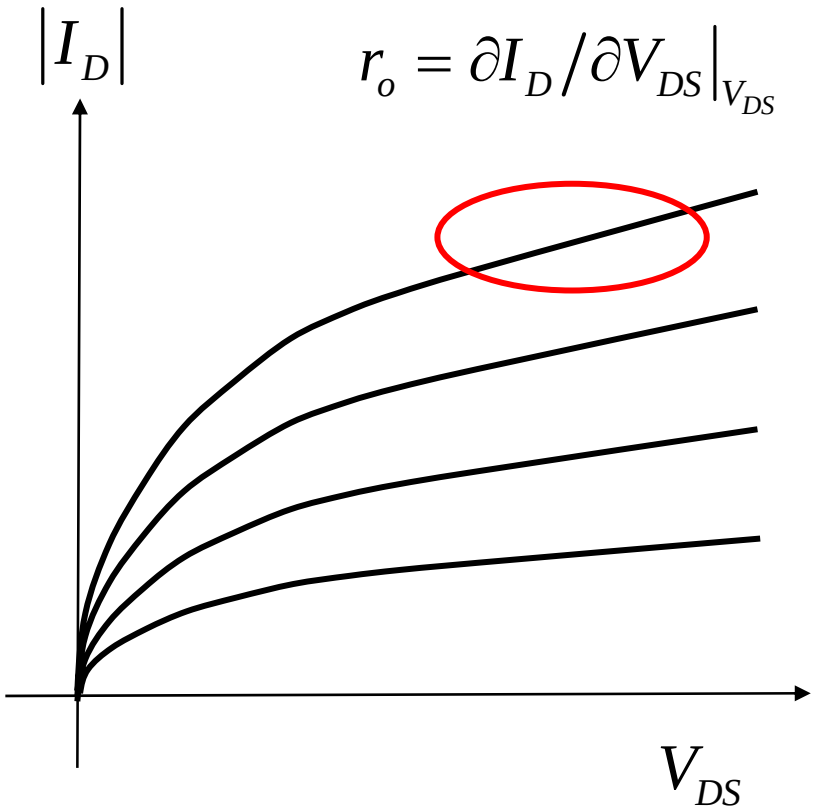
small signal gain

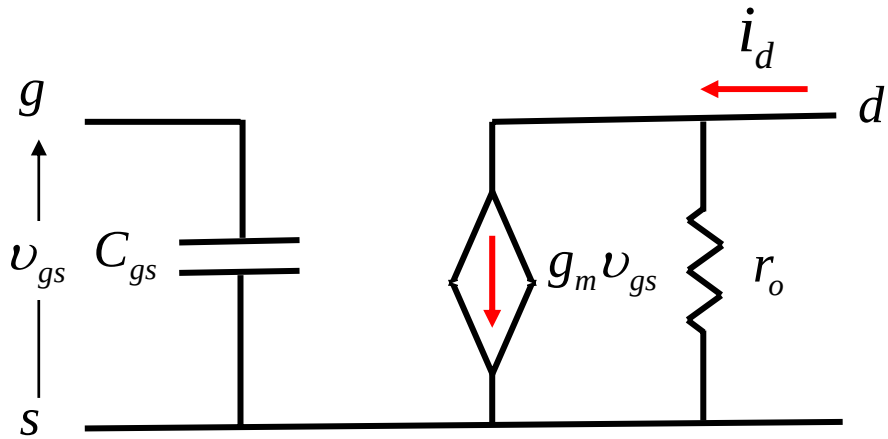


$$\upsilon_{out} = -g_m \upsilon_{in} R_D$$

$$\frac{\upsilon_{out}}{\upsilon_{in}} = A_\upsilon = -g_m R_D$$

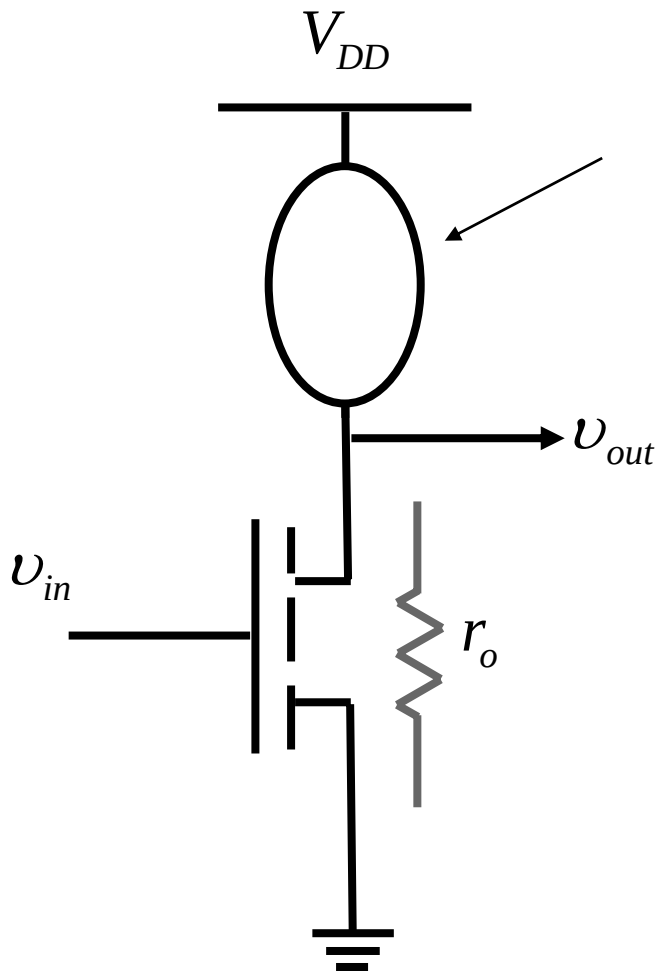
effect of output resistance





$$A_\upsilon = -g_m R_D \| r_o$$

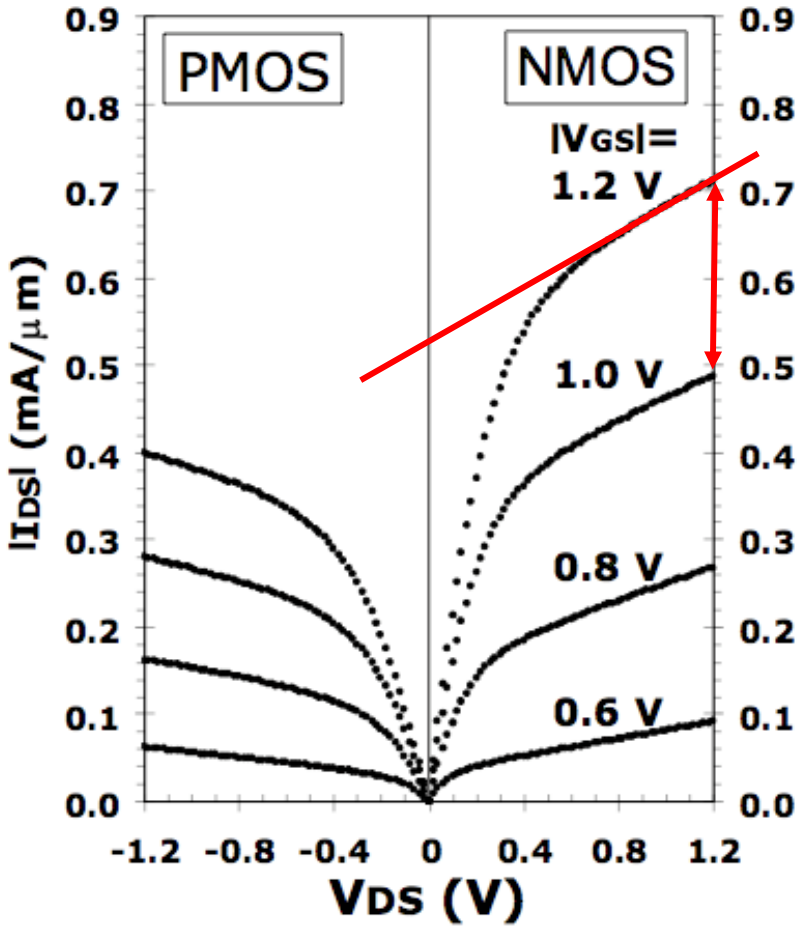
self-gain



high impedance current source

$$A_\upsilon(\max) = -g_m r_o$$

self-gain for 65 nm digital CMOS



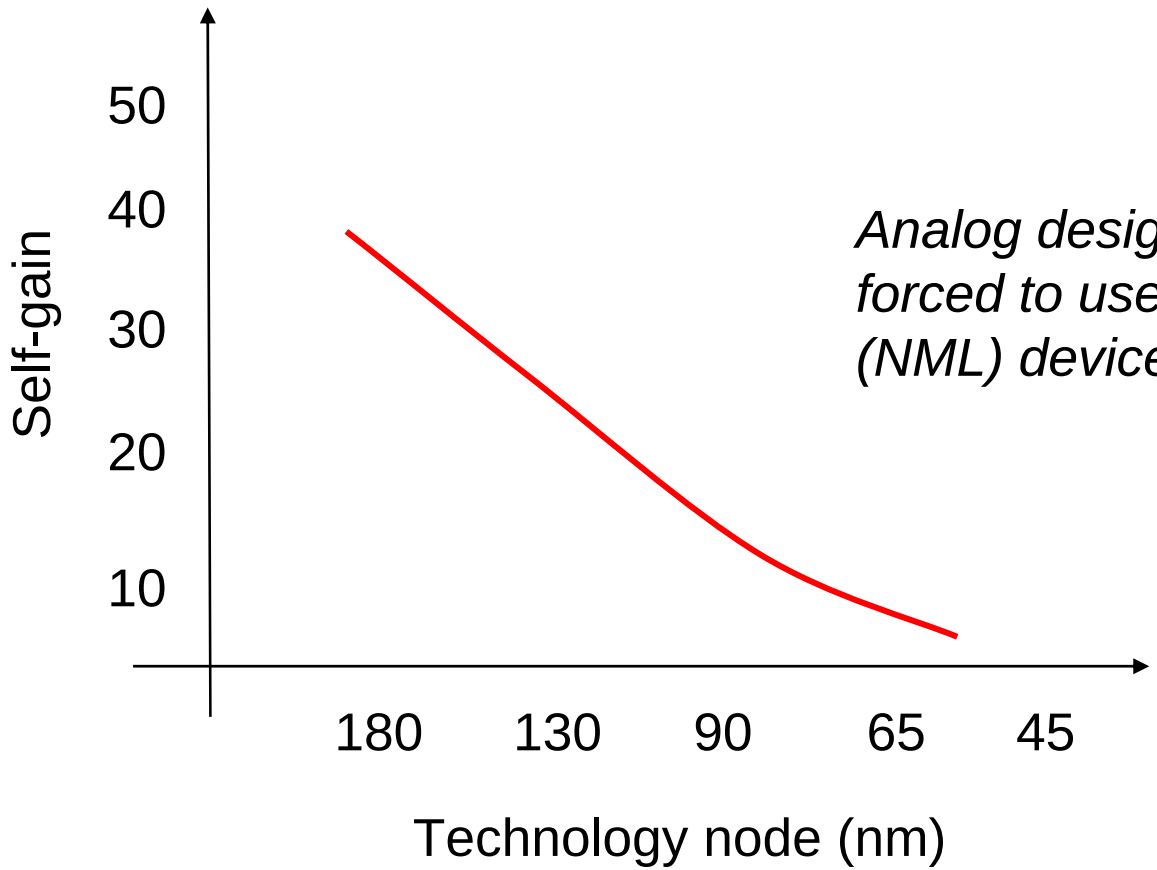
$$g_m \approx \frac{0.2\ \text{mA}/\mu\text{m}}{0.2\ \text{V}} = 1\ \text{mS}/\mu\text{m}$$

$$r_o \approx \frac{1.2\ \text{V}}{0.18\ \text{mA}/\mu\text{m}} \approx 7\ \text{Kž}\ \text{-}\mu\text{m}$$

$$\left|A_\upsilon(\max)\right| = g_m r_o \approx 7$$

C.-H. Jan. et al., 2005 IEDM

self-gain vs. scaling



Analog designers are frequently forced to use non-minimum length (NML) devices.

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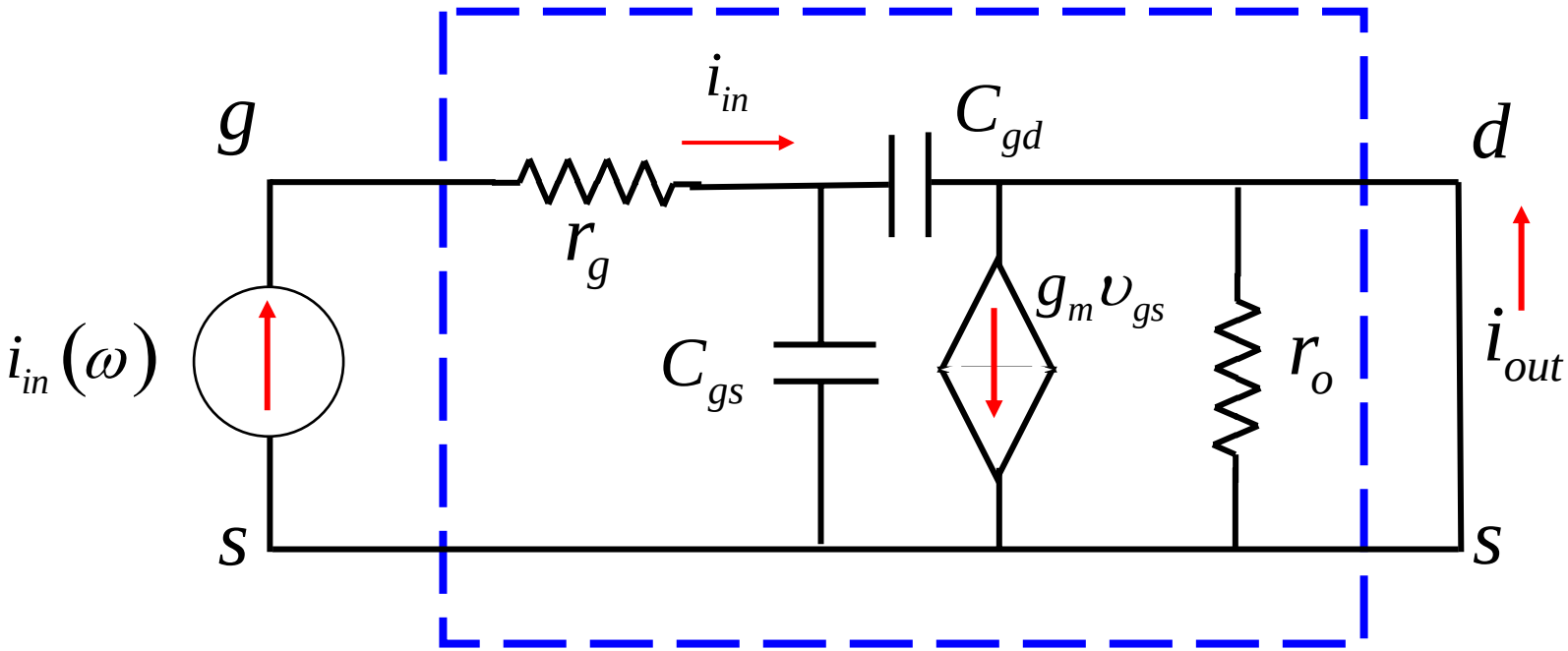
short-current current gain



$$i_{out} \approx g_m \upsilon_{gs}$$

$$\upsilon_{gs} = i_{in} \frac{1}{j\omega\left(C_{gs} + C_{gd}\right)}$$

$$i_{out} \approx \frac{g_m}{j\omega C_{TOT}} i_{in}$$

(should include C_{gb} too)

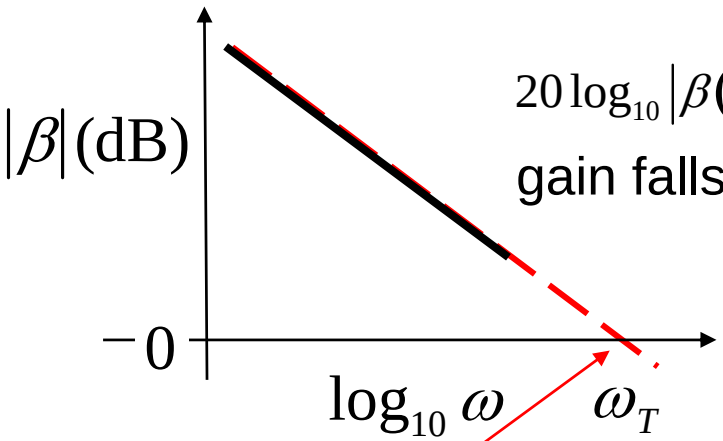
gain-bandwidth product

$$i_{out} \approx \frac{g_m}{j\omega C_{TOT}} i_{in}$$

$$\left|\beta(\omega_T)\right| = 1 = \frac{g_m}{\omega_T C_{TOT}}$$

$$\left|\beta(\omega)\right| \approx \frac{g_m}{\omega C_{TOT}}$$

$$f_T = \frac{g_m}{2\pi C_{TOT}}$$



$$20\log_{10}\left|\beta(\omega)\right| = C - 20\log_{10}\omega$$

gain falls at 20 dB per decade

'extrapolated ω_T'

gain-bandwidth product (ii)

$$\omega_T = \frac{g_m}{C_{TOT}}$$

$$g_m \approx WC_{ox}\upsilon_{SAT}$$

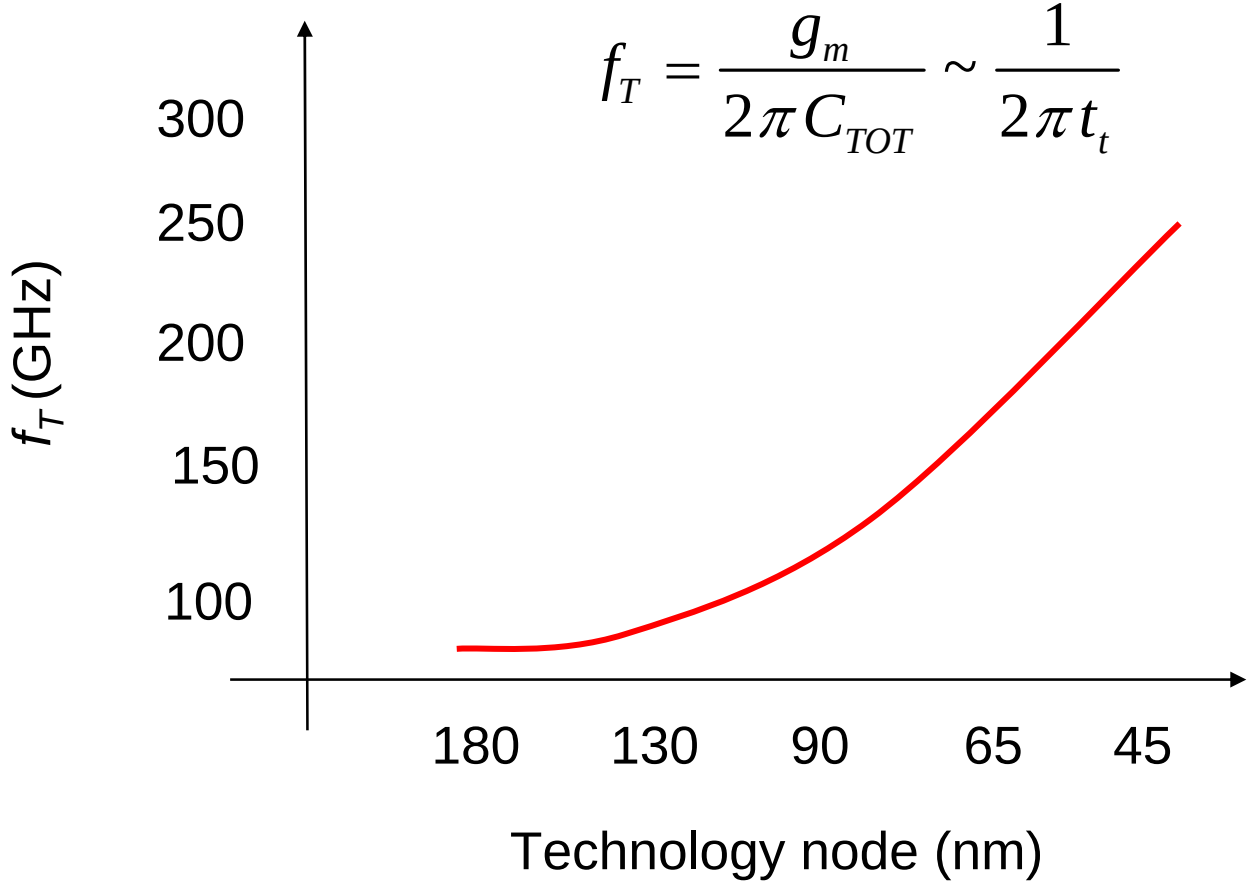
$$C_{TOT} \approx WLC_{ox}$$

$$\omega_T \approx \frac{\upsilon_{SAT}}{L} = \frac{1}{t_t}$$

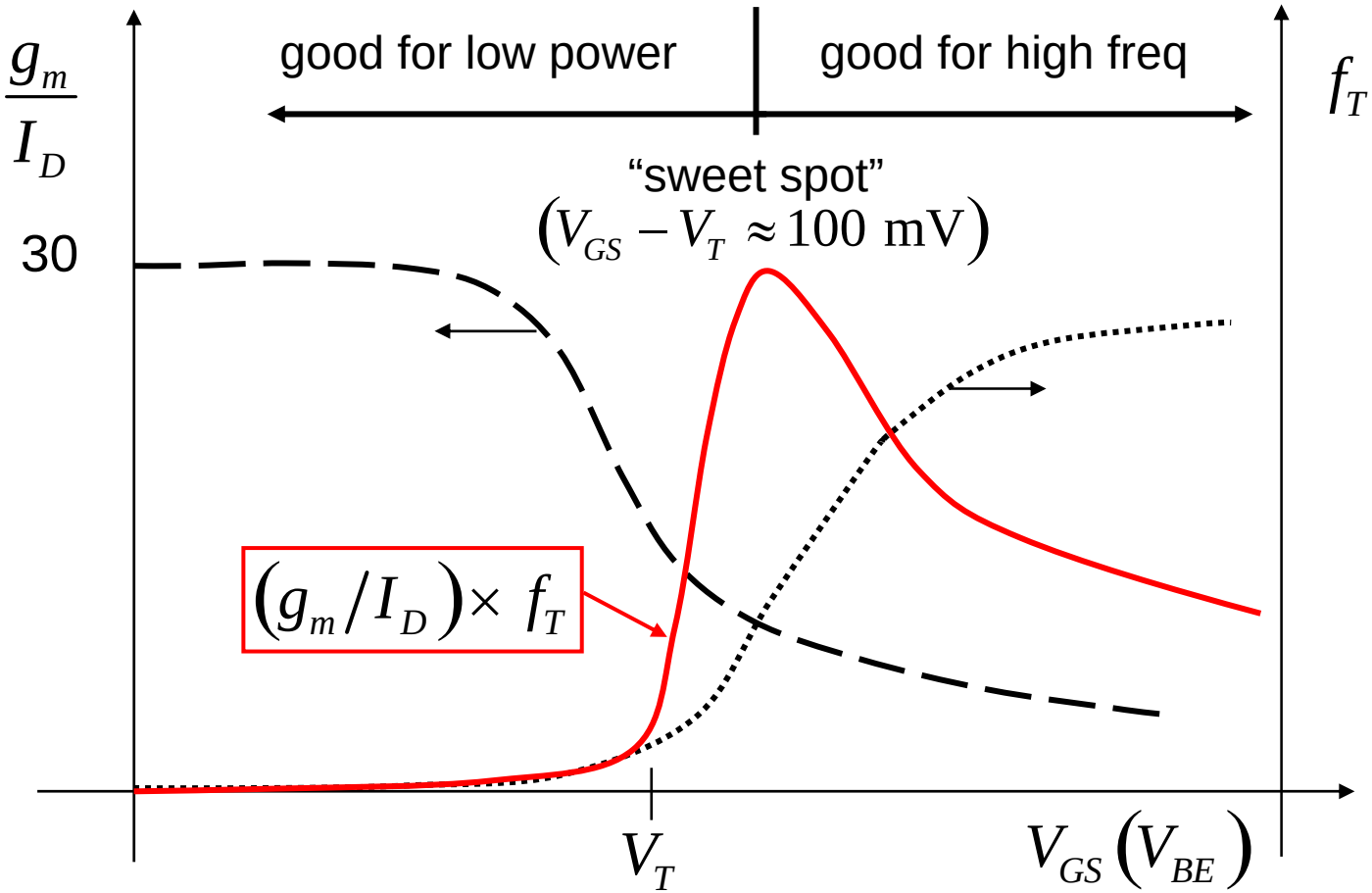
ω_T (f_T) is independent of W and increases as channel length, L, decreases

f_T vs. scaling

$$f_T = \frac{g_m}{2\pi C_{TOT}} \sim \frac{1}{2\pi t_t}$$



$g_m / I_D \times f_T$



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f_{max}

$$f_T = \frac{g_m}{2\pi C_{TOT}}$$

insensitive to r_g and r_o

independent of W

channel length scaling increases f_T

another figure of merit is f_{MAX}, the *maximum frequency of oscillation* or the *unity power gain*

$$f_{MAX} \approx \frac{\omega_T}{\sqrt{4r_g\left(\frac{1}{r_o} + \omega_T C_{gd}\right)}}$$

sensitive to parasitics

- $-r_g$ $\sim W$
- $-r_o$ $\sim 1/W$
- $-C_{gd} \sim W$

$f_{MAX} \sim 1/W$, need small W

channel length scaling increases r_g and lowers r_o

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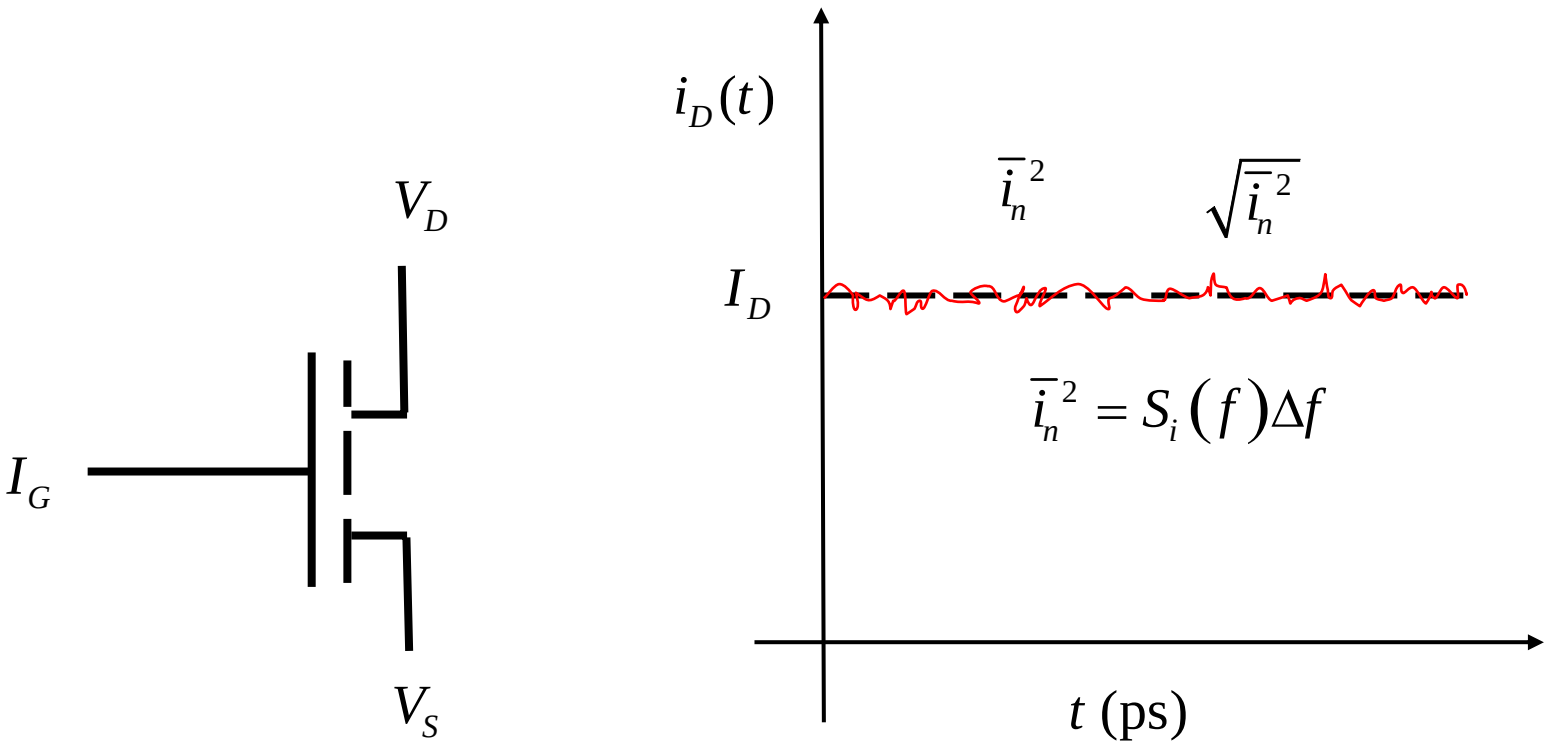
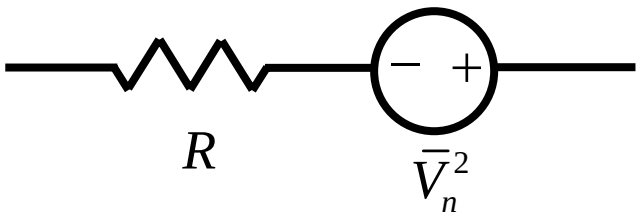
noise


V_D
I_G
V_S
$i_D(t)$
$\overline{i_n^2}$
$\sqrt{\overline{i_n^2}}$
I_D
$\overline{i_n^2} = S_i(f)\Delta f$
t (ps)

thermal noise

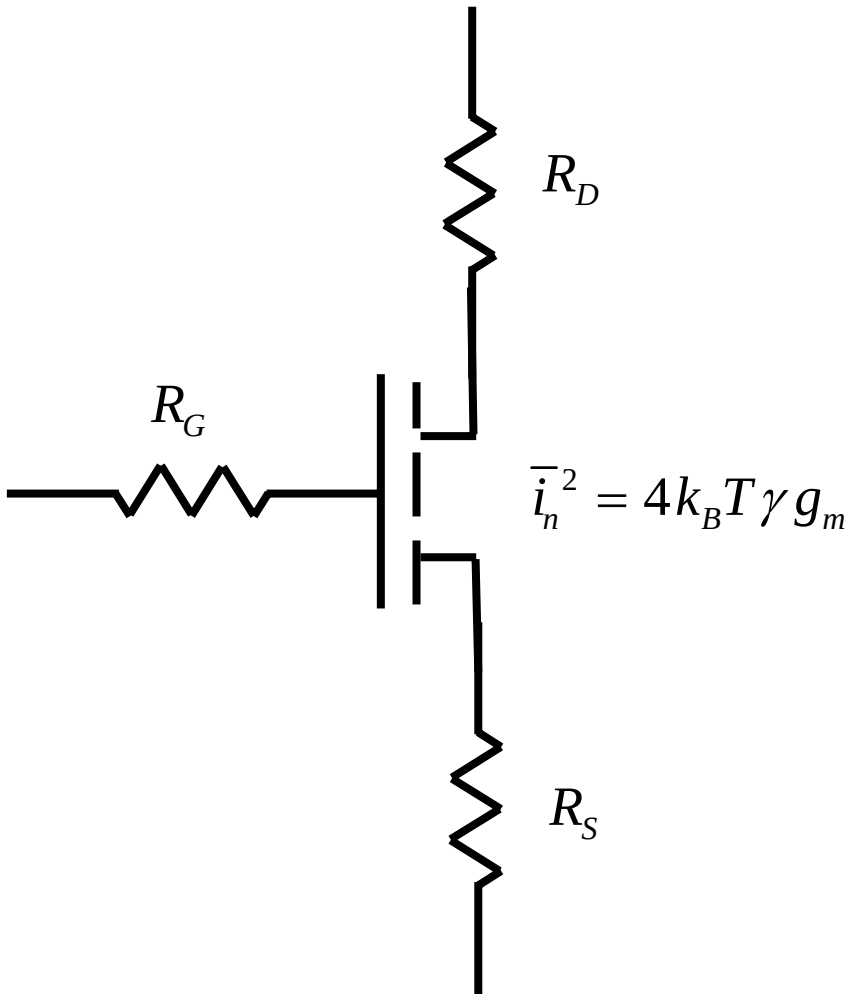
thermal noise

Johnson noise

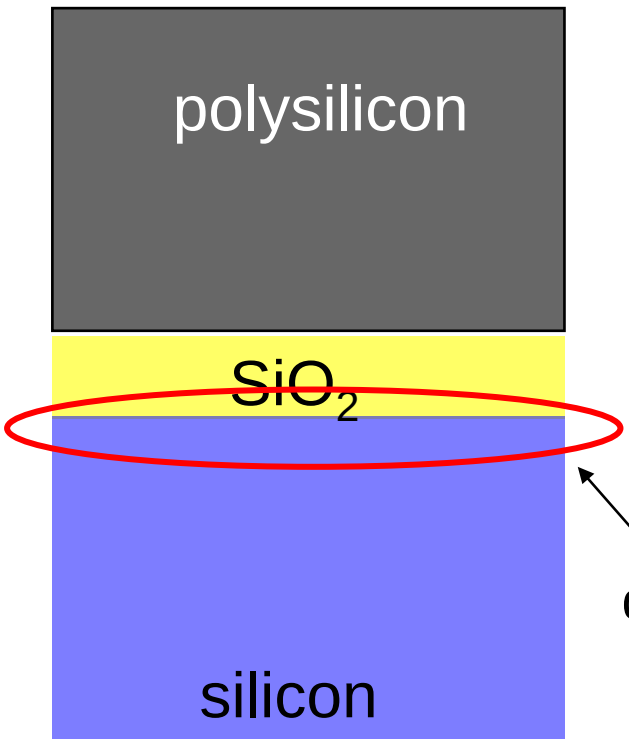


$$\bar{V}_n^2 = S_f(f)\Delta f = 4k_B T R \Delta f$$

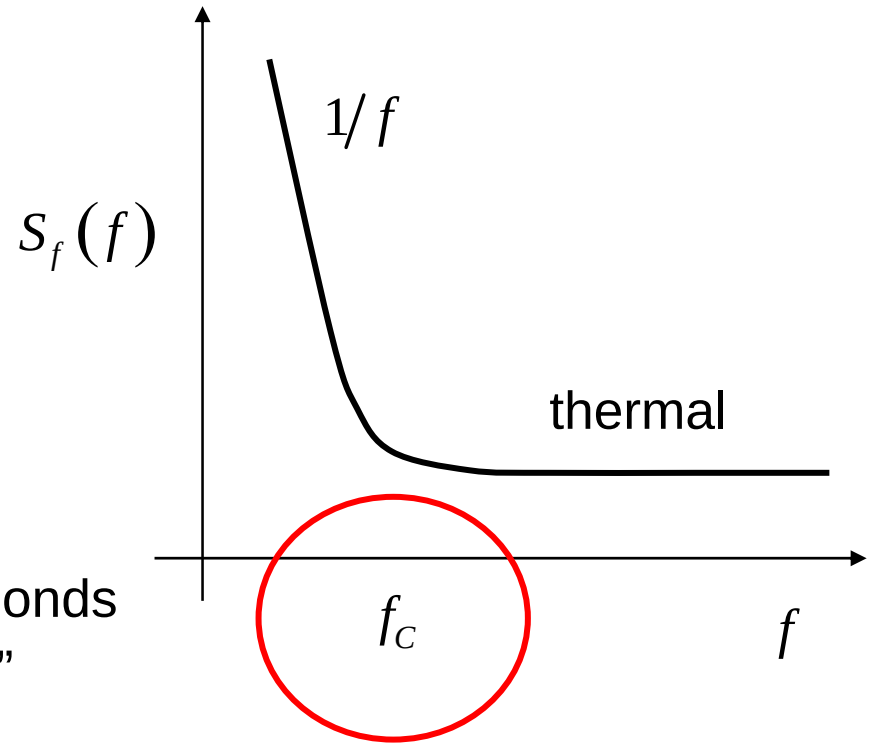
"white noise"



1/f "flicker" noise



dangling bonds
"traps"

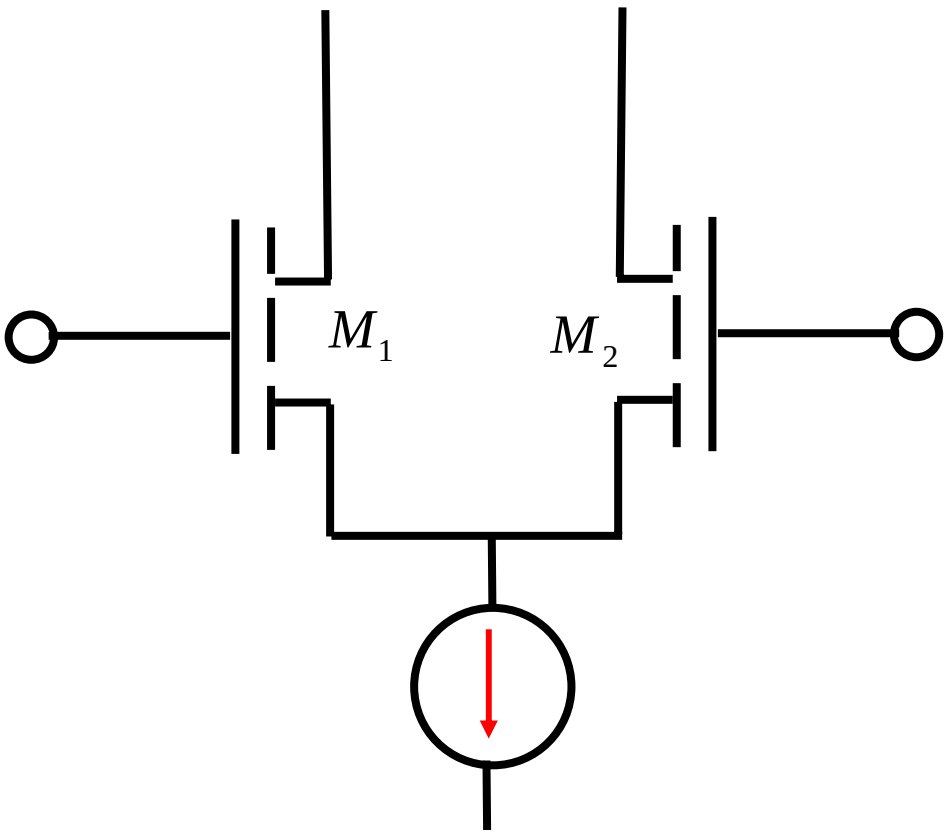


corner frequency

$f_C \approx 100$ kHz

mismatch

differential pair



analog circuits make use of matched transistors

sources of mismatch:

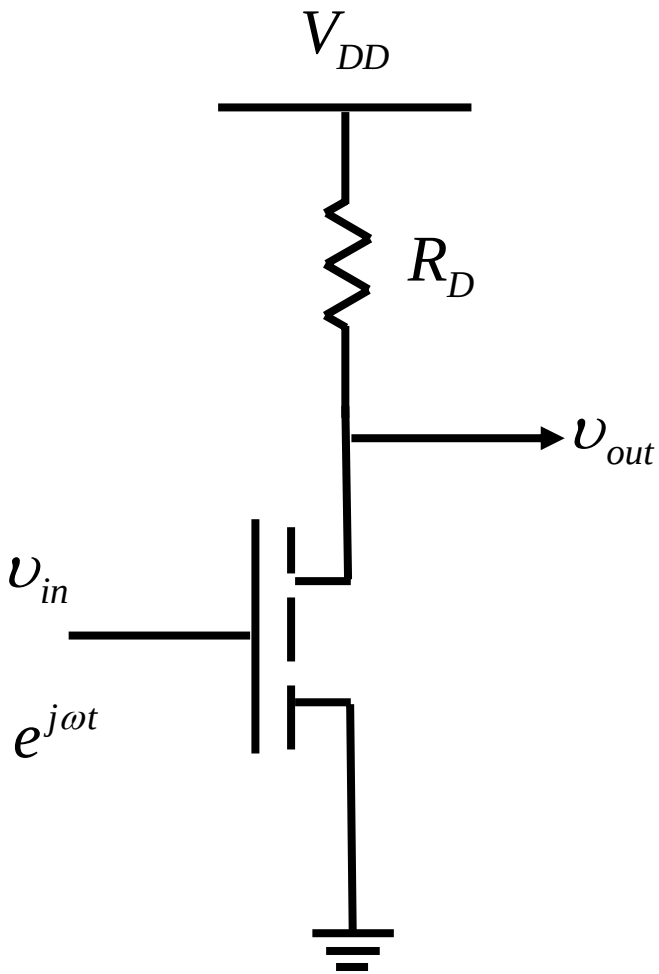
-variations in geometry
-ΔV_T, ΔT_{ox} , ...
-thermal effects, etc.

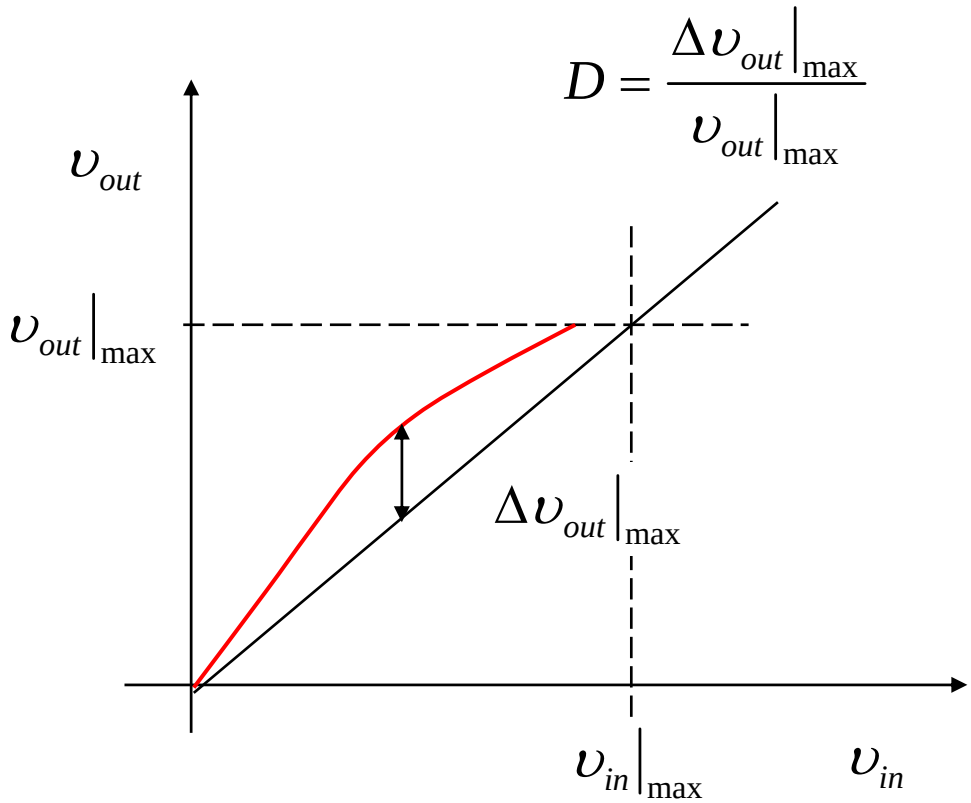
$$\Delta A = \frac{K}{\sqrt{WL}}$$

dealing with mismatch:

-circuit design
-careful layout

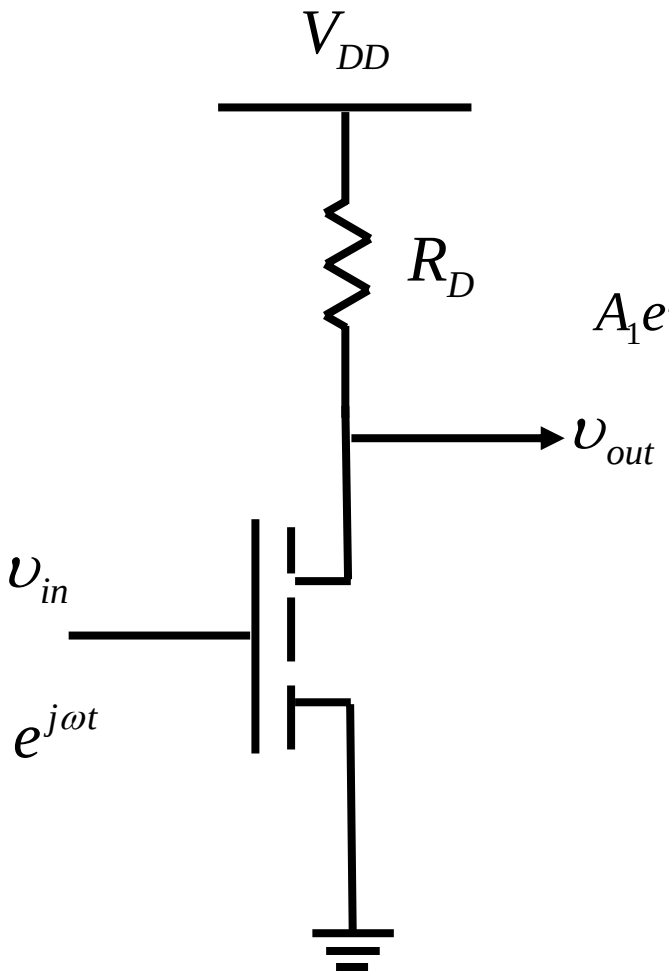
linearity





(below threshold)

harmonic distortion



$$A_1 e^{j\omega t} + A_2 e^{j2\omega t} + A_3 e^{j3\omega t} + \ldots$$

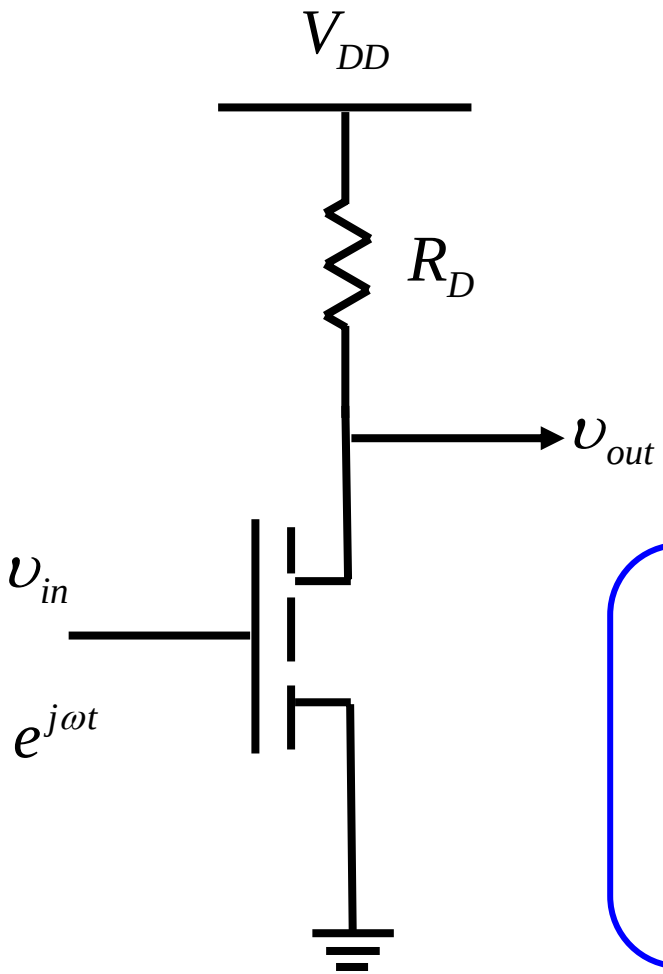
$$i_d = \frac{\partial I_D}{\partial V_{gs}} \upsilon_{gs} + \frac{1}{2!}\frac{\partial^2 I_D}{\partial V_{gs}^2} \upsilon_{gs}^2 + \frac{1}{3!}\frac{\partial^3 I_D}{\partial V_{gs}^3} \upsilon_{gs}^3 + \ldots$$

$$i_d = g_{m1}\upsilon_{gs} + g_{m2}\upsilon_{gs}^2 + g_{m2}\upsilon_{gs}^3 + \ldots$$

VIP_2 $\quad$ VIP_3

extrapolated gate voltage amplitude at which the amplitude of the harmonic = amplitude of fundamental

distortion and the devices



$$A_1 e^{j\omega t} + A_2 e^{j2\omega t} + A_3 e^{j3\omega t} + \ldots$$

$$i_d = \frac{\partial I_D}{\partial V_{gs}}\upsilon_{gs} + \frac{1}{2!}\frac{\partial^2 I_D}{\partial V_{gs}^2}\upsilon_{gs}^2 + \frac{1}{3!}\frac{\partial^3 I_D}{\partial V_{gs}^3}\upsilon_{gs}^3 + \ldots$$

$I_D \sim (V_{GS} - V_T)^{\alpha}$ (above threshold)

DIBL

$I_D \sim e^{qV_{GS}/k_BT}$ (below threshold)

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7) Noise, mismatch, linearity…
8) **Recent examples**

IEDM 2007

"Record RF Performance of 45-nm SOI CMOS Technology," by Sungjae Lee, et al., IBM.

45 nm SOI technology
1.16 nm gate oxide
strained Si technology

Sungjae Lee, et al. IEDM 2007

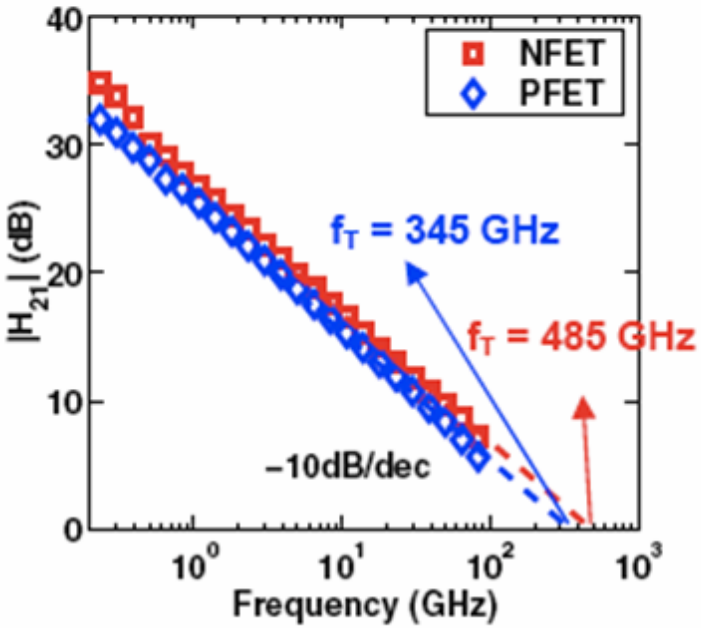

Fig. 2. Current gain $|H_{21}|$ from measured S-parameters for 30 µm wide (1 µm by 30 gate fingers) SOI NFET (L_{poly} =29 nm) and SOI PFET (L_{poly} =31 nm) with relaxed poly pitch at V_{GS} = 0.6 (-0.6) V, V_{DS} =1.0 (-1.0) V.

$$f_T \approx \frac{1}{2\pi t_t}$$

$$t_{tN} < 0.33\ \text{ps} \quad \langle \upsilon \rangle_N > 8.8 \times 10^6\ \text{cm/s}$$

$$t_{tP} < 0.46\ \text{ps} \quad \langle \upsilon \rangle_P > 6.7\ \text{cm/s}$$

Sungjae Lee, et al. IEDM 2007

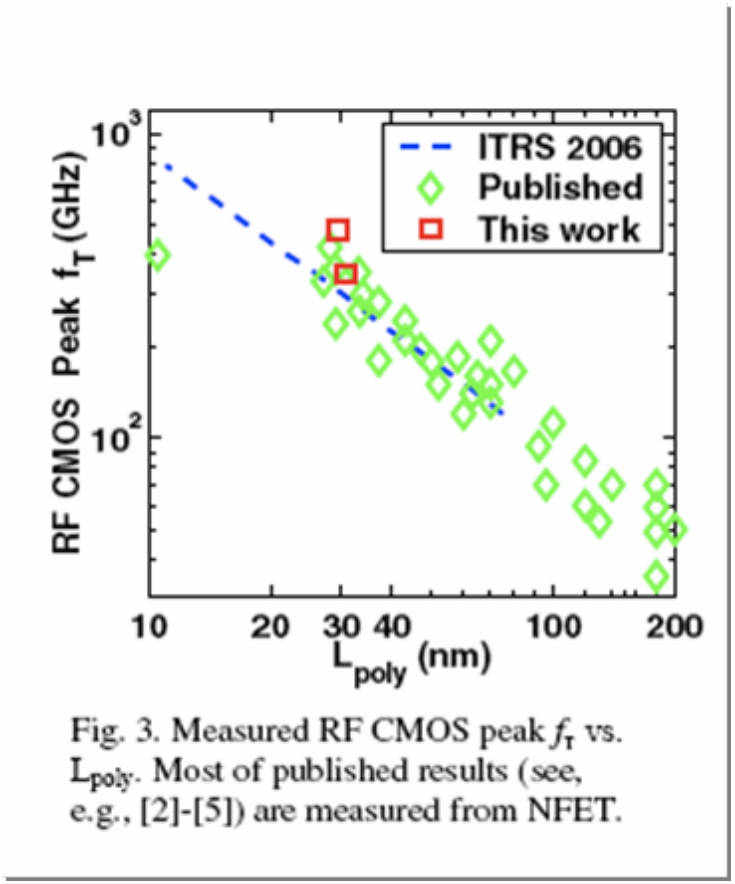

Fig. 3. Measured RF CMOS peak f_T vs. L_{poly}. Most of published results (see, e.g., [2]-[5]) are measured from NFET.

$$f_T = \frac{1}{2\pi t_t}$$

$$t_t = \frac{L}{\langle \upsilon \rangle}$$

$$L = 10 \text{ nm}, \langle \upsilon \rangle = 10^7 \text{ cm/s}$$

$$\rightarrow t_t = 0.1 \text{ ps}, \text{f}_\text{T} = 1.6 \text{THz}$$

$$f_T = \frac{g_m}{2\pi C_{TOT}}$$

Sungjae Lee, et al. IEDM 2007

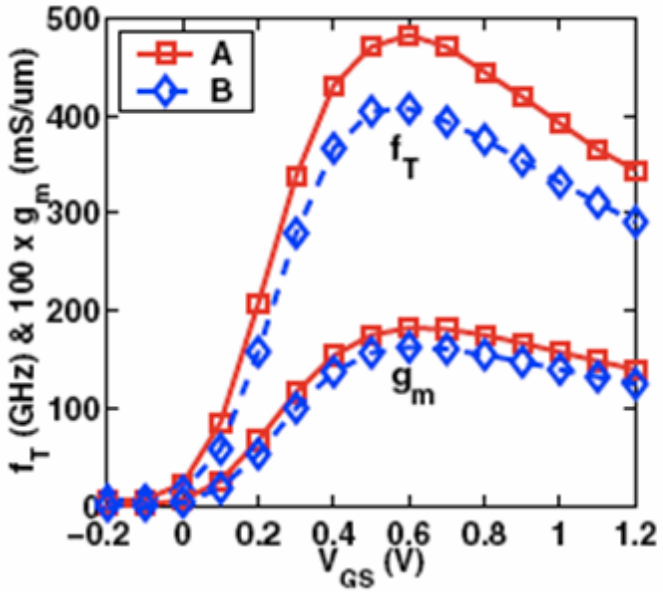

Fig. 4. Measured f_T and g_m vs. V_{GS} (at V_{DS} = 1.0 V) for 45-nm SOI NFET (L_{poly} =29 nm) with (A) relaxed poly pitch and (B) minimum poly pitch, obtained by extrapolating the value of $|H_{21}|$ at 10 GHz using -10 dB/dec slope after de-embedding.

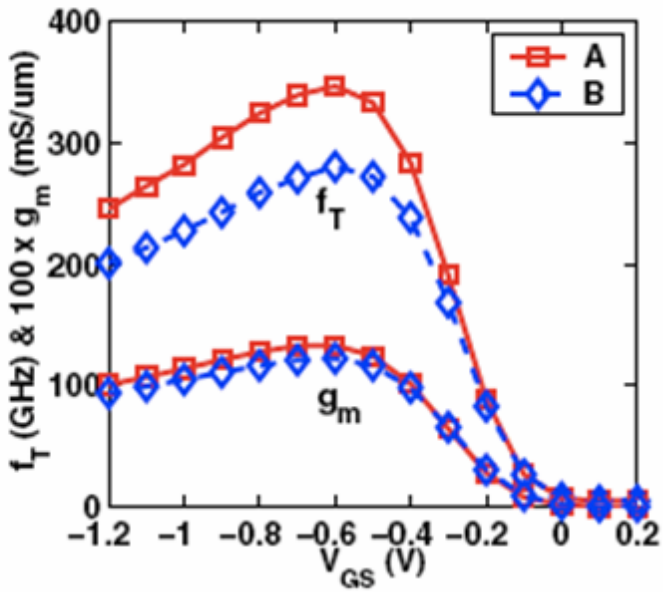

Fig. 5. Measured f_T and g_m vs. V_{GS} (at V_{DS} = -1.0 V) for 45-nm SOI PFET (L_{poly} =31 nm) with (A) relaxed poly pitch and (B) minimum poly pitch, obtained by extrapolating the value of $|H_{21}|$ at 10 GHz using -10 dB/dec slope after de-embedding.

$$f_T = \frac{g_m}{2\pi C_{TOT}}$$

Sungjae Lee, et al. IEDM 2007

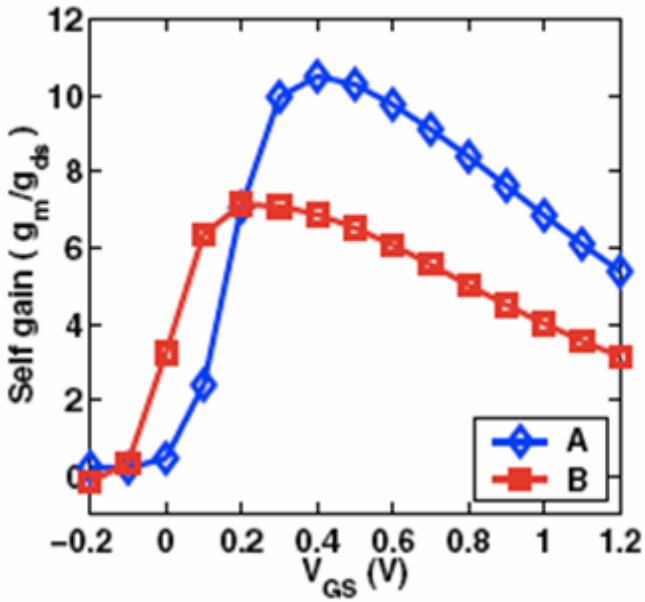

Fig. 11. Measured self-gain (= g_m/g_{ds}) vs. V_{GS} (at V_{DS} =1.0 V with body contact tied to the source) from S-parameter data at 10 GHz, comparing A: 13 µm(0.65 µm by 20 gate fingers), body-contacted SOI NFET with 46 nm L_{poly}, B: 12 µm (0.6 µm by 20 gate fingers), floating-body SOI NFET with 32 nm L_{poly}.

$$|A_V| = g_m r_o$$

IEDM 2007

"A 32nm CMOS Low Power SoC Platform Technology for Foundry Applications with Functional High Density SRAM," by Shien-Yang Wu, et al., Taiwan Semiconductor Manufacturing Company.

"A suitable SoC process technology needs to support both digital and analog functions with high density embedded memories."

Shien-Yang Wu, et al, IEDM 2007

"Potential 1/f noise degradation induced by gate oxide nitridation and local strain process has been one of the critical concerns in analog applications [8]. Gate oxide with different nitrogen profiles and strain process with different film stacks are studied."

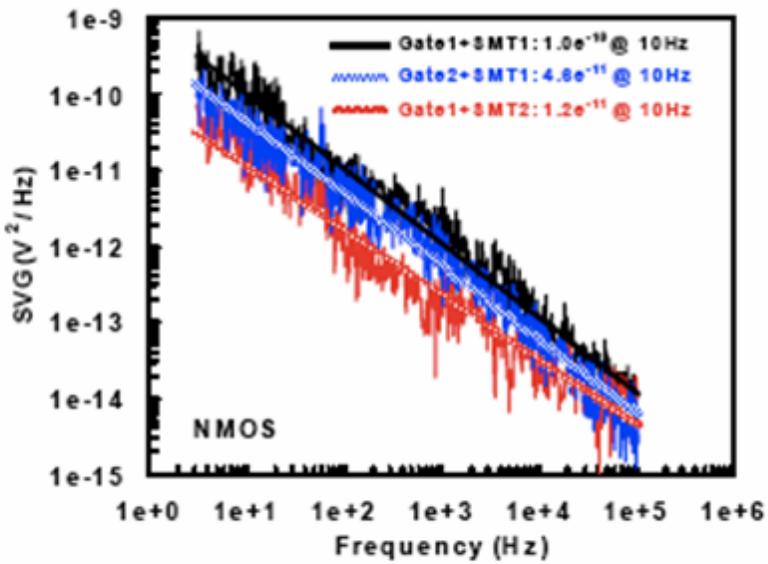

Fig. 8 (a) Comparison of NMOS 1/f noise for different combinations of gate oxide and strain process.

outline

1) Introduction
2) Small signal model
3) Transconductance
4) Self-gain
5) Gain bandwidth product
6) Unity power gain
7) Noise, mismatch, linearity…
8) Recent examples

references

1) Paul R. Gray and Robert G. Meyer, *Analysis and Design of Integrated Circuits*," 3rd Ed., Wiley, 1993

2) Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.