EE-612: Lecture 23: RF CMOS

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Fall 2008

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why analog /RF why CMOS?

many applications involve analog / rf signals:

1) many natural signals are analog (sensors)
2) disk drive electronics
3) wireless receivers
4) optical receivers
5) microprocessors / memories

CMOS:

1) many systems are both analog and digital
2) CMOS is the dominate technology for digital electronics
3) CMOS performance has recently become suitable for analog

CMOS device metrics (digital)

1) on-current: \( I_{ON} \)

2) off-current: \( I_{OFF} \)

3) subthreshold swing: \( S = \frac{\partial (\log_{10} I_D)}{\partial V_{GS}} \bigg|_{V_{DS}} \)

4) device delay: \( \tau = C_G V_{DD} / I_{ON} \)

5) DIBL, etc.
CMOS device metrics (analog)

1) transconductance: \( g_m = \frac{\partial I_D}{\partial V_{GS}} \bigg|_{V_{DS}} \)

2) output resistance: \( r_o = \frac{\partial I_D}{\partial V_{DS}} \bigg|_{V_{GS}} \)

3) \( f_T \) and \( f_{\text{max}} \):
   \( f_T = \frac{1}{2\pi \tau} \)

4) noise, mismatch, linearity, etc.

\[ |I_D| \]

\[ V_{DS} \]
outline

1) Introduction
2) **Small signal model**
3) Transconductance
4) Self-gain
5) Gain bandwidth product
6) Unity power gain
7) Noise, mismatch, linearity…
8) Examples
small signal model

\[ i_D = I_D + i_d \]

\[ i_G = I_G + i_g \]

\[ i_d = g_m v_{gs} \quad g_m = \frac{i_d}{v_{gs}} \approx \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{v_{DS}} \]

(quasi-static assumption)
additional parameters in the s.s. model
small signal model (ii)

\[ r_o = \frac{\partial I_D}{\partial V_{DS}} \bigg|_{V_{DS}} \quad g_{mb} = \frac{\partial I_D}{\partial V_{BS}} \bigg|_{V_{DS}} \]
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transconductance

### MOS (above \( V_T \), saturated)

\[
g_m = \frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}}
\]

\[
I_D = W C_{ox} \nu_{sat} (V_{GS} - V_T)
\]

\[
g_m = W C_{ox} \nu_{sat}
\]

\[
g_m/I_D = 1/(V_{GS} - V_T)
\]

\[
g_m/I_D = 1/(1.1 - 0.17) \approx 1 \text{ V}^{-1}
\]

(65 nm HP)

### Bipolar

\[
g_m = \frac{\partial I_C}{\partial V_{BE}}|_{V_{CE}}
\]

\[
I_C = I_{C0} e^{qV_{BE}/k_BT}
\]

\[
g_m = I_C/(k_BT/q)
\]

\[
g_m/I_C = 1/(k_BT/q)
\]

\[
g_m/I_C = 1/(0.026) \approx 40 \text{ V}^{-1}
\]
MOSFET transconductance

\[ g_m = W C_{ox} \nu_{sat} \]

\( T_{ox} \) scaling, high-k, mobility improvements (e.g. strain) increase \( g_m \).
transconductance (subthreshold)

**MOS (below $V_T$, saturated)**

\[
g_m = \frac{\partial I_D}{\partial V_{GS}} \big|_{V_{DS}}
\]

\[
I_D = I_{OFF} e^{qV_{GS}/mk_B T}
\]

\[
g_m = \frac{I_D}{(mk_B T / q)}
\]

\[
g_m / I_D = 1/(mk_B T / q)
\]

\[
g_m / I_D = 1/1.3(0.026) \approx 30 \text{ V}^{-1}
\]

**bipolar**

\[
g_m = \frac{\partial I_C}{\partial V_{BE}} \big|_{V_{CE}}
\]

\[
I_C = I_{C0} e^{qV_{BE}/k_B T}
\]

\[
g_m = \frac{I_C}{(k_B T / q)}
\]

\[
g_m / I_C = 1/(k_B T / q)
\]

\[
g_m / I_C = 1/(0.026) \approx 40 \text{ V}^{-1}
\]
\( \frac{g_m}{I_D} \) figure of merit

\[
\frac{g_m}{I_D} = \frac{1}{(m k_B T/q)}
\]

BJT

MOSFET

\[
g_m/I_D = 1/(V_{GS} - V_T)
\]

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3) Transconductance
4) Self-gain
5) Gain bandwidth product
6) Maximum power gain
7) Noise, mismatch, linearity
8) Examples
small signal gain

\[ i_d = g_m v_{in} \]

\[ V_{DD} \]

\[ R_D \]

\[ v_{out} = -g_m v_{in} R_D \]

\[ v_{in} \]

\[ v_{out} \]

\[ \frac{v_{out}}{v_{in}} = A_V = -g_m R_D \]
effect of output resistance

\[ r_o = \frac{\partial I_D}{\partial V_{DS}} \bigg|_{V_{DS}} \]

\[ A_v = -g_m R_D \parallel r_o \]
self-gain

\[ V_{DD} \]

high impedance current source

\[ v_{in} \]

\[ r_o \]

\[ v_{out} \]

\[ A_v(\text{max}) = -g_m r_o \]
self-gain for 65 nm digital CMOS

\[
g_m \approx \frac{0.2 \text{ mA/\text{	extmu}m}}{0.2 \text{ V}} = 1 \text{ mS/\text{	extmu}m}
\]

\[
r_o \approx \frac{1.2 \text{ V}}{0.18 \text{ mA/\text{	extmu}m}} \approx 7 \text{ K\Omega/\text{	extmu}m}
\]

\[
|A_v(\text{max})| = g_m r_o \approx 7
\]

C.-H. Jan. et al., 2005 IEDM
Analog designers are frequently forced to use non-minimum length (NML) devices.
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6) Unity power gain
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short-current current gain

\[ i_{\text{out}} \approx g_m v_{gs} \]

\[ v_{gs} = i_{\text{in}} \frac{1}{j\omega(C_{gs} + C_{gd})} \]

(should include \( C_{gb} \) too)

\[ i_{\text{out}} \approx \frac{g_m}{j\omega C_{\text{TOT}}} i_{\text{in}} \]
gain-bandwidth product

\[
i_{\text{out}} \approx \frac{g_m}{j\omega C_{\text{TOT}}} i_{\text{in}}
\]

\[
|\beta(\omega)| \approx \frac{g_m}{\omega C_{\text{TOT}}}
\]

\[
|\beta(\omega_T)| = 1 = \frac{g_m}{\omega_T C_{\text{TOT}}}
\]

20 log\text{_{10}}|\beta(\omega)| = C - 20 \log\text{_{10}} \omega

gain falls at 20 dB per decade

\[
f_T = \frac{g_m}{2\pi C_{\text{TOT}}}
\]
gain-bandwidth product (ii)

\[ \omega_T = \frac{g_m}{C_{TOT}} \]

\[ g_m \approx W C_{ox} \nu_{SAT} \]

\[ C_{TOT} \approx W L C_{ox} \]

\[ \omega_T \approx \frac{\nu_{SAT}}{L} = \frac{1}{t_t} \]

\( \omega_T (f_T) \) is independent of \( W \) and increases as channel length, \( L \), decreases
\[ f_T = \frac{g_m}{2\pi C_{TOT}} \sim \frac{1}{2\pi t_t} \]

**f_T vs. scaling**
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6) **Unity power gain**
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Another figure of merit is $f_{\text{MAX}}$, the maximum frequency of oscillation or the unity power gain.

Channel length scaling increases $r_g$ and lowers $r_o$.
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\[ \text{noise} \]

\[ \bar{i}_n^2 = S_i(f) \Delta f \]
thermal noise

Johnson noise

\[ \overline{V_n^2} = S_f(f) \Delta f = 4k_BTR\Delta f \]

“white noise”
1/f “flicker” noise

polysilicon

SiO₂

dangling bonds “traps”

$S_f(f)$

corner frequency

$1/f$

thermal

$f_c$

$f_c \approx 100 \text{ kHz}$
mismatch

analog circuits make use of matched transistors

**sources of mismatch:**

- variations in geometry
- $\Delta V_T$, $\Delta T_{ox}$, ...
- thermal effects, etc.

$$\Delta A = \frac{K}{\sqrt{WL}}$$

**dealing with mismatch:**

- circuit design
- careful layout
The linearity of a device can be quantified by the parameter $D$ defined as:

$$D = \frac{\Delta v_{out\ max}}{v_{out\ max}}$$

This parameter represents the percentage deviation from linearity. In the context of the diagram, $D$ can be visualized as the ratio of the maximum output deviation $\Delta v_{out\ max}$ to the maximum output voltage $v_{out\ max}$.

In the circuit diagram, $V_{DD}$ is the supply voltage, $R_D$ is the resistance, $v_{in}$ is the input voltage, and $e^{j\omega t}$ represents a sinusoidal input. The output voltage $v_{out}$ is shown as a function of $v_{in}$, with $v_{out\ max}$ and $\Delta v_{out\ max}$ indicating the maximum output voltage and the maximum deviation from linearity, respectively.
harmonic distortion

$$A_1 e^{j\omega t} + A_2 e^{j2\omega t} + A_3 e^{j3\omega t} + ...$$

$$i_d = \frac{\partial I_D}{\partial V_{gs}} v_{gs} + \frac{1}{2!} \frac{\partial^2 I_D}{\partial V_{gs}^2} v_{gs}^2 + \frac{1}{3!} \frac{\partial^3 I_D}{\partial V_{gs}^3} v_{gs}^3 + ...$$

$$i_d = g_{m1} v_{gs} + g_{m2} v_{gs}^2 + g_{m2} v_{gs}^3 + ...$$

$$VIP_2 \quad VIP_3$$

extrapolated gate voltage amplitude at which the amplitude of the harmonic = amplitude of fundamental
distortion and the devices

\[ A_1 e^{j\omega t} + A_2 e^{j2\omega t} + A_3 e^{j3\omega t} + \ldots \]

\[ i_d = \frac{\partial I_D}{\partial V_{gs}} v_{gs} + \frac{1}{2!} \frac{\partial^2 I_D}{\partial V_{gs}^2} v_{gs}^2 + \frac{1}{3!} \frac{\partial^3 I_D}{\partial V_{gs}^3} v_{gs}^3 + \ldots \]

\[ I_D \sim (V_{GS} - V_T)^\alpha \quad \text{(above threshold)} \]

DIBL

\[ I_D \sim e^{qV_{GS}/k_BT} \quad \text{(below threshold)} \]
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8) Recent examples
“Record RF Performance of 45-nm SOI CMOS Technology,”
by Sungjae Lee, et al., IBM.

45 nm SOI technology
1.16 nm gate oxide
strained Si technology
Sungjae Lee, et al. IEDM 2007

\[ f_T \approx \frac{1}{2\pi t_t} \]

\[ t_{tN} < 0.33 \text{ ps} \quad \langle \nu \rangle_N > 8.8 \times 10^6 \text{ cm/s} \]

\[ t_{tP} < 0.46 \text{ ps} \quad \langle \nu \rangle_P > 6.7 \text{ cm/s} \]
Sungjae Lee, et al. IEDM 2007

\[ f_T = \frac{1}{2\pi t_i} \]

\[ t_i = \frac{L}{\langle \nu \rangle} \]

\[ L = 10 \text{ nm}, \langle \nu \rangle = 10^7 \text{ cm/s} \]
\[ \rightarrow t_i = 0.1 \text{ ps}, f_T = 1.6 \text{ THz} \]

\[ f_T = \frac{g_m}{2\pi C_{TOT}} \]
Sungjae Lee, et al. IEDM 2007

\[ f_T = \frac{g_m}{2\pi C_{TOT}} \]

Fig. 4. Measured \( f_T \) and \( g_m \) vs. \( V_{GS} \) (at \( V_{DS} = 1.0 \text{ V} \)) for 45-nm SOI NFET (\( L_{poly} = 29 \text{ nm} \)) with (A) relaxed poly pitch and (B) minimum poly pitch, obtained by extrapolating the value of \( |H_{21}| \) at 10 GHz using -10 dB/dec slope after de-embedding.

Fig. 5. Measured \( f_T \) and \( g_m \) vs. \( V_{GS} \) (at \( V_{DS} = -1.0 \text{ V} \)) for 45-nm SOI PFET (\( L_{poly} = 31 \text{ nm} \)) with (A) relaxed poly pitch and (B) minimum poly pitch, obtained by extrapolating the value of \( |H_{21}| \) at 10 GHz using -10 dB/dec slope after de-embedding.
Sungjae Lee, et al. IEDM 2007

\[ |A_V| = g_m r_o \]

Fig. 11. Measured self-gain (= \( g_m/g_{ds} \)) vs. \( V_{GS} \) (at \( V_{DS} = 1.0 \) V with body contact tied to the source) from S-parameter data at 10 GHz, comparing A: 13 \( \mu \)m (0.65 \( \mu \)m by 20 gate fingers), body-contacted SOI NFET with 46 nm \( L_{poly} \), B: 12 \( \mu \)m (0.6 \( \mu \)m by 20 gate fingers), floating-body SOI NFET with 32 nm \( L_{poly} \).

“A suitable SoC process technology needs to support both digital and analog functions with high density embedded memories.”
“Potential 1/f noise degradation induced by gate oxide nitridation and local strain process has been one of the critical concerns in analog applications [8]. Gate oxide with different nitrogen profiles and strain process with different film stacks are studied.”

Fig. 8 (a) Comparison of NMOS 1/f noise for different combinations of gate oxide and strain process.
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references
