Enhanced Pool Boiling Using Carbon Nanotube Arrays

Sebastine Ujereh
Vanderbilt University/Purdue University
West Lafayette, IN 47902

Since the invention of computers, improvements and innovations in computers and computer related technology have been made at exponential rates. The advancement of integrated circuit technology in computers is no exception. Computer chips have steadily continued to decrease in size while power input has correspondingly increased. The increase in power input to the chip and decrease in chip size has resulted in an overall increase in heat flux. This trend calls for improvements in chip-cooling technologies. The potential of direct liquid immersion, pool boiling, as a superior alternative to air cooling and indirect liquid cooling technologies has been observed [1]. Pool boiling remains a very attractive cooling option due the unique attribute of passive fluid circulation. Having no mechanical pumps, pool boiling hardware is less complex, easier to seal, and free of pump-induced fluid pulsation [1]. One of the main obstacles for improvements in chip cooling technology is the limiting factor of critical heat flux (CHF). Large amounts of power cannot be input to the chip without the phenomenon of CHF destroying the chip. The introduction of carbon nanotube (CNT) arrays will increase the temperature at which CHF is reached, thus allowing for more power input. The field of enhanced pool boiling may prove to be an application of CNT's. Given the relatively new discovery of carbon nanotubes, not much progress has been made towards a practical and marketable application of these devices [2]. This experimental study is conducted to explore CNT arrays on a silicon surface and how this will affect pool boiling behavior. The present study involves the collection of pool boiling data on a smooth silicon surface as well as a silicon surface coated with CNT's.

Figure 1 below shows a schematic of the experimental test loop. The power input to the silicon surface test section in the boiling chamber is supplied by the Variac power meter. The temperature within the chamber is collected by a data acquisition system, which sends the information to a PC. Cooling water is supplied to condense to vapor within the boiling chamber.

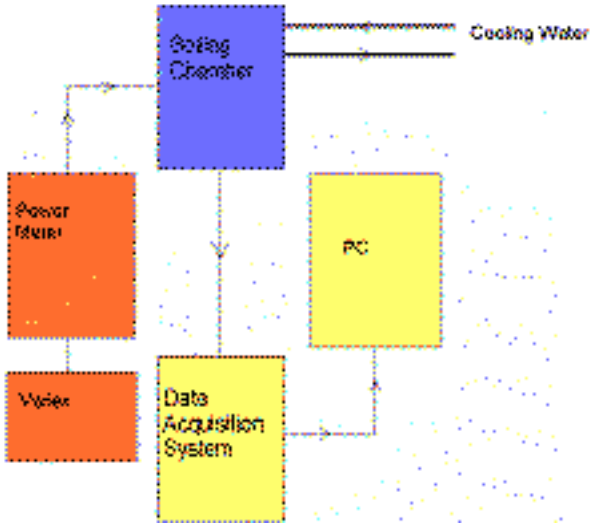

Fig 1. Test Loop

Figure 2 below shows a schematic of the boiling chamber in which the tests were conducted.

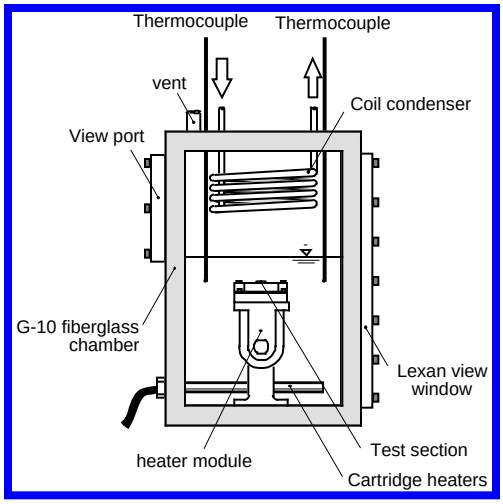

Fig 2. Boiling Chamber

The oxide on a blank two-inch silicon wafer was removed to facilitate metal deposition. After the oxide was removed, the wafer was brought to the NRC thermal evaporator for metal deposition. On the back side of the wafer a layer of chrome was evaporated, followed by a layer of gold. The wafer sample was then diced into _ inch squares using a Tempress 602 dicing saw. The _ inch chip was soldered onto the surface of a copper block of the same size. This test section is shown in Fig. 3. A heater was also soldered onto the bottom of the copper plate.

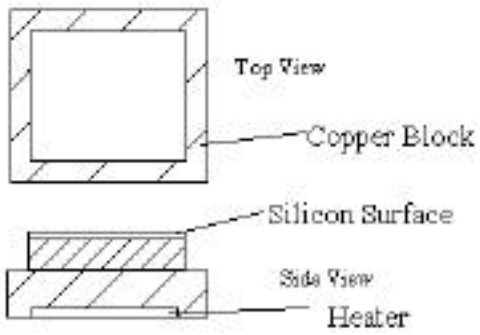

Fig 3 Schematic of copper block with silicon soldered onto surface and heater soldered underneath

The copper plate was fitted with a thermocouple and two copper leads. The copper block then was mounted into a pool-boiling facility. Two thermocouples were hooked up and measured the bulk temperature of the FC-72, while another one measured the temperature of the copper block, and the heater leads were connected to a Variac power input device.

Once the experiment was set up the silicon surface was cleaned with acetone and the dielectric fluorocarbon (FC-72, 3M) was poured into the facility. The FC-72 was brought to its boiling point of approximately 56.6 C while there was a power input of 10 W to the silicon chip in order to remove the acetone from the surface. The power was

reduced to 1 Watt, and the temperature of the FC-72 and the temperature of the silicon chip were monitored and recorded using LabView data acquisition software. The power input, current, and voltage were recorded manually. This process was repeated in 1-watt increments until the CHF point is reached, as indicated by a steady increase in its temperature at a constant input power.

Heat flux results show CHF being reached at a wall temperature of approximately 100 C with a power input of 12W/cm. These results are based on measurements on a completely smooth silicon surface.

Experimental data of silicon surface coated with CNT's are not yet available. It is expected that this surface should significantly enhance the effect of pool boiling. Not only due to the variations to the surface of the chip on the nano-scale, but also given the unique characteristics of carbon nanotubes as excellent thermal conductors. It has been readily observed that carbon nanotubes exhibit superior thermal conductivity. A recent experimental study indicated that the thermal conductivity of a multi-walled nanotube (MWNT) is greater than 3000 W/mK at room temperature [3], which is about eight times higher than that of copper. Such a high thermal conductivity will transfer heat from the silicon surface to the fluid at a much higher rate.

References

1. Mudawar, I et al. "Microelectronic Cooling by Enhanced Pool Boiling of a Dielectric Flourocarbon Liquid." Transactions of the ASME. vol 111 (1989). 752-759.

2. Iijima, Sumio. "Carbon nanotubes: past, present, and future." Physica B. 323 (2002). 1-5.

3. Kim, Phillip et al. "Mesoscopic thermal transport and energy dissipation in carbon nanotubes." Physica B. 323 (2002). 67-70.