Nano-Scale patterning of CdS/CdTe solar cells.

Cesar Lopez
University of Texas at El Paso, El Paso, Tx 79968 USA
Purdue University, West Lafayette, In 47907 USA
NCN/INAC summer internship 2003

Introduction

The research for new sources of energy has increased dramatically during the last few years. The low cost of implementation in solar cells may generate a powerful option to be use in electrical systems [1]. Several attempts have been made to improve efficiency on solar cells. CdS/CdTe has been found to be one of the most promising solar cells developed. Due to a relativity easy manufacturability and a good absorption coefficient, CdS/CdTe cell efficiency improved tremendously during the 1980's attaining 14% efficiency by the beginning of 1990's. However, during the last 10 years little progress has been made to further increase the cells efficiency. Since then, the latest results show very small increases of 2-3% [3,4].

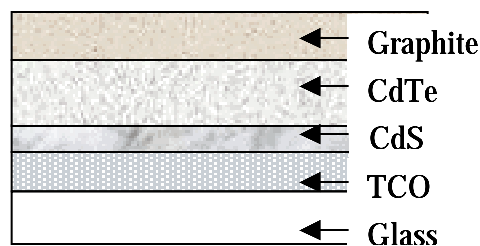

Figure 1. High efficiency CdS/CdTe solar cell structure

CdS/CdTe solar cell layers have typically been grown on TCO/glass as shown in Figure 1. A high efficiency solar cell typically use the chemical bath deposition (CBD) [5] and closed-space sublimation (CSS) [6] methods for deposition of CdS and CdTe layers respectively. The CSS process is one of the most efficient ways to control grain size deposition, which has direct effect on cell performance [6,7]. However, regardless of the average grain size obtained, CSS CdTe deposition results in a randomized polycrystalline layer. We attribute the slow increases in efficiency improvement on the randomness of the polycrystalline layers. Therefore, a single crystal CdTe layer structure may significantly improve interface defects and layer performance that can result in cell enhancement. However, single crystal growth is cost prohibitive. It has been found that

crystal defects and structure mismatches can be significantly decreased by patterning at small scales [8-10]. Therefore, to reduce CdTe grain non-uniformity an array of ordered crystals can be created by various methods. For example, by depositing and patterning a dielectric growth mask prior to depositing CdTe. Nevertheless, there is not much work done on CdTe nanopatterning. For these reasons, the objective of the current research project is to minimize crystal defects by the design and implementation of a nanopatterning procedure.

The general procedure of this project is divided in four basic parts. 1)CdS growth on ITO/glass substrate, 2) SIO2 layer deposition, 3)SiO2 nanopatterning, 4)CdTe layer deposition. The first and last part will be performed at UTEP while SiO2 deposition and patterning at Purdue University. The following paragraphs will focus on part 3, the nanopatterning procedure.

SiO2 nanopatterning

Several steps need to be done to pattern the solar cell as desired. The SiO2 grown layer(Fig. 2a) will be used to patterned into an array of windows. The purpose of this array is to achieve control on grain uniformity and single crystal growth in each window in the CdTe deposition. The first step to pattern the solar cells is to design a mask with various feature sizes in the range of nanometer scale to a few microns. The reason for using different feature size is to characterize the crystal growth and grain deposition at each particular patterning scale for future improvements on mask design.

Next, a photoresist spinner must be use

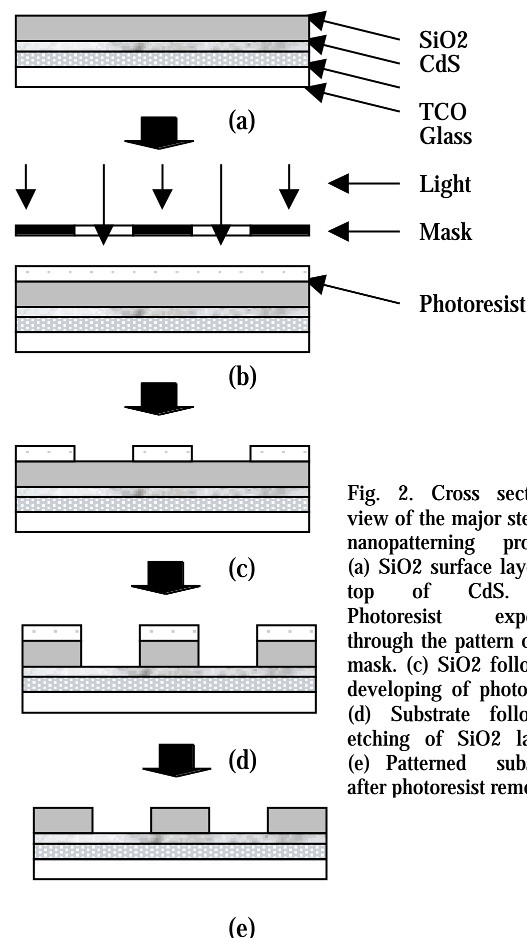

Fig. 2. Cross sectional view of the major steps in nanopatterning process. (a) SiO2 surface layer on top of CdS. (b) Photoresist exposure through the pattern of the mask. (c) SiO2 following developing of photoresist (d) Substrate following etching of SiO2 layers. (e) Patterned substrate after photoresist removal.

to deposit a thin uniform layer of photoresist on the SiO2 layer. An AZ1500 series photoresist will be used. The resist thickness varies from 1.0-2.0um which decreases as the spinning speed is increase. Within this range, the final thickness is inversely proportional to the square root of the spinning speed. Typical speeds ranges are from 3000 to 7000rpm. The next part will include a soft-bake procedure to remove solvents, get better adhesion and to improve photosensitivity. To achieve this task, the solar cell will be placed in an oven for 30min at $90^{\circ}C$. Following soft-bake, the sample is ready to be use in the mask aligner for exposure. A Karl SUSS MJ3BUV mask aligner will be use to expose the photoresist and transfer the shape of the mask designed into the surface of the photoresits layer (Fig. 2b). To obtain the desired openings, a developer will be use from 60 to 120sec and the unwanted photoresist will be removed after rinse with DI water. Once the photoresist was developed as shown in Figure 2c, a hard-baking step is required. The Solar cell will be place in an oven from 20-30min at $120^{\circ}C$ to harden the photoresist and improve adhesion to the SiO2 surface. Then, a wet oxide etch method will be used to etch the SiO2 in the photoresist openings. This process must be very precise to etch just the SiO2 surface (Fig. 2d). Overetching on the SiO2 surface will affect the CdS surface; therefore a new solar cell will have to be constructed. Finally, the last part of the designed procedure is to remove the remaining photoresist from the SiO2 layer and the sample will be ready for CdTe deposition as shown in figure 2e.

Mask Design

A dark field mask layout with a 4000*4000 array of windows was designed using Mentor graphics software. The file was transfer to GDS format and sent it to be generated in an electronmask platemaker. Numerous problems were found to generate the pattern of the mask and after several attempts it was found that it will take several days to generate the arrays need it. The arrays generated a big file very

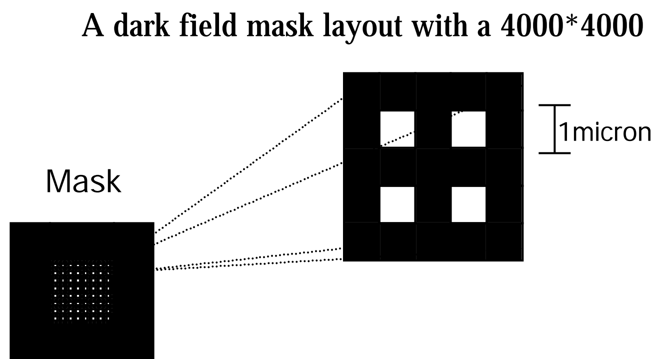

Fig. 3 Representation of mask designed with minimum feature size of 1micorn

complicate to be processed by the platemaker. The mask designed was modified a few times and the array scale adjusted from 1 to 3micron for the minimum feature size(Fig. 3). Since the ideal thickness of the CdTe layer is from 2-3micron the biggest feature size that was appropriate to design was choose to be at no more than 3micron. The mask consisted in 1000*1000windows array in the smallest feature size and 333 for the biggest. It covered a total area of 10000*10000um with 5 different feature sizes. To cover the largest part in a 2 by 1inch sample the pattern was repeated several times to be generated on the mask. Unfortunately, the reticle mask could not be generated on the platemaker even with the new mask designed. Therefore, the mask was sent to a company to be created. The patterning process was impossible to continue without the mask, but several goals were accomplished in order to prepare for the next processing steps when the mask would arrive.

A photoresit spinner was use to deposit the photoresist. Given that the mask was design with a dark field, a positive resist was chosen. An AZ1518 positive photoresist was tested in a few samples with a range of 4000-7000rpm of spinning speed to obtain different thicknesses. Some problems were found after deposition. The photoresist does not attach properly to the CdS surface without previous cleaning procedure. Even tough, the samples were designed and stored in clean environments, photoresist adhesion may be affected by dust or moisture. Also, given that the solar cells developed are rectangular in shape, the circular rotation of the photoresist spinner prevents the deposition of the photoresits in the corners. In addition, the Karl SUSS MJ3BUV mask aligner was tested several times for exposure on silicon wafers.

Conclusion

The nanopatterning procedure was developed according to the most viable and accessible methods of photolitography. However, things are not quite straight forward in practice. The mask has to be adjusted to the minimum feature size of 1-3micron arrays. Even tough the mask patterning was not designed for scales below of a micron, a uniform selective growth is expected on the patterning of the solar cell. Moreover, as soon as the mask is received the procedure will be finished.

REFERENCES

1 K.D. Rogers, J.D. Painter, M.J Healy, D.W Lane, M.E. Ozsan, "The crystal structure of CdS-CdTe thin film heterojunction solar cell," Thin Solid Films **339** (1999) 299-304.
2 D.L. Batzner, M.E. Oszan, D. Bonnet, K. Bucher, "Device analysis methods for physical cell parameters of CdTe/CdS solar cells," Thin Solid Films **361-362** (2000) 288-292.
3 T. Aramoto, S. Kumazawa, H, Higuchi, "Jpn. J. Appl. Phys., Part 1 **36**, 6304-5.
4 J. Brittand and C. Ferekides, "Thin-film CdS/CdTe solar cell with 15.8% efficiency;" Appl. Phys. Lett. **62**, 2851.(1993).
5 H.R. Moutinho, D. Albin, Y. Yan, R.G. Dhere, "Deposition and properties of CBD and CSS CdS thin films for solar cells application," Thin Solid films **436** (2003) 175-180
6 Rohatgi A, Chou HC, Jokerst NM, Thomas EW. "Effects of CdTe growth conditions and techniques on the efficiency limiting defects and mechanisms in CdTe solar cells," American Inst. of conference proceedings AIP. **353**, (1996), 368-75.
7 Visoly-Fisher I, Cohen SR, Cahen D. "Direct evidence for grain boundary depletion in polycrystalline CdTe from nanoscale-resolved measurements," Appl. Phys. Lett. **82,** 4, (2003).556-8.
8 Hersee SD, Zubia D, Xinyu Sun, Bommena R, Fairchild M, Zhang S, "Nanoheteroepitaxy for the Integration of Highly Mismatched Semiconductor Materials," IEEE J. Quant. Elec. **38 (**2002), 1017-28.
9 Linthicum K, Gehrke T, Thomson D, Carlson E, "Pendeoepitaxy of gallium nitride thin films," Appl. Phys. Lett .**75**, 2, (1999) 196-8.
10 E.A Fitzgerald, P.D. Kirchner, R. Proano, G.D. Petit, "Elimination of interface defects in mismatched epilayers by a reduction in growth area," Appl. Phys. Lett **52** (1988) 1496-1498.