nanoHUB.org
Impact on Education

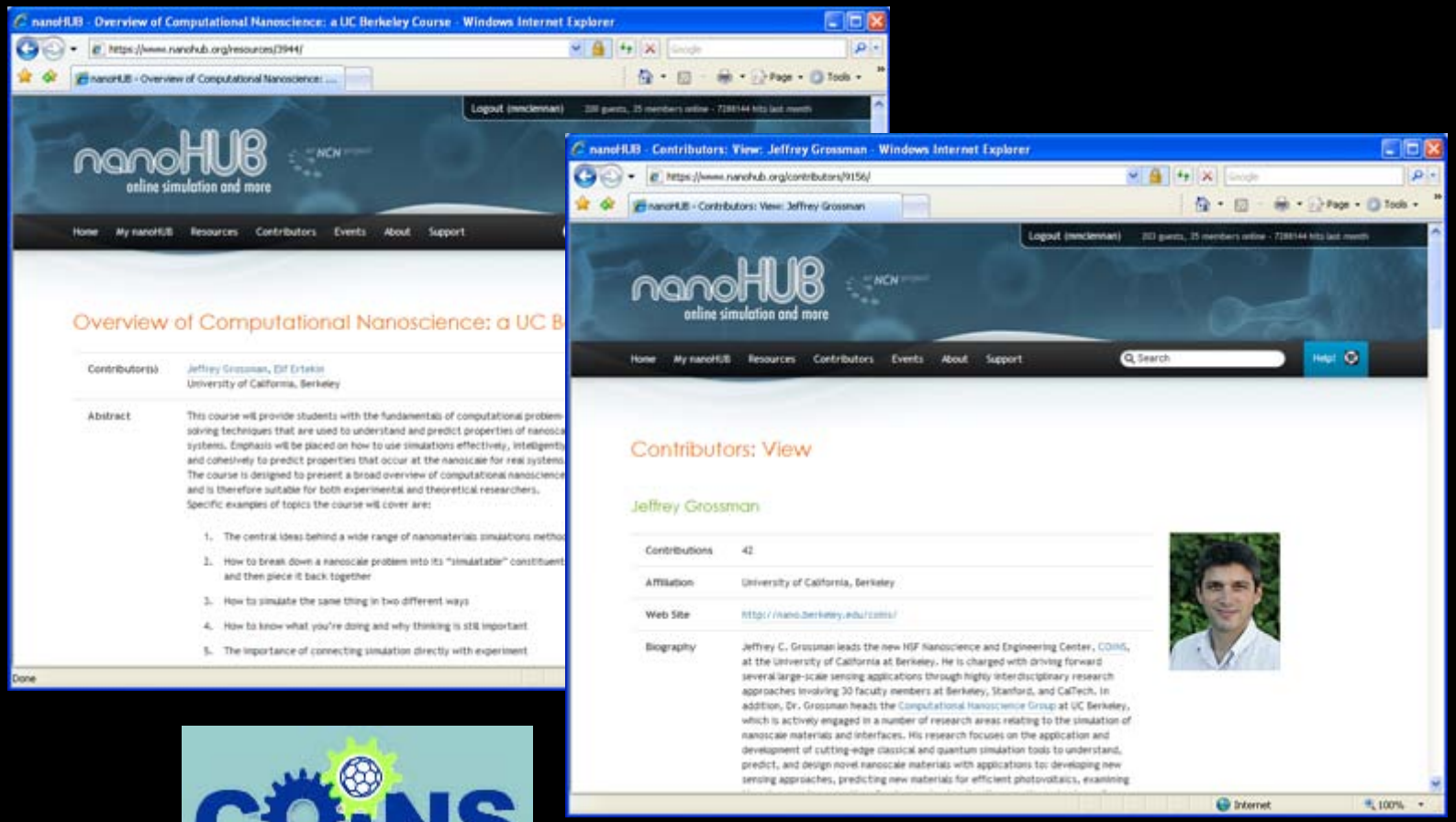
Gerhard Klimeck

nanoHUB.org in

Education

PHYC203/NSEC242:

Computational Nanoscience



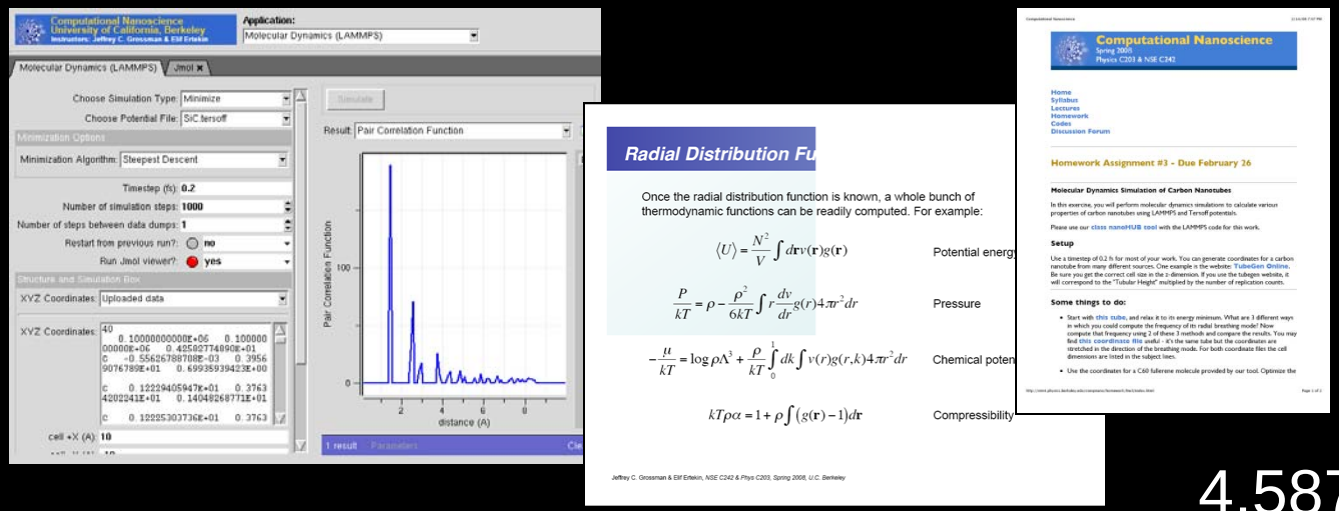
NCN@Berkeley

Powerful Research Codes

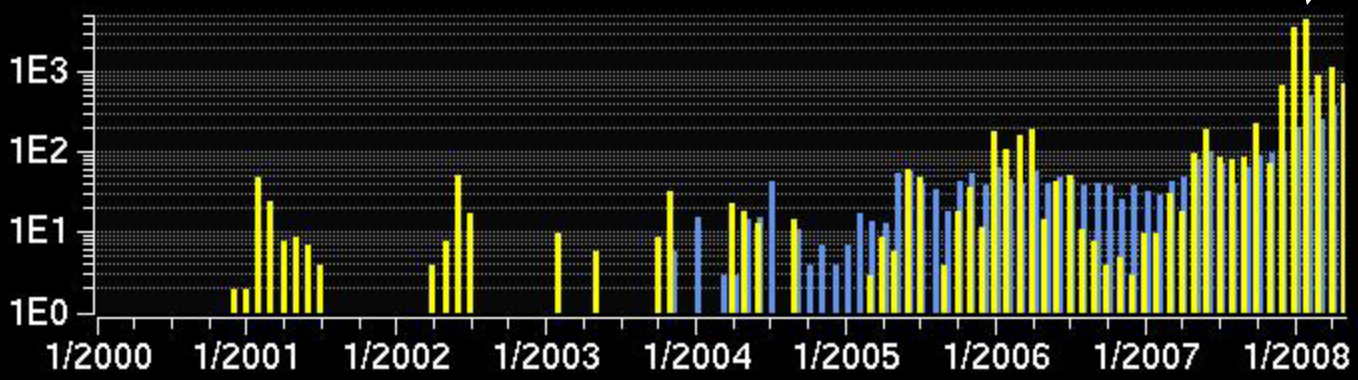
LAMMPS

Sandia National Laboratories

UC Berkeley Usage



4,587 runs!

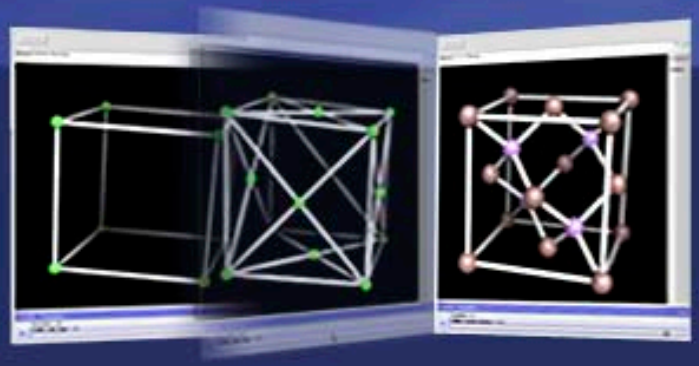


■ Simulation Runs ■ Web Visits

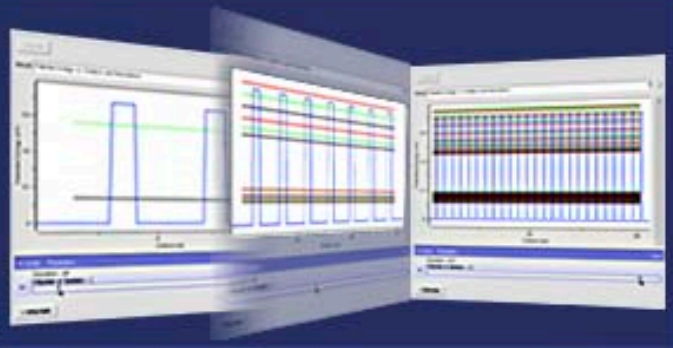
Introduction to semiconductor device education with ABACUS

nanoHUB.org

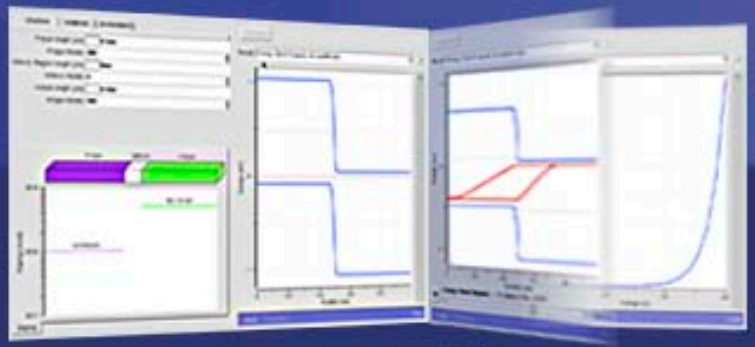
Assembly of Basic Applications for Coordinated Understanding of Semiconductors



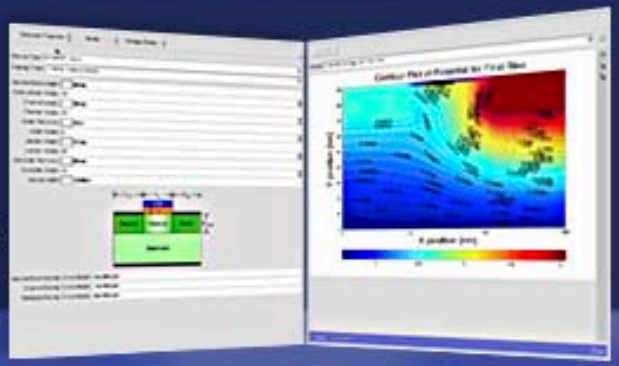
What is the silicon crystal structure



What is band structure



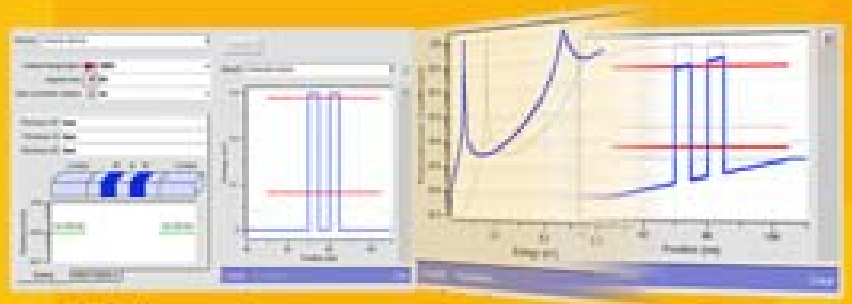
What are highly doped P/N-junctions



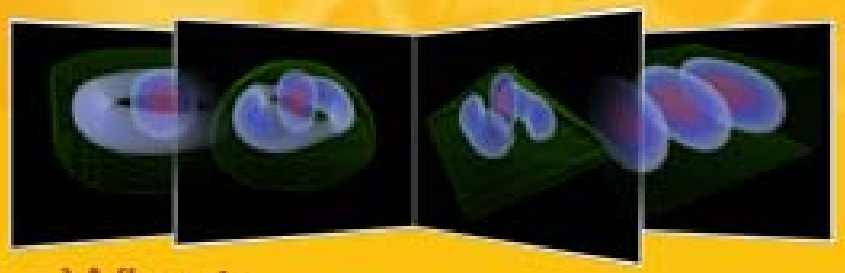
Where is voltage drop in a MOSFET

tutorials all lessons main

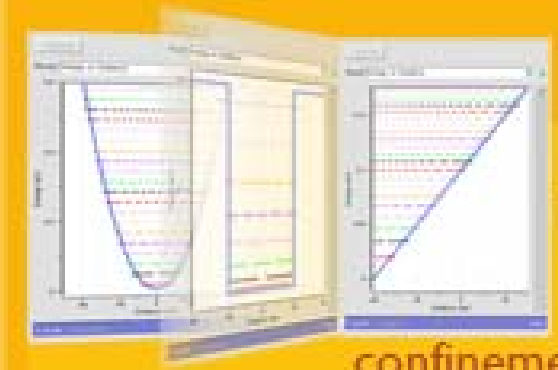
Advancing Quantum Mechanics for Engineers with AQME



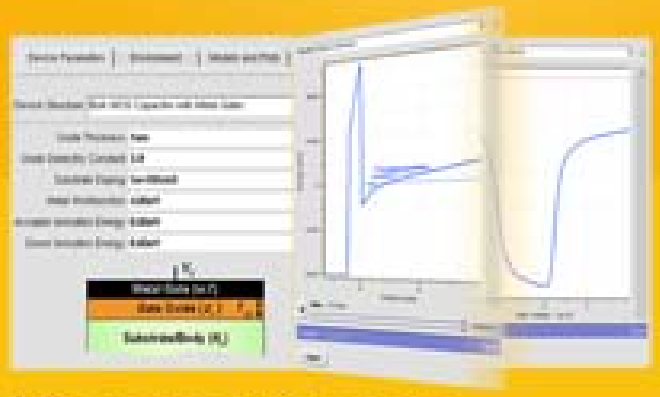
What is resonant tunneling



What is an artificial atom

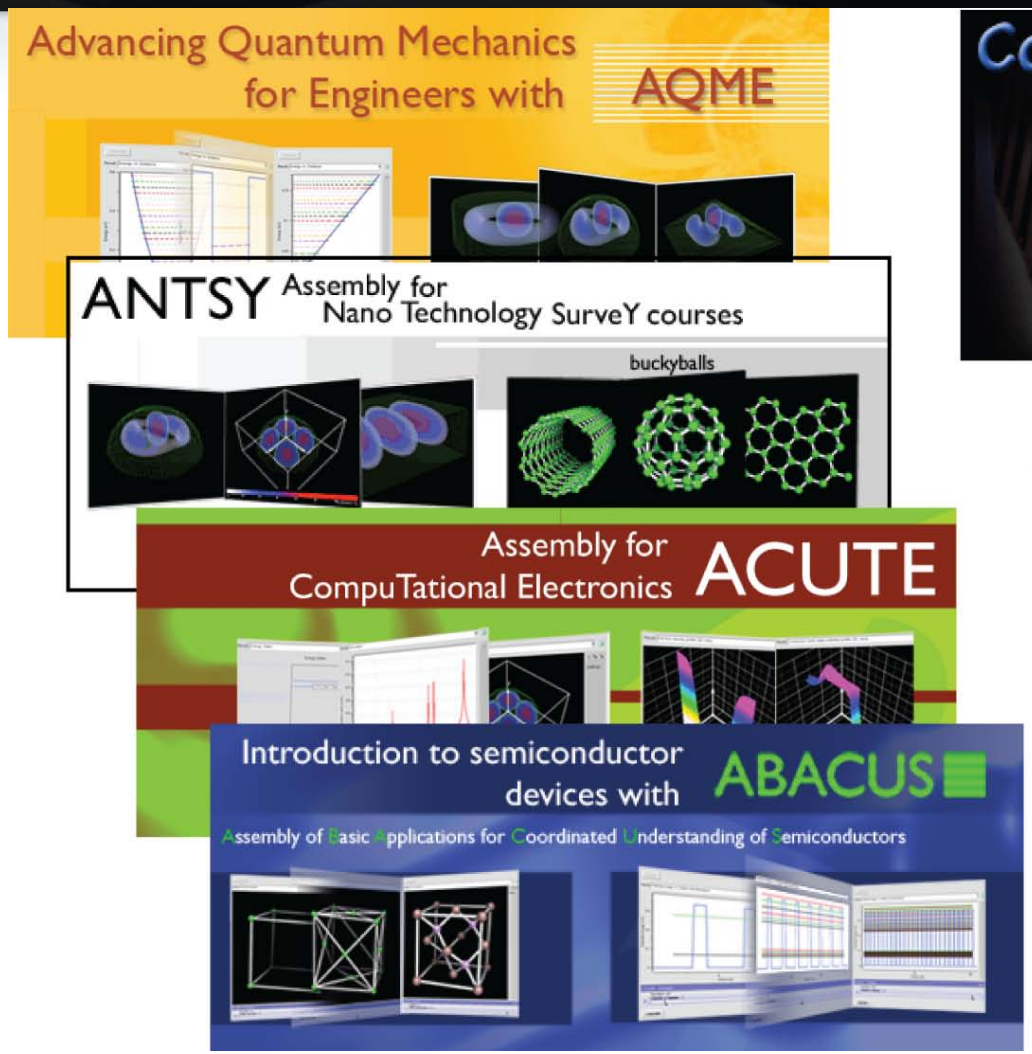


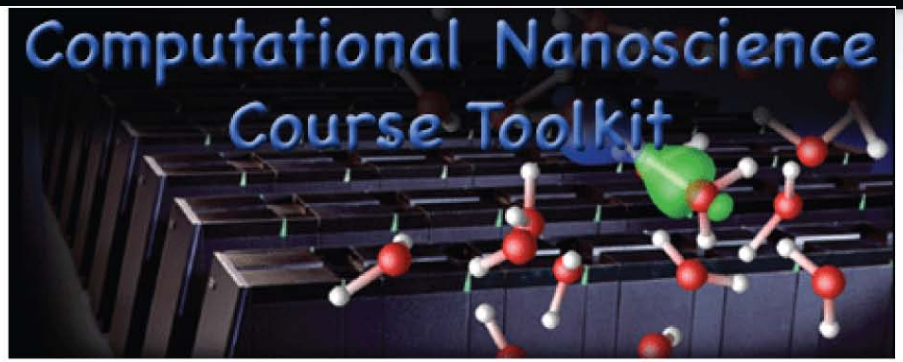
What is the relation between confinement potential and the state spectrum

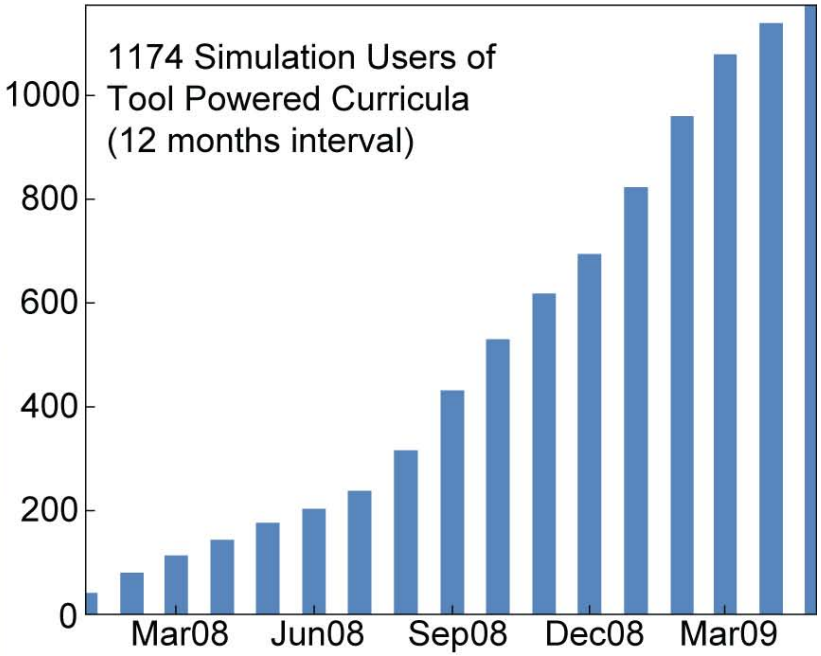


What are MOSFET subbands

Development of Tool-Powered Curricula







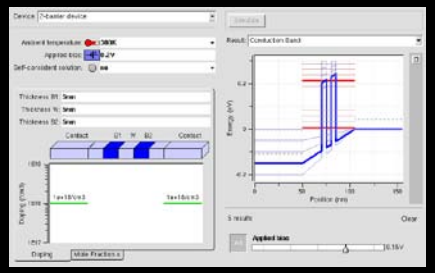
Use in Education

The nanoHUB has proven itself to be an extremely valuable tool for education and research. …We have used the Resonant Tunneling Diode simulator and the MSL simulator on the nanoHUB for homework exercises and mid-term exams. A class survey of the use of the nanoHUB simulation engines had shown that ***the experience is quite positive. The staff at the nanoHUB has been very responsive in supporting our class activities in a professional manner.***

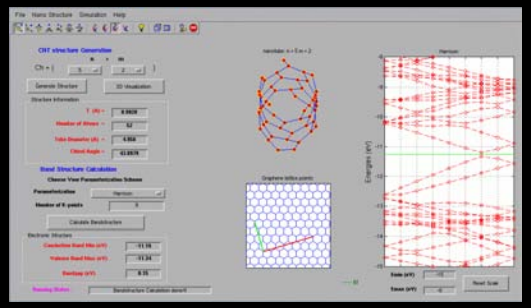
H.-S. Philip Wong

Professor of Electrical Engineering

Stanford University



Resonant Tunneling Diodes



MSL simulator

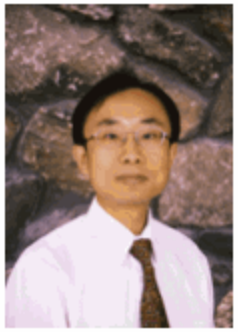
New Contributor

Contributors

H.-S. Philip Wong

Contributions	2
Affiliation	Stanford University
Web Site	http://www.stanford.edu/~hspwong

Biog eceived the B.Sc. (Hons.) in 1982 from the University M.S. in 1983 from the State University of New York at the Ph.D. in 1988 from Lehigh University, all in ring. He joined the IBM T. J. Watson Research Center,



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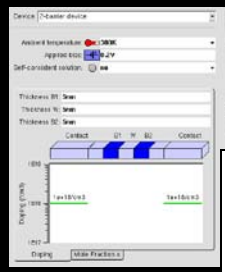
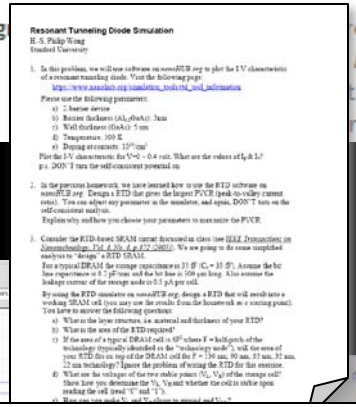


Resonant T
Diodes



Resonant Tunneling Diode Simulation

H.-S. Philip Wong

Stanford University

1. In this problem, we will use software on nanoHUB.org to plot the I-V characteristic of a resonant tunneling diode. Visit the following page:

   http://www.nanohub.org/simulation_tools/rtd_sol_information

   Please use the following parameters:

   a) 2 barrier device
   b) Barrier thickness (Al_xGaAs): 3nm
   c) Well thickness (GaAs): 5 nm
   d) Temperature: 300 K
   e) Doping at contacts: $10^{18}/cm^3$

   Plot the I-V characteristic for V=0 – 0.4 volt. What are the values of I_p & I_v?

   p.s. DON'T turn the self-consistent potential on

2. In the previous homework, we have learned how to use the RTD software on nanoHUB.org. Design a RTD that gives the largest PVCR (peak-to-valley current ratio). You can adjust any parameter in the simulator, and again, DON'T turn on the self-consistent analysis.

   Explain why and how you choose your parameters to maximize the PVCR.

3. Consider the RTD-based SRAM circuit discussed in class (see IEEE Transactions on Nanotechnology, Vol. 4, No. 4, p.472 (2005)). We are going to do some simplified analysis to "design" a RTD SRAM.

   For a typical DRAM the storage capacitance is 31 fF (C_s = 31 fF). Assume the bit line capacitance is 0.2 pF/mm and the bit line is 500 μm long. Also assume the leakage current of the storage node is 0.3 pA per cell.

   By using the RTD simulator on nanoHUB.org, design a RTD that will result into a working SRAM cell (you may use the results from the homework as a starting point). You have to answer the following questions:

   a) What is the layer structure, i.e. material and thickness of your RTD?
   b) What is the area of the RTD required?
   c) If the area of a typical DRAM cell is $8F^2$ where F = half-pitch of the technology (typically identified as the "technology node"), will the area of your RTD fits on top of the DRAM cell for F = 130 nm, 90 nm, 65 nm, 32 nm, 22 nm technology? Ignore the problem of wiring the RTD for this exercise.
   d) What are the voltages of the two stable points (V_1, V_2) of the storage cell? Show how you determine the V_1, V_2 and whether the cell is stable upon reading the cell (read "1" and "1").
   e) How can you make V_1 and V_2 closer to ground and V_{dd}?

Homework for Resonant Tunneling Diodes

06 Jan, 2006 | Teaching Materials | Contributor(s): H.-S. Philip Wong

This homework assignment was created by H.-S. Philip Wong for EE 218 "Introduction to Nanoelectronics and Nanotechnology" (Stanford University). It includes a couple of simple "warm up" exercises and two design problems, intended to teach students the electronic properties of resonant tunneling ...

Deji Akinwande

Stanford University

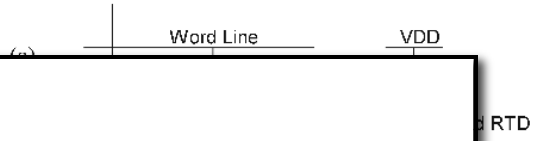
In Philip Wong's Fall 2005 class

776 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 4, APRIL 2007

A Composite Circuit Model for NDR Devices in Random Access Memory Cells

Deji Akinwande, *Member, IEEE*, and H.-S. Philip Wong, *Fellow, IEEE*

***Abstract*—Devices exhibiting negative differential resistance (NDR), such as resonant tunneling diodes and Esaki-type diodes,**



C. Validation of Composite Model

Analytical models are not useful if they are inaccurate. In Fig. 4, a graphical comparison between the three sets of composite models and experimental composite data from the NDR device reported in [6] are shown. As another example,

[1] Online, available http://www.nanohub.org, "Resonant tunneling diodes simulator." The "self-consistent solution" option was turned off. Contact/well material = GaAs, barrier material = AlAs, contact doping = $1 \times 10^{19}/\mathrm{cm}^3$, barrier width = 1 nm, well width = 1.5 nm, RTD area = 918 nm^2.

nanoHUB.org: Impact on Education

- Tools and seminars are being used as instructional materials
- Tool Powered curricula geared towards instruction
- Used in over 290 classes in the past few years
- Used in over 90 institutions for class room instruction
- Instructors are beginning to upload their contributions
- Instruction in fundamentals and subsequent use in research with the same tools!