Nanoelectronics

Diagram:
- Gate metal
- p-type Si
- n-type Silicon
- Gate dielectric
- Source
- Drain
Nanoelectronics

Continued downscaling of microelectronics,
Or chemistry synthesis,
Or some combination of both?

Gerhard Klimeck and Mark Lundstrom Network for Computational Nanotechnology
Nano Challenges

• Difficult to measure, design, make and use on nanoscale
  – Moore’s first law:
    • The amount of space required to install a transistor on a chip shrinks by roughly half every 18 months
  – Moore’s second law:
    • The cost of building a chip manufacturing plant
Substrate Materials

Silicon
Silicon Nitride
Silicon Carbide
Galium Arsenide
Others?

<table>
<thead>
<tr>
<th>Table 4.2</th>
<th>Performance Comparison of Substrate Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>Cost</td>
</tr>
<tr>
<td>Ceramic</td>
<td>Medium</td>
</tr>
<tr>
<td>Plastic</td>
<td>Low</td>
</tr>
<tr>
<td>Silicon</td>
<td>High</td>
</tr>
<tr>
<td>Glass</td>
<td>Low</td>
</tr>
</tbody>
</table>

Fundamentals of Microfabrication, Marc Madou, 2nd edition
Lithography (Patterning the substrate)

**Photolithography** – most commonly used, transfers the pattern of a **mask** onto a substrate using **photoresist** (negative and positive) and **UV light**.
Next Generation Lithography's

1.) Extreme Ultraviolet Lithography – 10 -14nm wavelength
2.) X-Ray Lithography
3.) Charged Particle Beam Lithography
   - Electron Beam
   - Ion Beam
4.) Scanning Probe Lithography
   - dip pen
   - tip/sample (with voltage or force)
5.) Soft Lithography Techniques
6.) Self-Assembled Lithography
7.) 3-Dimensional photolithography

www.azonano.com/.../image001.gif
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