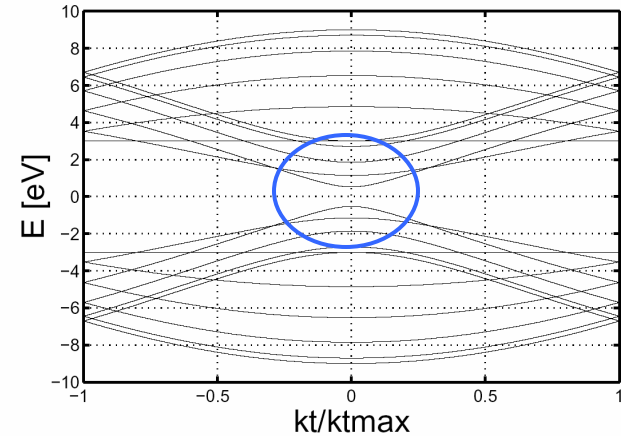
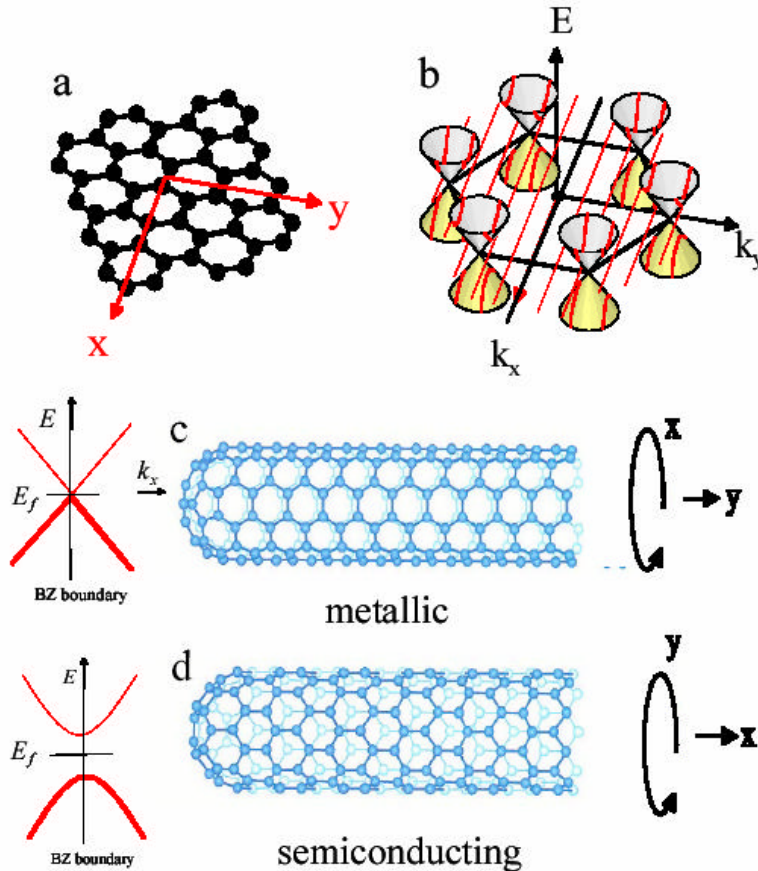


Optimization of Transistor Design for Carbon Nanotubes

Jing Guo

Department of Electrical and Computer Engineering
University of Florida, Gainesville, FL, USA

1. Introduction
2. Simulation Approach
3. Device Physics & Optimization
4. Summary

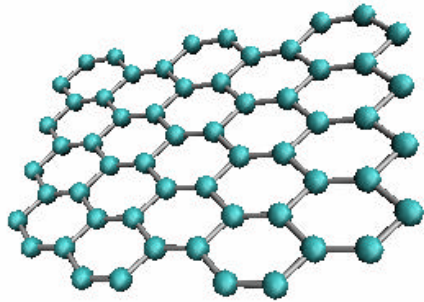


$$E(k) = \pm \left(\frac{E_G}{2} \right) \sqrt{1 + (3kd/2)^2}$$

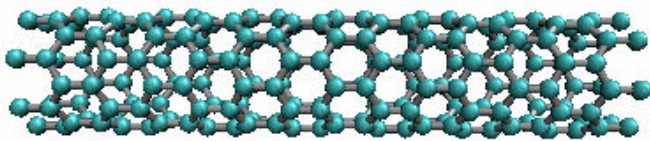
$$E_G \approx 0.8eV/d(\text{nm})$$

McEuen et al., *IEEE Trans. Nanotech.*, **1**, 78, 2002.

(see also: R. Saito, G. Dresselhaus, and M.S. Dresselhaus, *Physical Properties of Carbon Nanotubes*, Imperial College Press, London, 1998.)



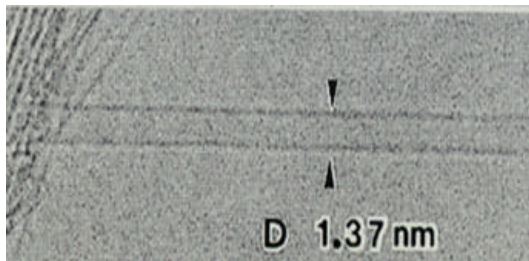
graphene



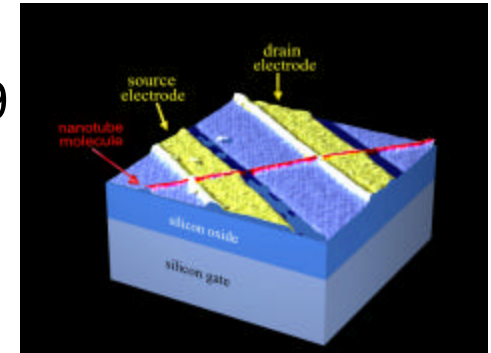
CNT

- **near ballistic transport**
- **no dangling bonds**
- **symmetric cond./val. bands**
- **resistant to electromigration**
- **direct bandgap**
- **small size**

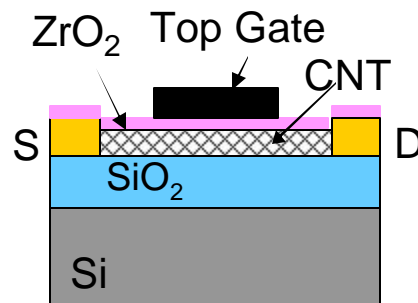
SWNT discovery:
Iijima, 1993



CNTFETs:
Delft, 1998
IBM, 1998
Stanford, 1999



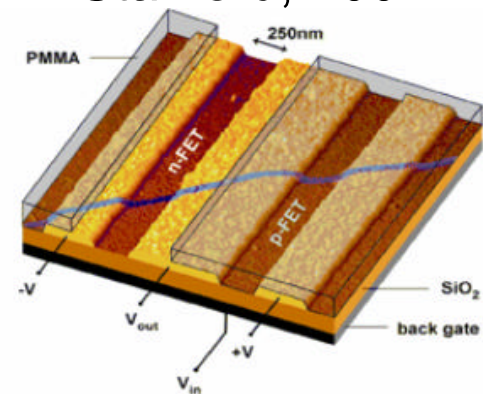
High- κ gate dielectrics
ohmic contacts:
Stanford, 2002



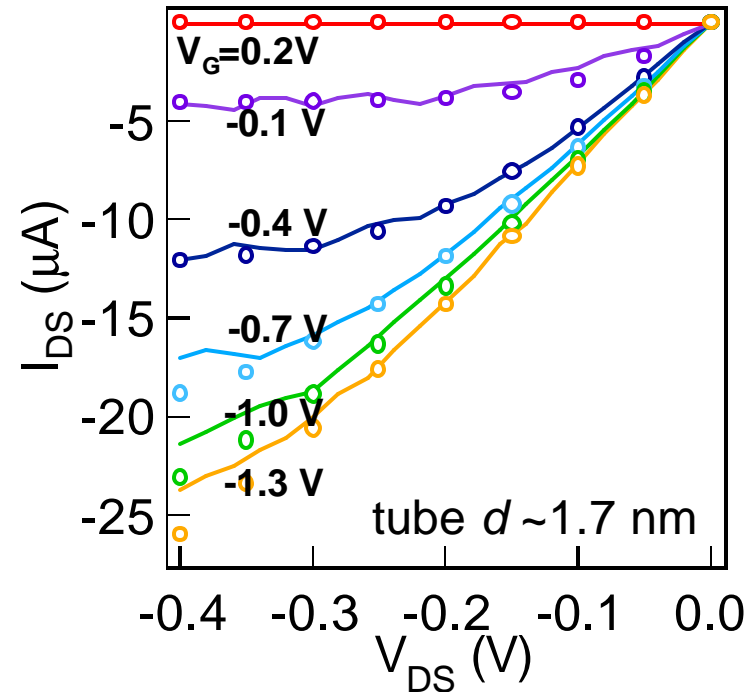
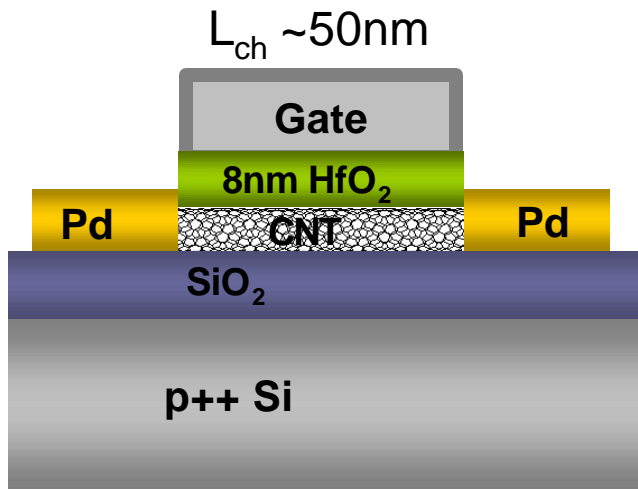
opto-electronics:
IBM, 2003

bio-sensing:
Stanford, 2003
Cornell, 2003

CMOS circuits:
Delft, 2001
IBM, 2001
Stanford, 2002



nanotube diameter ~ 1.7 nm



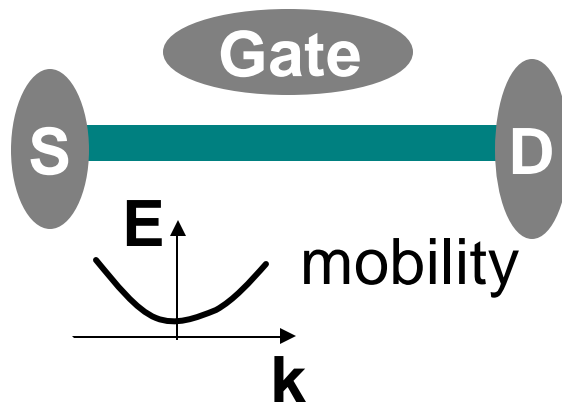
$$G_D \approx G_B$$

$$I_{ON} \approx 3,000\text{mA} / \text{mm} \quad (W = 2d)$$

Javey, Guo, Farmer, Wang, Yenilmez, Gordon, Lundstrom, and Dai, Nano Lett., 2004

1. Introduction
2. Simulation Approach
3. Device Physics & Optimization
4. Summary

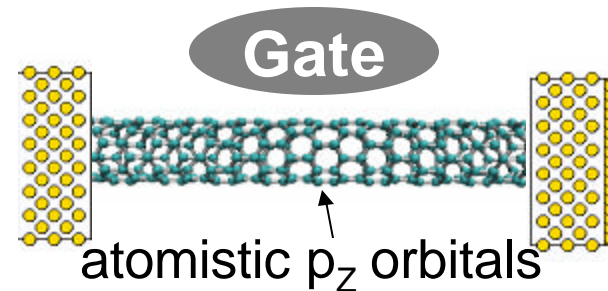
Top-down view



Semiclassical approach

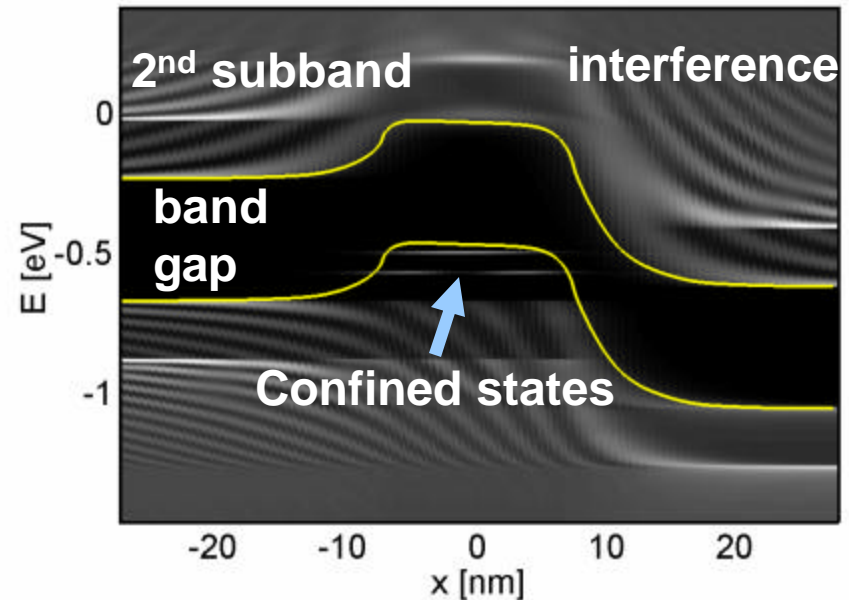
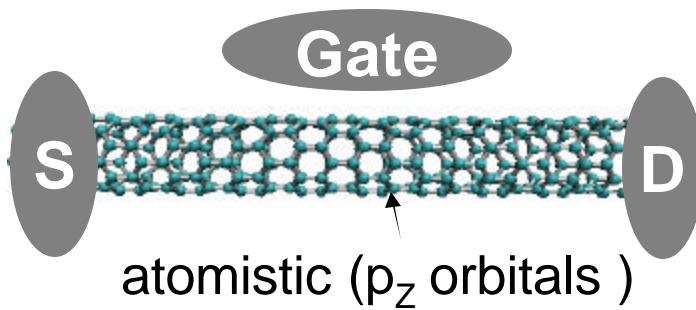
applicable only when quantum effects not important

Bottom-up view



Quantum approach

- tunneling at M/CNT contacts
- tunneling and interference in the CNT



- 1) atomistic treatment of CNT channel
- 2) coaxial gate (2D Poisson) / planar gate (3D Poisson)
- 3) ballistic or with scattering
- 4) phenomenological contacts;

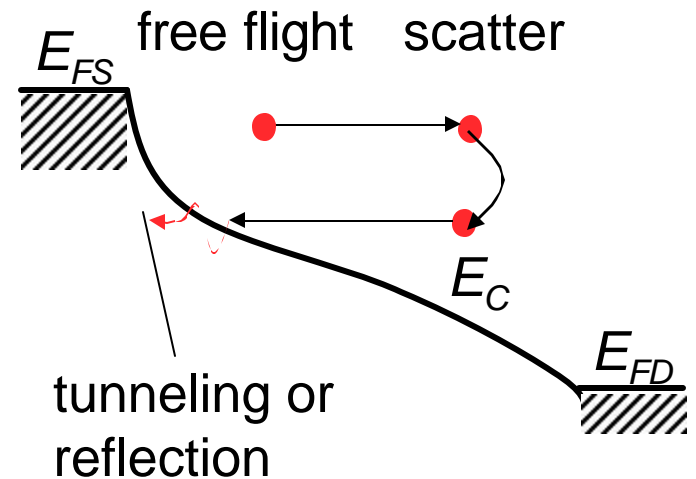
Guo, Datta, Lundstrom, and Anantram, IJMCE, **2**, 257, 2004

Scattering in CNTs

- low-field mfp $\sim 1 \mu\text{m}$
- low-field $m \sim 100,000 \text{ cm}^2/\text{V}\cdot\text{s}$
(Dunkop et al., *Nano Lett.*, **4**, 35, 2004)
- high-field mfp $\sim 10\text{nm}$
(Javey, et al., Park, et al.)

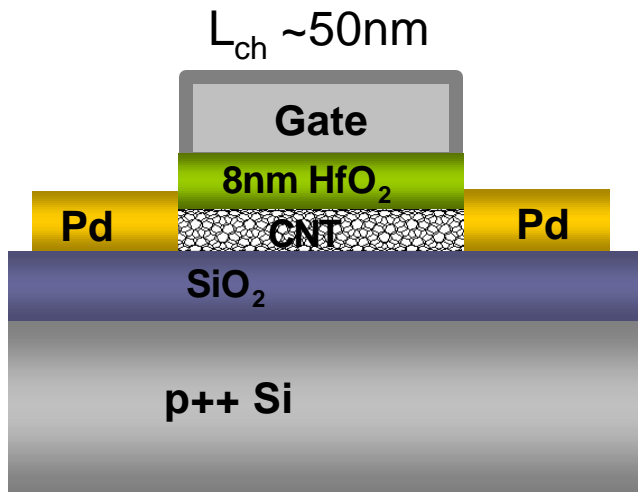
CNTFET Monte Carlo

- Analytical CNT band structure
- Acoustic and optical phonon scattering
- Pauli exclusion
- WKB tunneling
- Self-consistent electrostatics

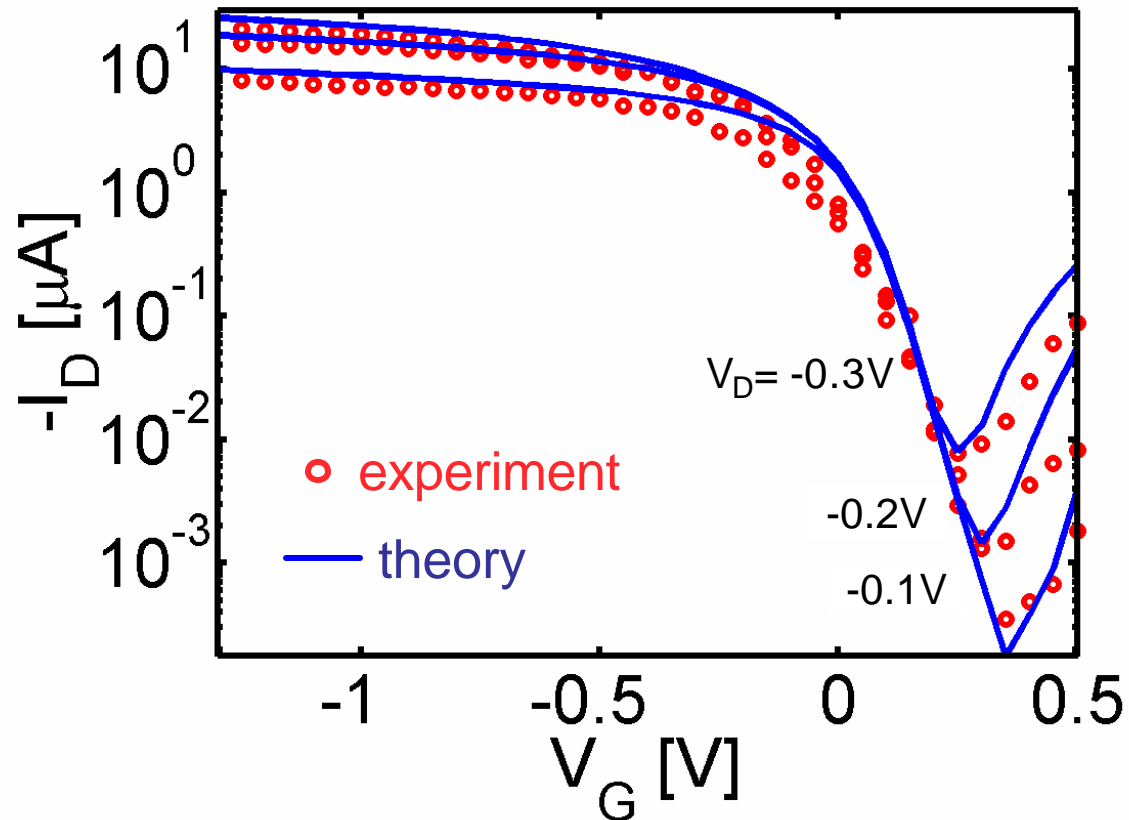


1. Introduction
2. Simulation Approach
3. Device Physics & Optimization
4. Summary

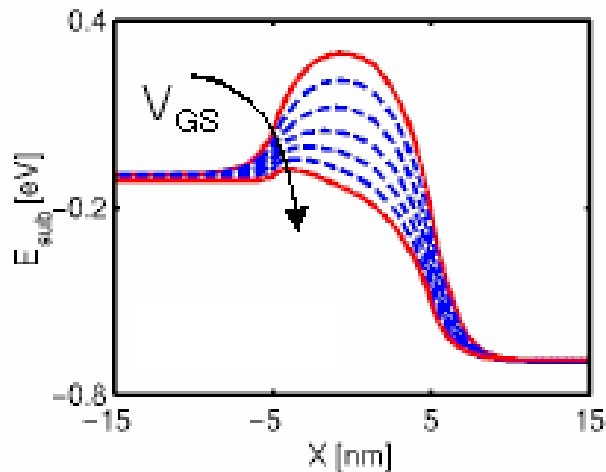
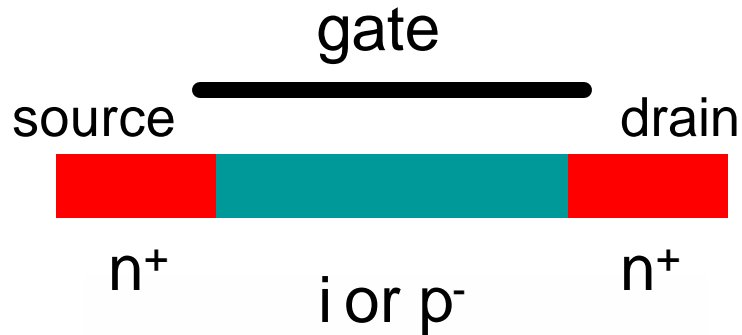
nanotube diameter ~ 1.7 nm



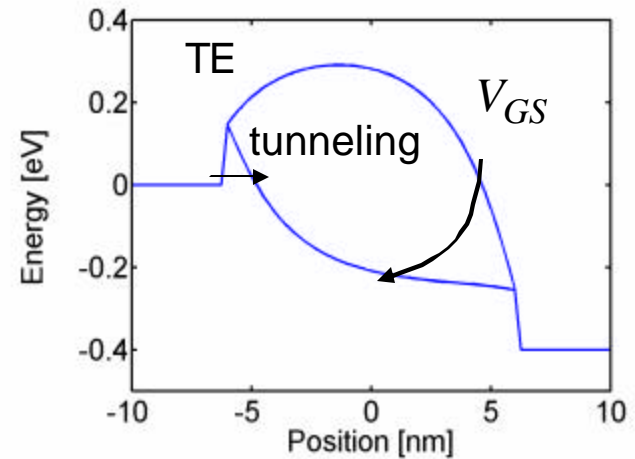
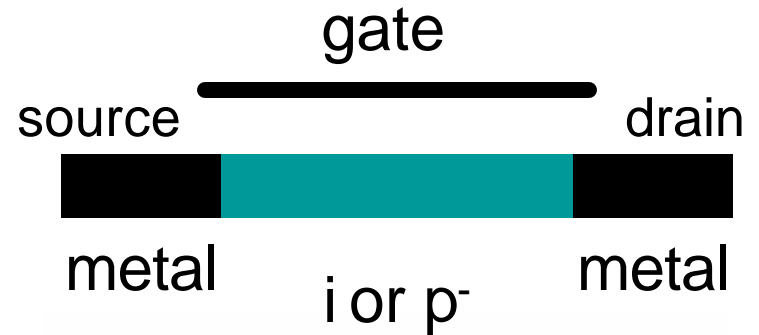
- 1) Does theory describe experiment?
- 2) How to understand I-V?
- 3) How to optimize transistor design ?
- 4) How to compare to Si MOSFETs?
- 5) What's the potential for RF?



SB height: $\phi_{Bp} = 0$, $d_{CNT} \sim 1.7nm$ $R_S = R_D \sim 1.7K\Omega$

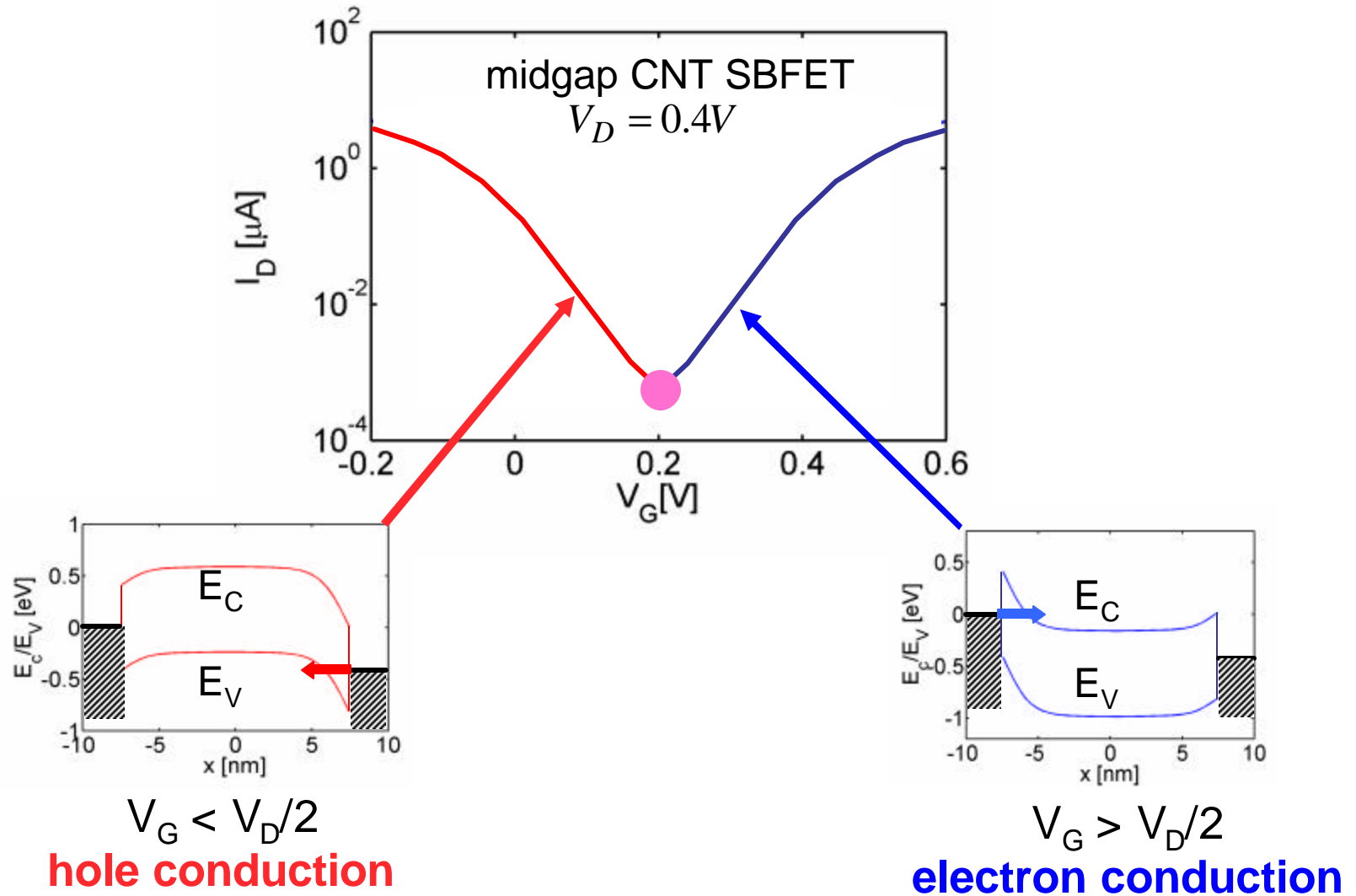


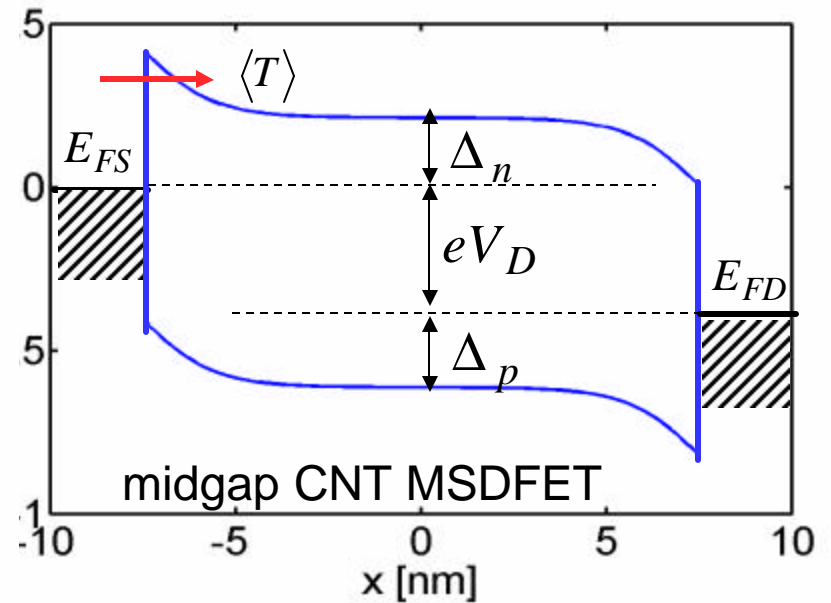
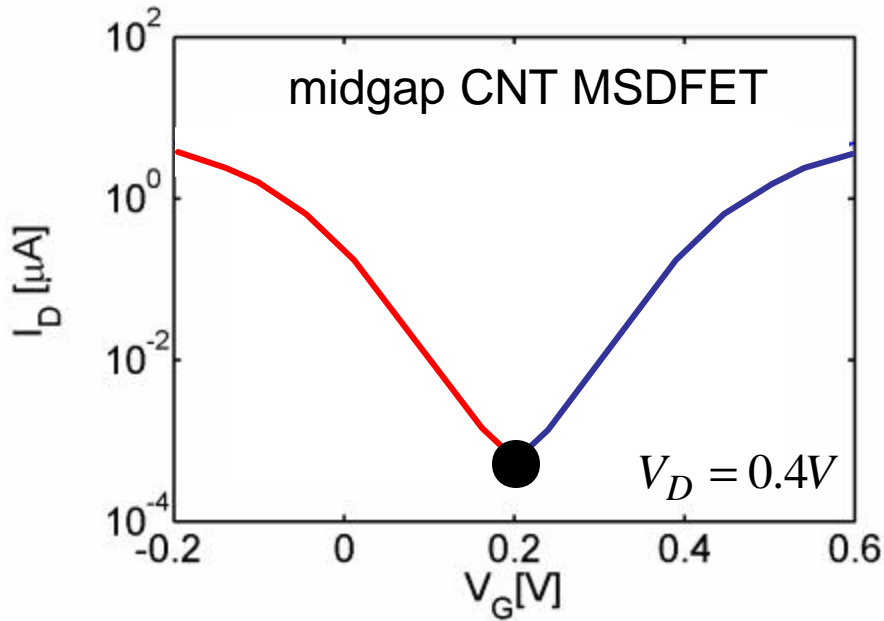
MOSFET



SBFET

Carbon nanotubes as Schottky barrier transistors
 Heinze et al, *PRL*, **89**, 106801, 2002

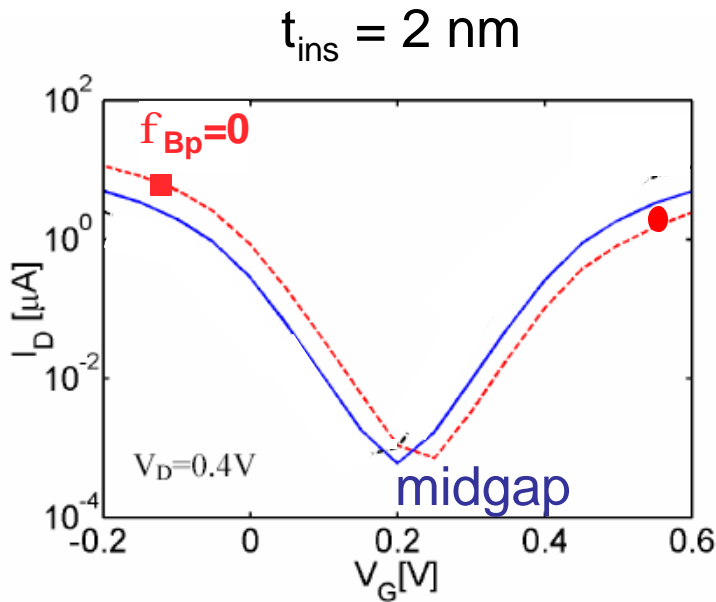




$$V_{GS} = V_{DG} = V_D/2$$

$$\Delta_n = \Delta_p \approx \frac{E_g - eV_D}{2}$$

$$I_{\min} \sim \langle T \rangle \frac{8ek_B T}{h} \exp\left(-\frac{E_g - eV_D}{2k_B T}\right)$$

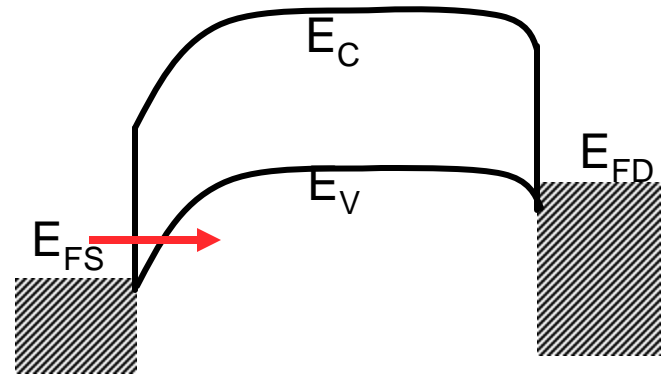


Radosavljevic et al,
APL **83**, 2435, 2003

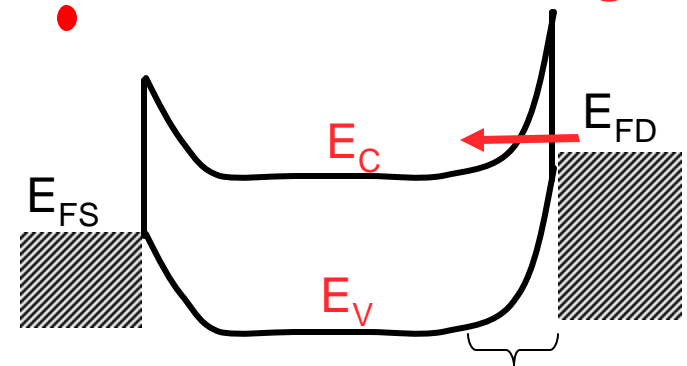
Guo, Datta and Lundstrom,
IEEE Trans. ED, **51**, 172, 2004

$f_{Bp} = 0$

hole conduction at low V_G

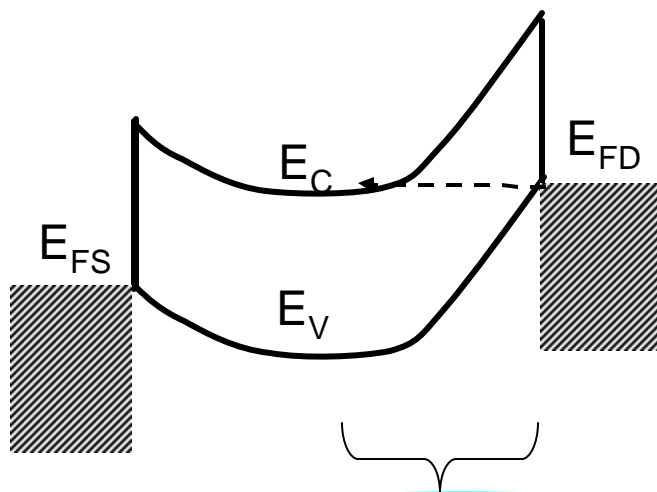


electron conduction at high V_G



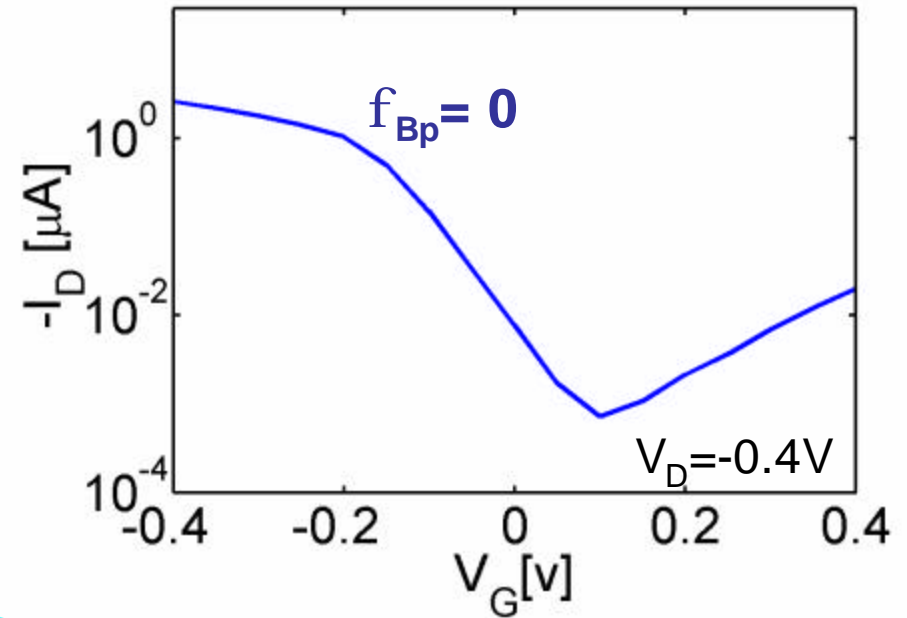
barrier thickness set by t_{ins}
(geometric screening)

opaque barrier for electron tunneling

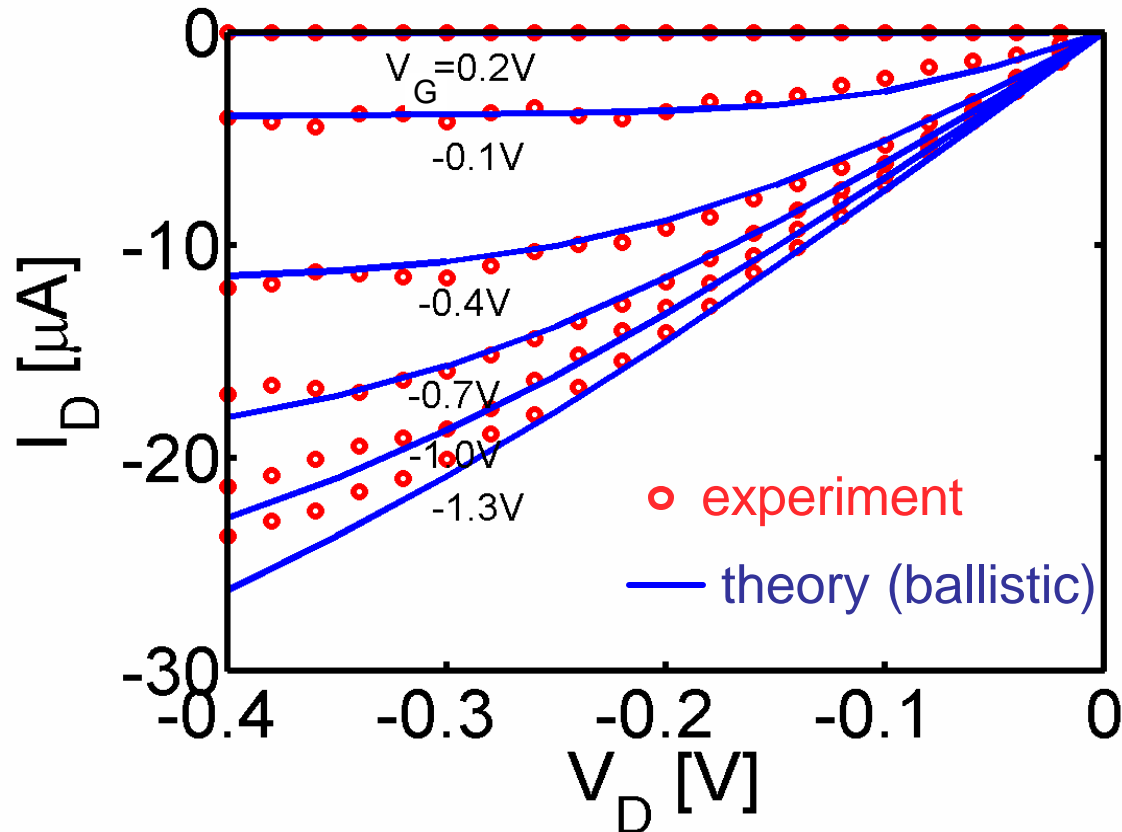


barrier thickness set by t_{ins}
(geometric screening)

$t_{ins} = 40 \text{ nm}$

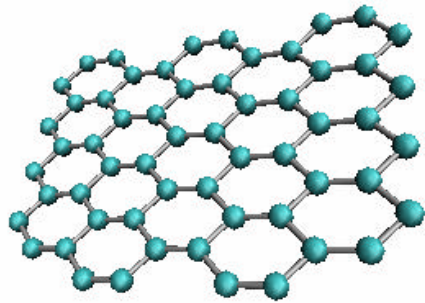


Guo, Datta and Lundstrom, *IEEE Trans. ED*, **51**, 172, 2004

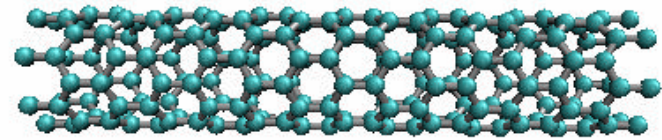


SB height: $\phi_{\text{Bp}}=0$, $d_{\text{CNT}} \sim 1.7\text{nm}$, $R_S=R_D \sim 1.7\text{K}\Omega$

⇒ Deliver near-ballistic DC on-current



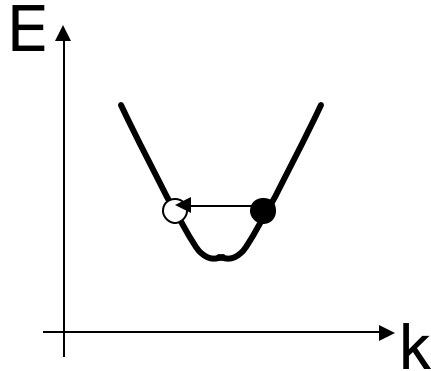
graphene



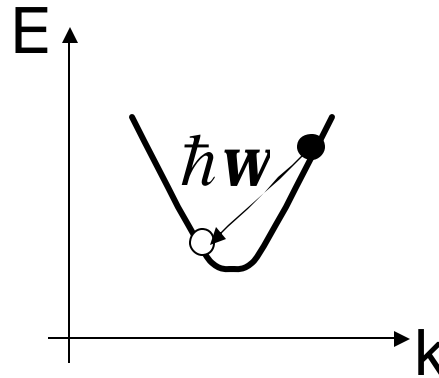
CNT

Phonon scattering dominates in CNTs

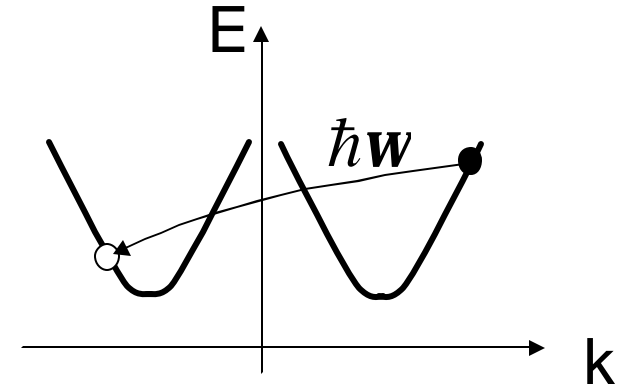
Yao, Kane, and Dekker, *Phys. Rev. Lett.*, **84**, 2941, 2000



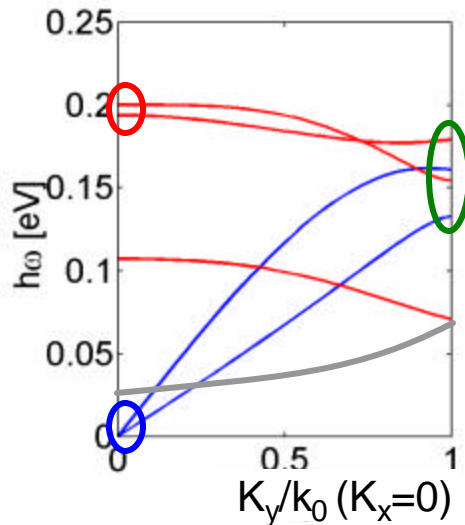
● AP



● OP (intra.)



● OP (intervalley)

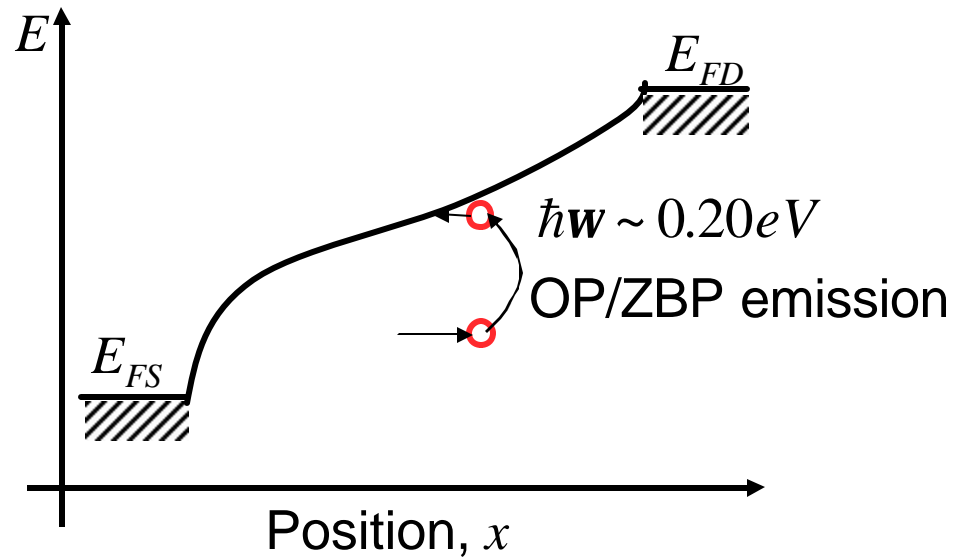


AP: long mfp ($I_1^{high} \sim 1 \mu\text{m}$)

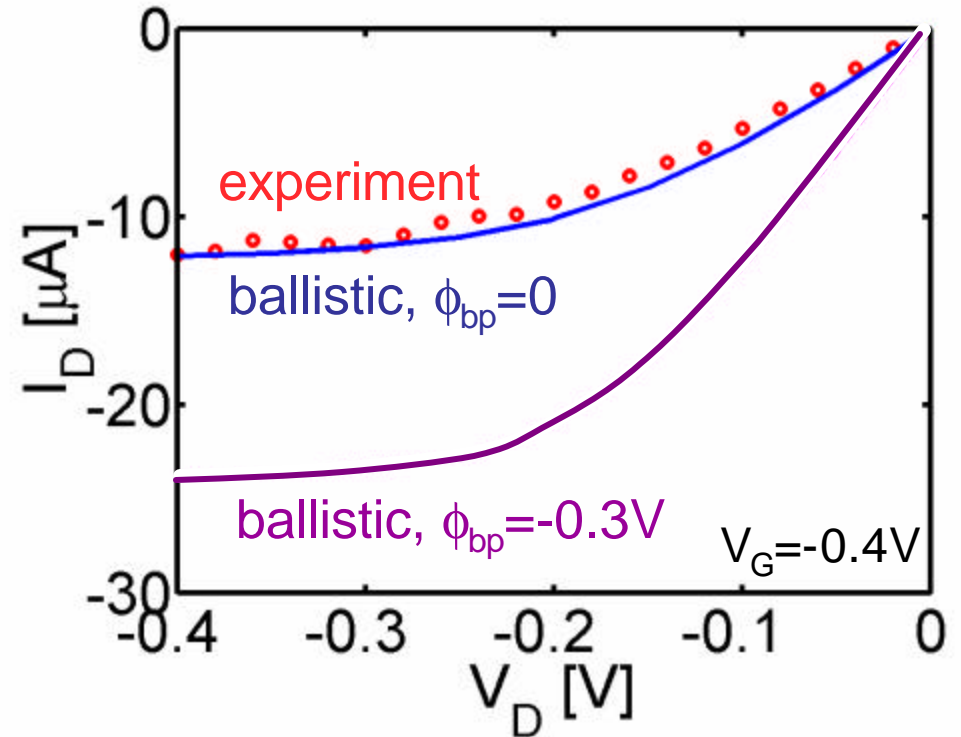
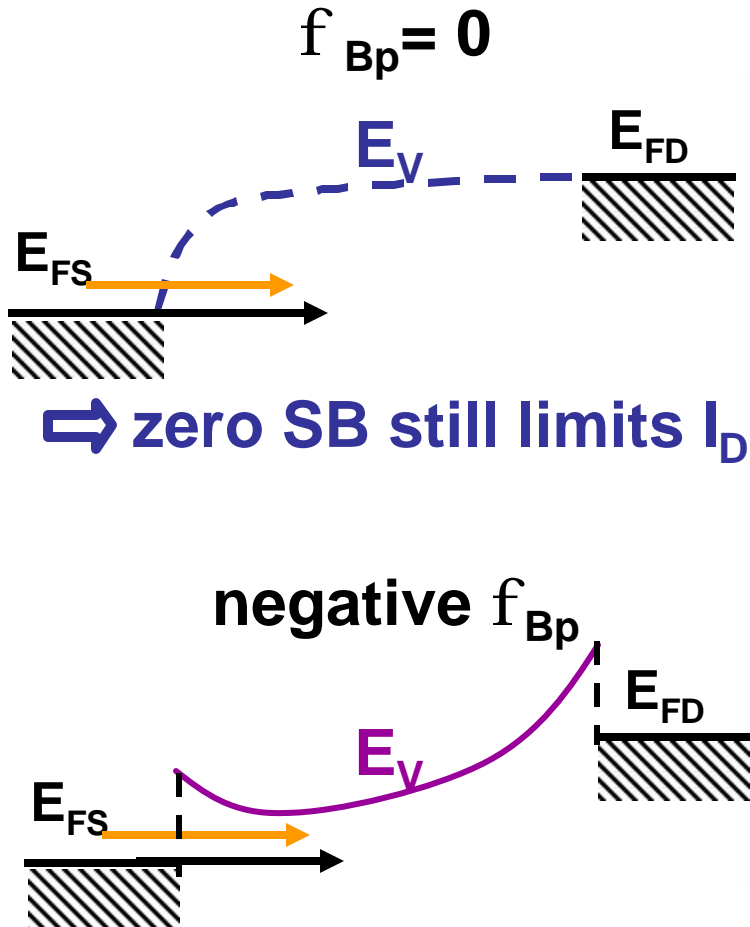
OP: short mfp ($I_2^{high} \sim 10 \text{nm}$, $\hbar\omega_{OP} \sim 0.2 \text{eV}$)

Javey, Guo, Paulsson et al., *Phys. Rev. Lett.*, **92**, 106804, 2004

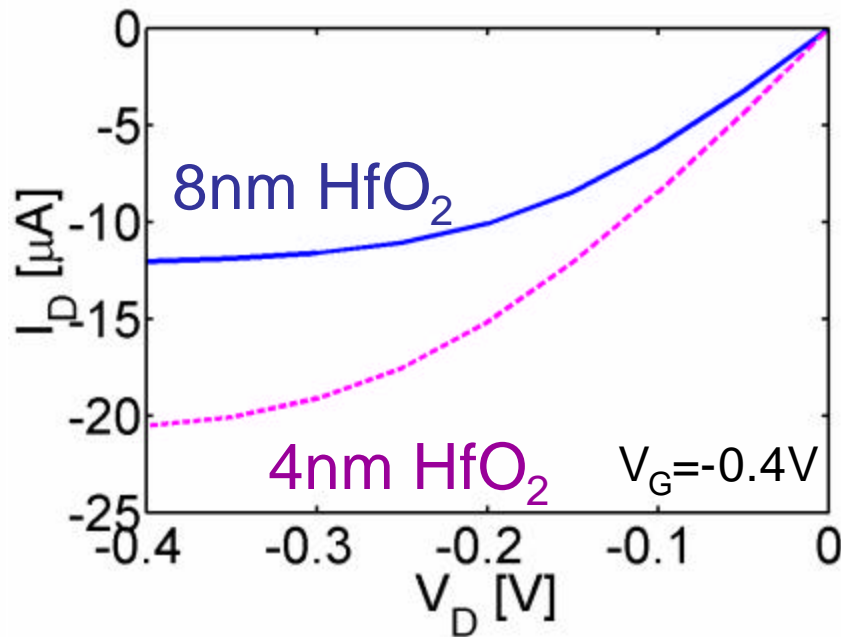
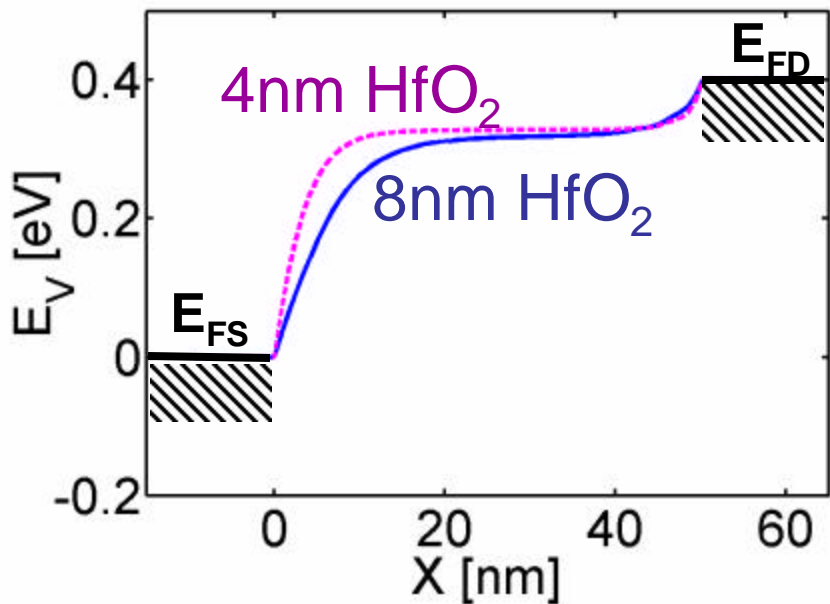
Park, Rosenblatt, Yaish et al., *Nano Lett.*, **4**, 517



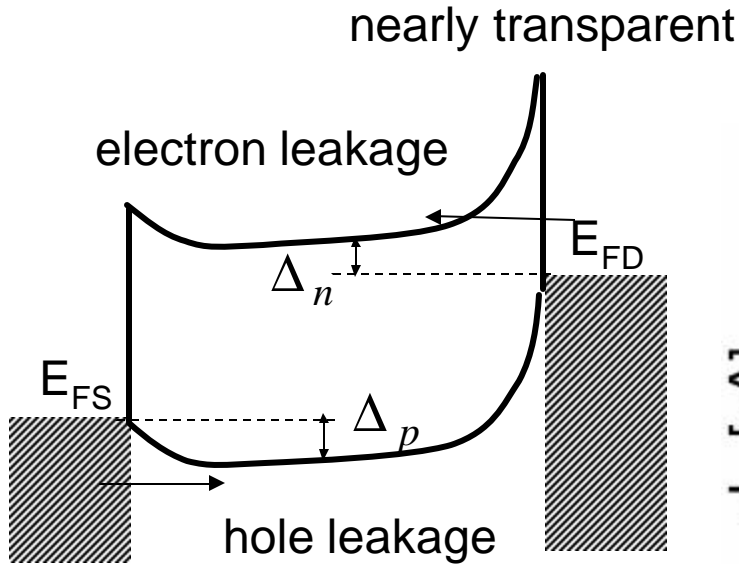
⇒ Deliver near-ballistic DC on-current
 confirmed by a separate Monte-Carlo simulation



Guo and Lundstrom,
IEEE TED, **49**,1897, 2002 (silicon)

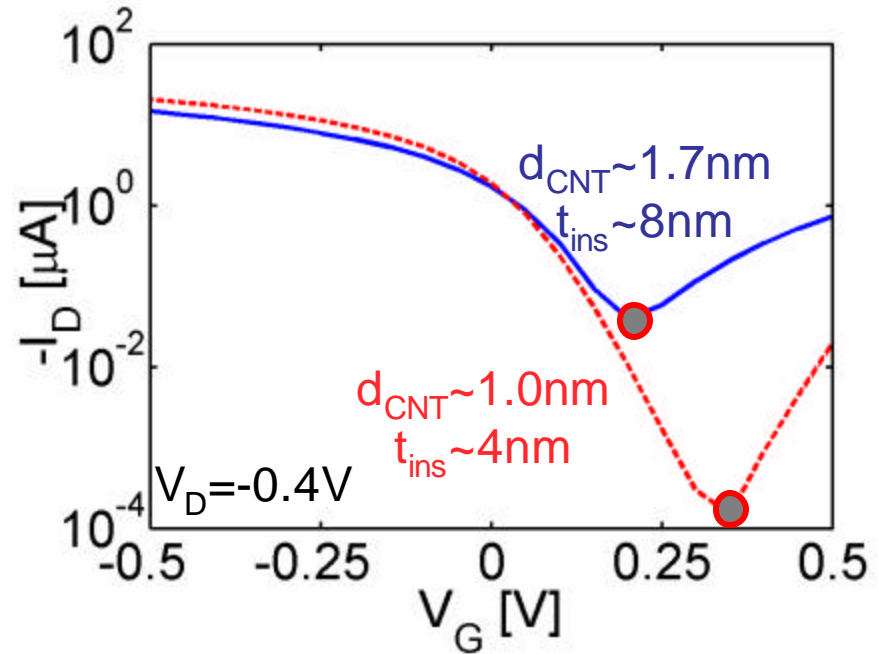


barrier thickness set by t_{ins}
(geometric screening)



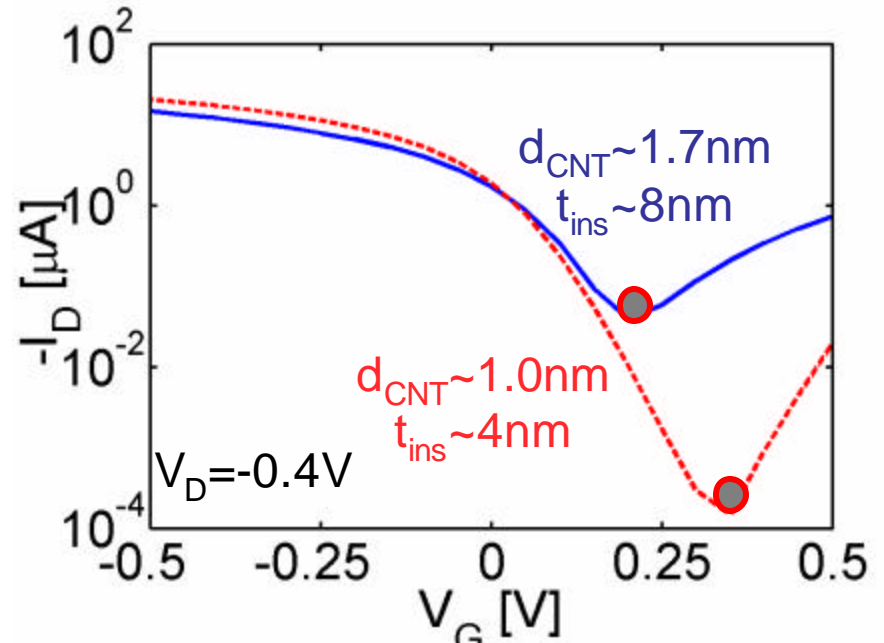
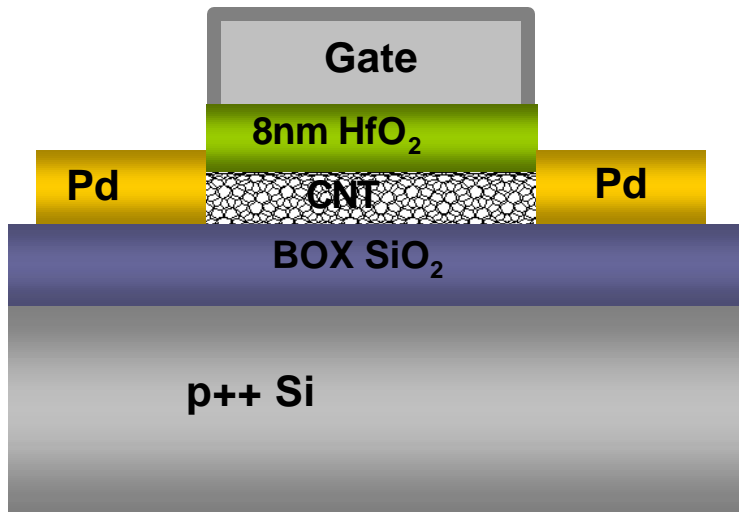
$$\Delta_n \sim \Delta_p \sim \frac{E_g - eV_D}{2}$$

$$E_g \sim 0.8\text{eV}/d(\text{nm})$$



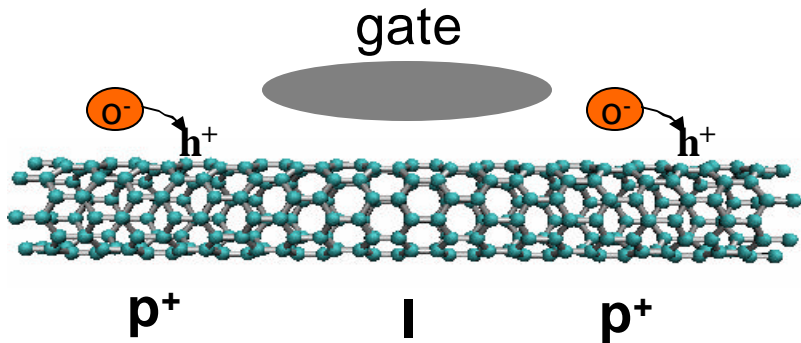
small d_{CNT} reduces I_{min}

CNT SBFET (Ballistic)



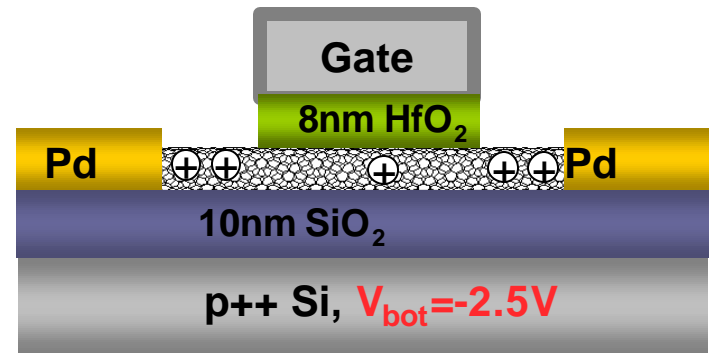
$L_G = 50\text{ nm}$
 $t_{\text{HfO}_2} = 4.0\text{ nm}$
 $t_{\text{box}} = 100\text{ nm}$
 $d_{\text{CNT}} = 1.0\text{ nm}$
 $R_{\text{DS}} = 0.0\ \Omega$

$I_{\text{ON}} \sim 16\ \mu\text{A}$ (12)
 $I_{\text{MIN}} \sim 10^{-4}\ \mu\text{A}$ (0.1 μA)
 $I_{\text{ON}}/I_{\text{MIN}} \sim 10^5$ (10^2)
 $S \sim 65\text{ mV/dec}$ (100 mV/dec)
 $g_m \sim 40\ \mu\text{S}$ (30 μS)



chemical S/D doping

Chen et al, 62nd DRC abstract, 2004

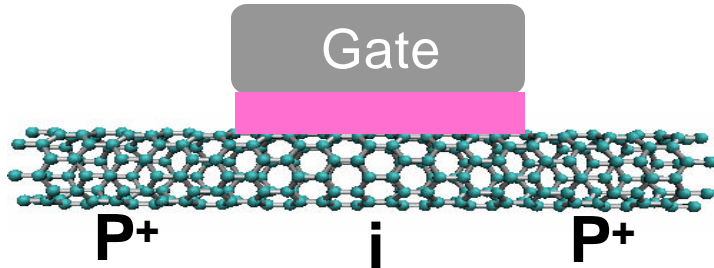


electrical S/D doping

Javey et al, Nano. Lett., 4, 447, 2003

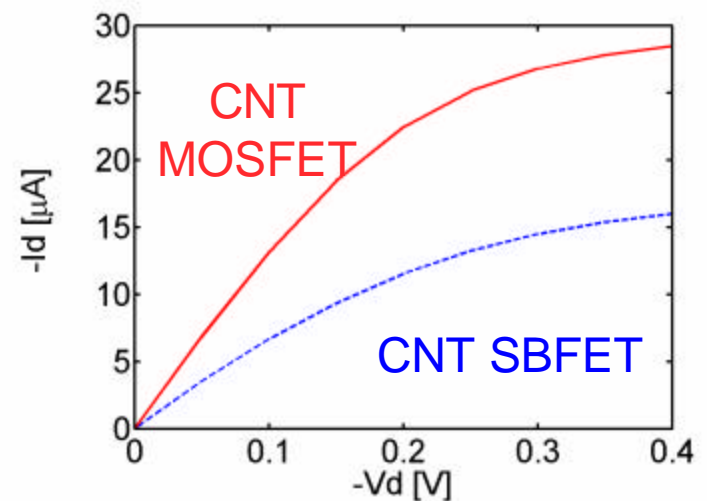
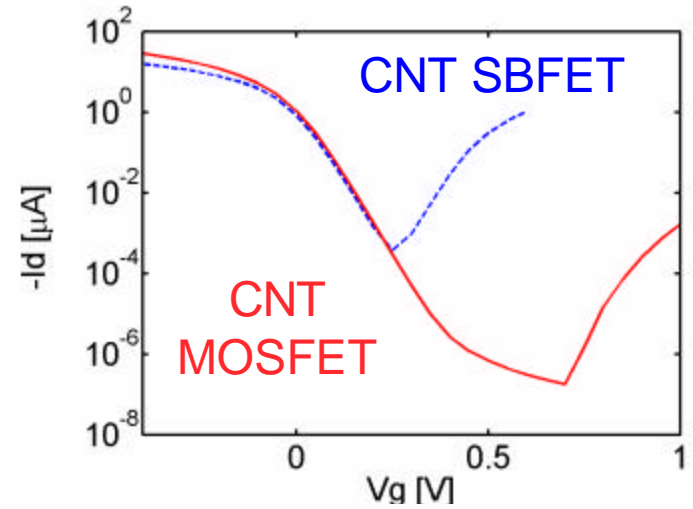
Lin et al, 62nd DRC abstract, 2004

CNT MOSFET (Ballistic)

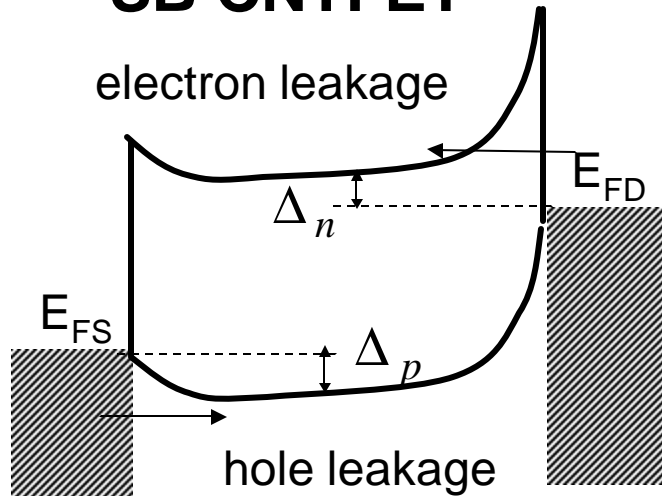


doped S/D CNT MOSFETs:

$I_{MAX} \sim 28 \mu A$	(16)
$I_{MIN} \sim 10^{-7} \mu A$	(10^{-4})
$I_{MAX}/I_{MIN} \sim 10^8$	(10^5)
$S \sim 65 \text{ mV/dec}$	(65)
$g_m \sim 80 \mu S$	(40)

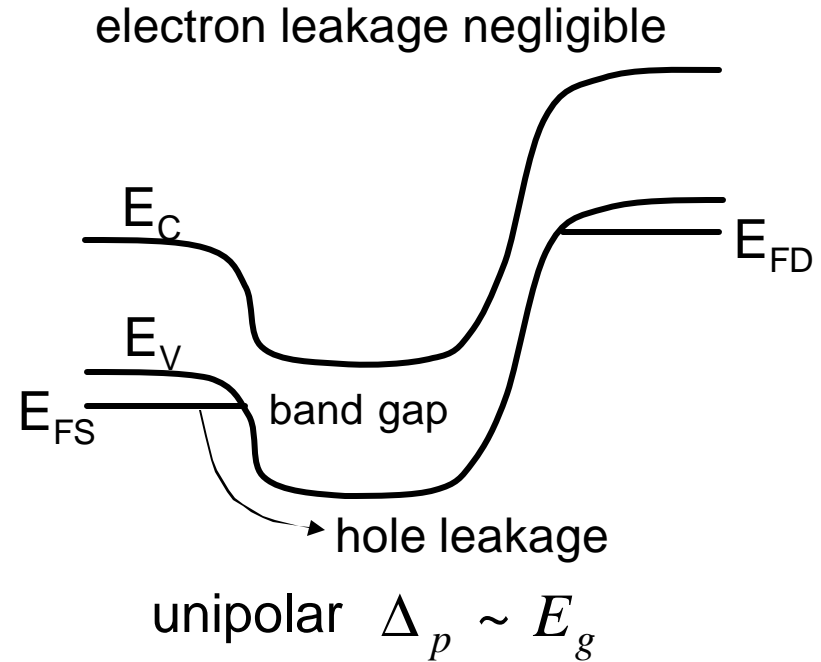


SB CNTFET

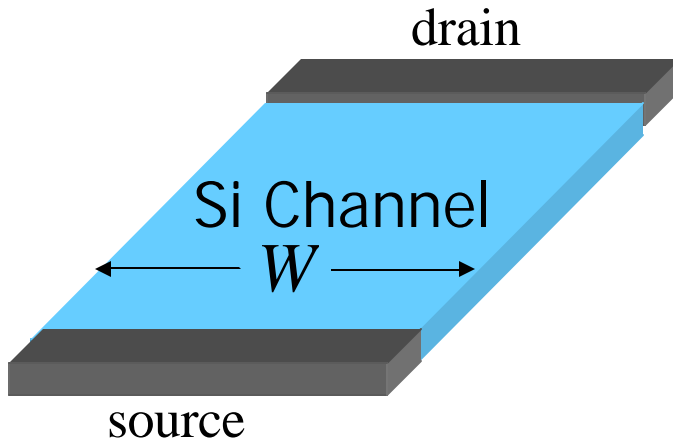


ambipolar $\Delta_n \sim \Delta_p \sim \frac{E_g - eV_D}{2}$

CNT MOSFET

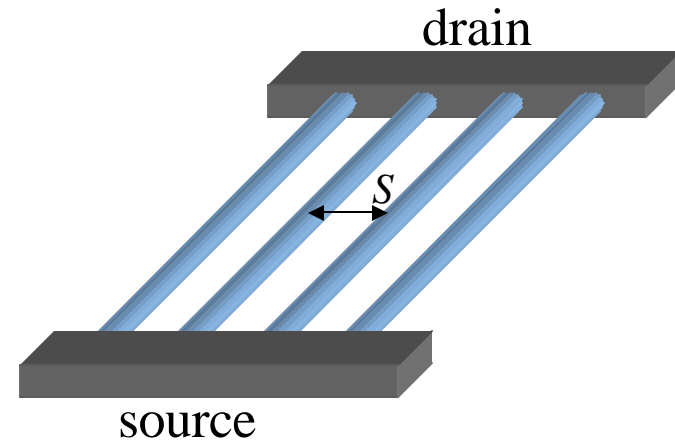


Suppressed ambipolar conduction



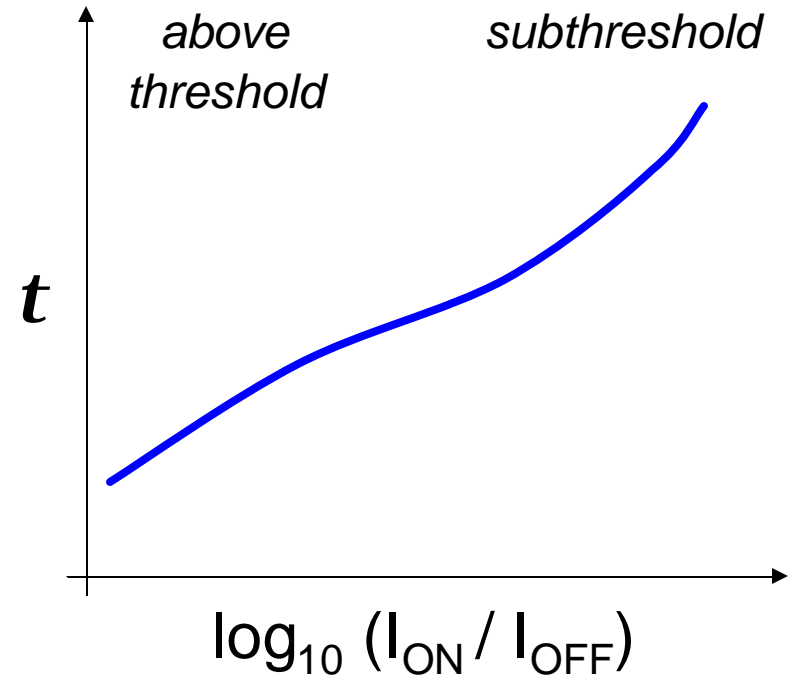
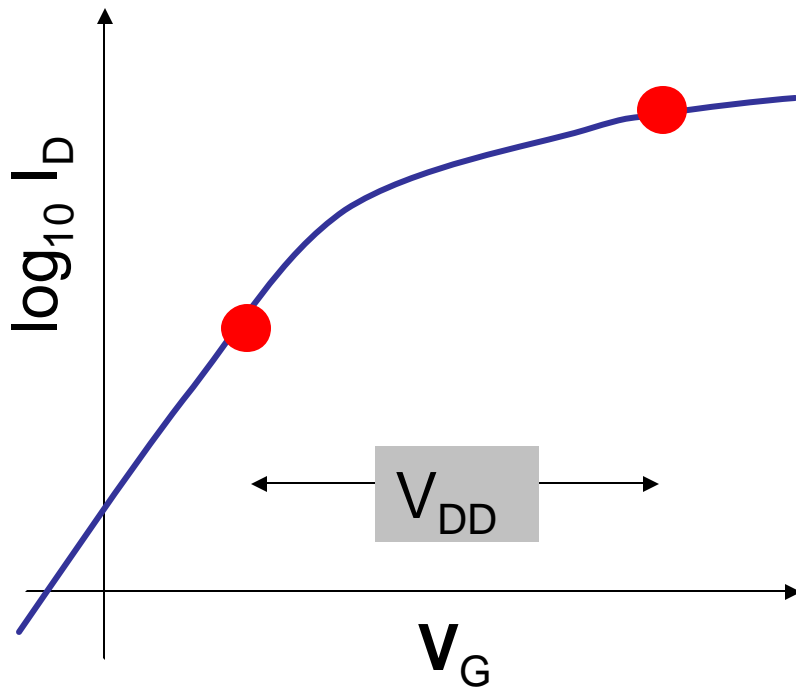
Si MOSFET

$$I_{ON} \text{ (mA/mm)}$$



CNT array FET

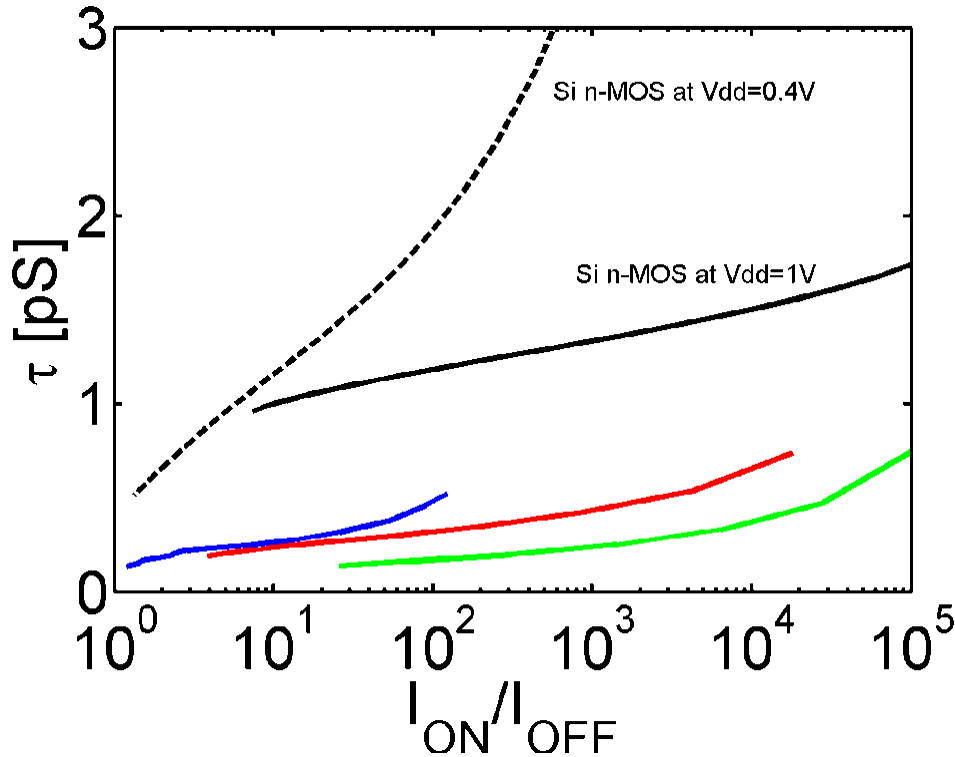
$$S = 2d_{CNT} ?$$



V_{DD} window specifies I_{ON} and I_{OFF}

device delay metric:

$$t = C_G V_{DD} / I_{ON}$$



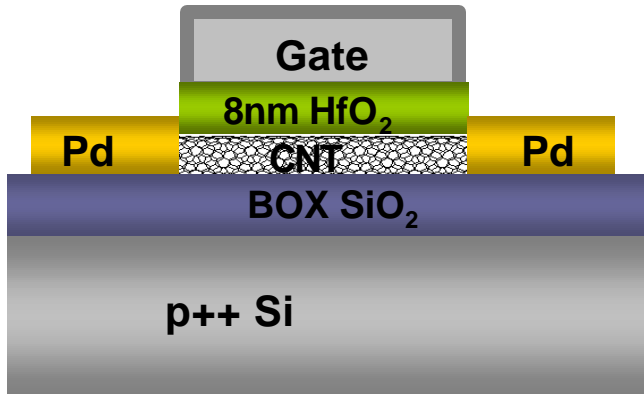
Si MOSFET ($V_{DD} = 0.4V$)

p-CNT SBFET (Javey)

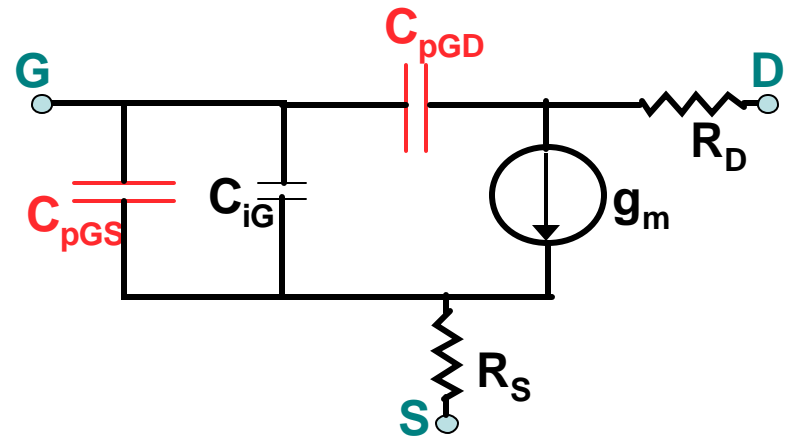
p-CNT SBFET (projected)

CNT MOSFET (projected)

Si n-MOS data is 70 nm L_G from 130 nm technology
from Antoniadis and Nayfeh, MIT



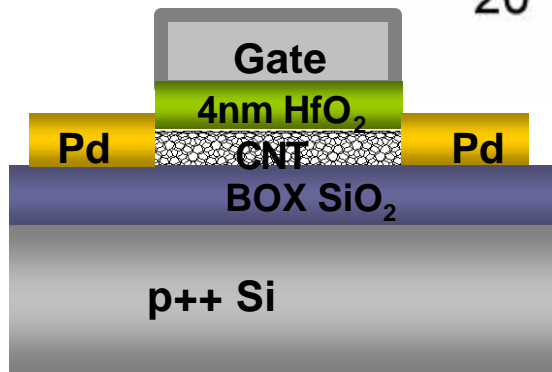
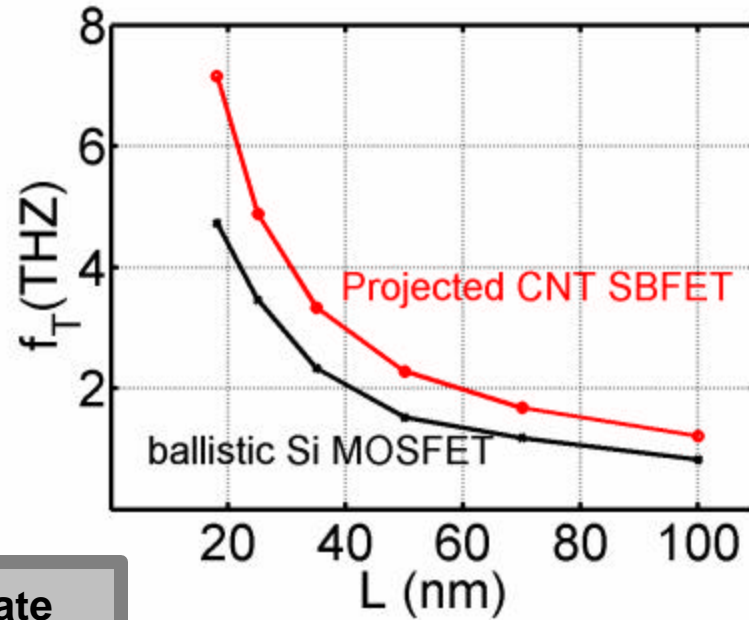
electrode width: $8\mu\text{m}$



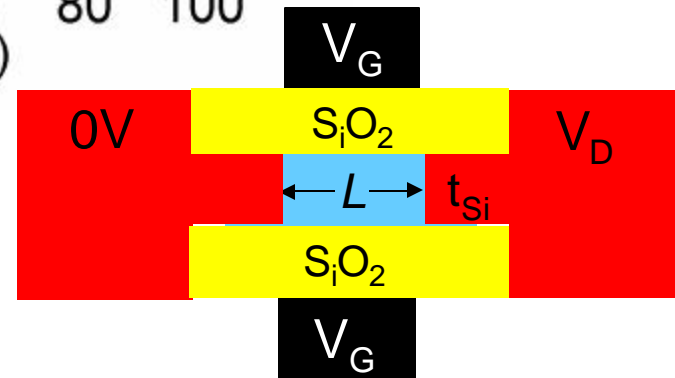
$$C_{G, \text{parasitic}} \sim 2\text{fF} \gg C_{G, \text{intrinsic}} \sim 3\text{aF}$$

$$f_T \approx \frac{g_m}{2\pi C_G} \approx 3\text{GHz}$$

⇒ RF performance limited by parasitic capacitance



projected CNT SBFET
 $t_{HfO_2} = 4.0$ nm, $d_{CNT} = 1.0$ nm



ballistic Si MOSFET
 $t_{SiO_2} = 1.2$ nm, $t_{Si} = 3.0$ nm

1. Introduction
2. Simulation Approach
3. Device Physics & Optimization
4. Summary

CNTFETs:

- coupled electrical-thermal transport
- High-frequency performance
- noise
- SPICE models
- CMOS applications

New applications:

- opto-electronics
- biological sensing

- 1) CNTFETs are promising devices
- 2) CNTFET technology is rapidly advancing
- 3) CNTFET device physics is interesting
- 4) Simulation capability rapidly advancing
- 5) Circuit and system performance needs to be assessed
- 6) New applications (beyond digital CMOS) should be explored

Theory: M. Lundstrom, S. Datta, M. P. Anantram,
M. Vaidyanathan, S. Hasan,

Experiment: A. Javey, H. Dai