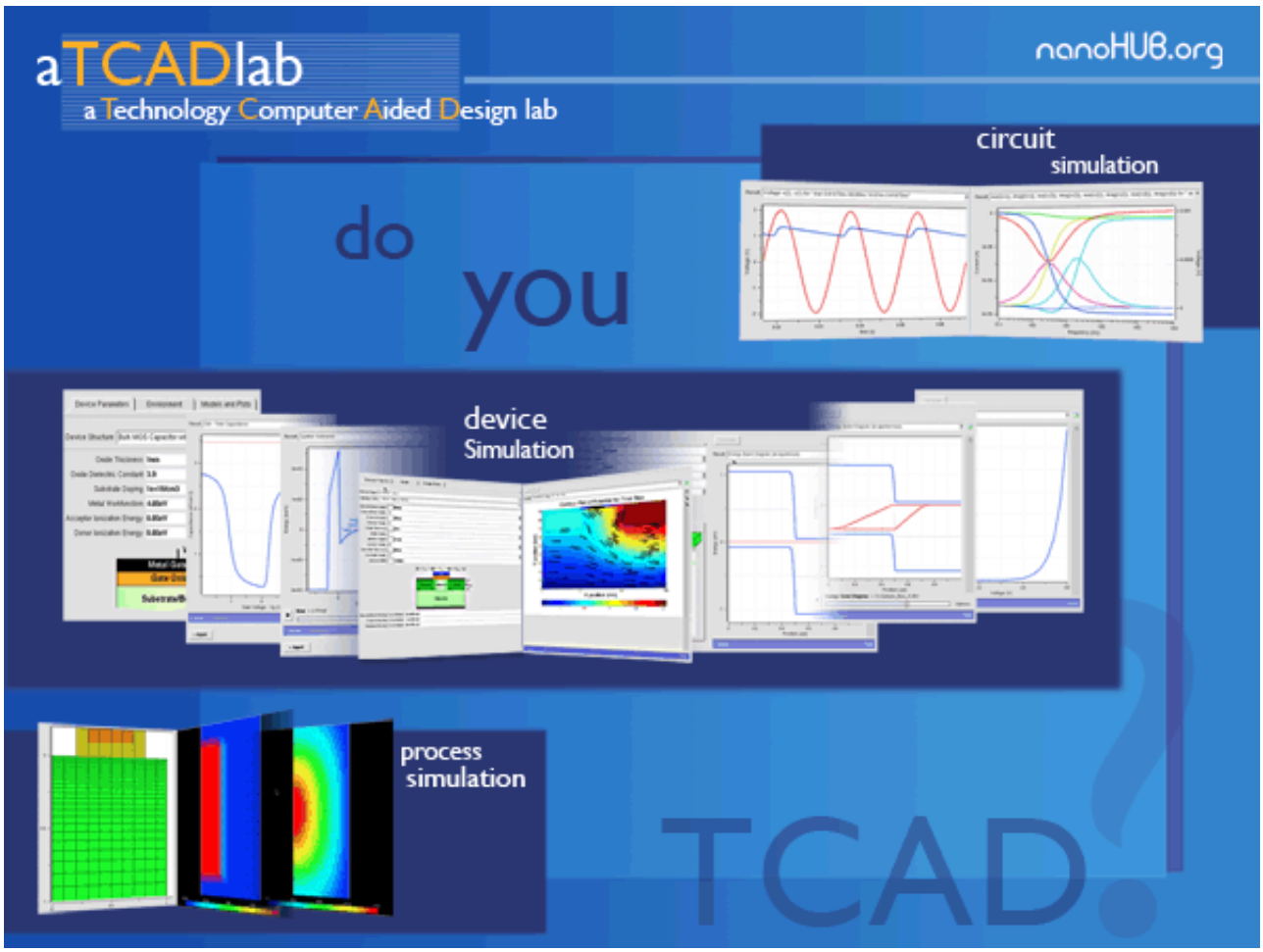
# a TCAD Lab




## Introduction to TCAD Simulation

The existing semiconductor industry is now fundamentally built on the assumption that almost every aspect of a chip is first designed in software.

Process simulation provides the ability to optimize and control the various processing steps, such as implantation, oxidation, diffusion, etching, and deposition, among others. Prophet and TSuprem are tools of choice on nanoHUB.org for this endeavor. However, learning about the basics of process simulation may be daunting at first, and there are four simplified process labs available in this tool set that guide students towards full-blown process simulation.

Device simulation either takes in-process simulation data or assumes certain device geometries, doping profiles, etc. and simulates electrical device performances. PADRE and Schred are tools of choice on nanoHUB.org for this simulation step. PADRE is a full-fledged simulation environment for semiclassical device simulation. It has a complicated input language that may be inappropriate for usage in those classroom environments where simple device modeling concepts need to be introduced. Drift-Diffusion Lab, PN junction Lab, MOScap, and

MOSFET are simplified GUI-driven tools that enable students (and professionals) to easily configure PADRE without requiring the user to master the PADRE input language.

Circuit simulation ultimately provides system level design capabilities. nanoHUB.org has a sinple interface to the Berkeley Spice3f4 for such usages.

This nanoHUB “topic page” provides an easy access to selected nanoHUB Semiconductor Device Education Material that is openly accessible and usable by everyone around the world.

We invite you to participate in this open source, interactive educational initiative:

- Contribute your content by uploading it to the nanoHUB. (See “Contribute Content”) on the nanoHUB mainpage.
- Provide feedback for the items you use on the nanoHUB through the review system. (Please be explicit and provide constructive feedback.)
- Let us know when things do not work for you by filing a ticket through the nanoHUB “Help” feature on every page.
- Finally, let us know what you are doing and give us your suggestions for improving nanoHUB.org by using the “Feedback” section, which you can find under “Support“

Thank you for using nanoHUB, and be sure to share your nanoHUB success stories with us. We like to hear from you, and our sponsors need to know that the nanoHUB is having impact.

## Semiconductor Process Modeling

Semiconductor process modeling is a vast field in which several commercial products are available and in use for production in industry and to some extent in education. nanoHUB is serving a few applications that are primarily geared towards education. The four tools entitled ‘Process Lab …’Oxidation, Oxidation Flux, Concentration Dependent Diffusion, and Point Defect Coupled Diffusion are all educational front-ends to the general Prophet tool in aTCADlab.

### Oxidation

(Image(/site/resources/tools/prolabox/prolabox.gif, 120, class=align-right) failed - File not found) The Oxidation Lab in aTCADlab simulates the oxidation process in integrated circuit fabrication. It is supported by a supplemental document that describes the theory and potential experiments that can be conducted.

### Oxidation Flux

(Image(/site/resources/tools/prolaboxflux/prolaboxflux.gif, 120, class=align-right) failed - File not found) The Process Oxidation Flux Lab in aTCADlab simulates the oxidation flux in the oxide growth process in integrated circuit fabrication. It is supported by a supplemental document that describes the theory and potential experiments that can be conducted.

### Concentration Dependent Diffusion

(Image(/site/resources/tools/prolabcdd/prolabcdd.gif, 120, class=align-right) failed - File not found) The Concentration Dependent Diffusion Lab in aTCADlab simulates the oxidation flux in the oxide growth process in integrated circuit fabrication.

### Point Defect Coupled Diffusion

(Image(/site/resources/tools/prolabdcd/prolabdcd.gif, 120, class=align-right) failed - File not found) The Point Defect Coupled Diffusion Lab in aTCADlab the point-defect-coupled diffusion process in integrated circuit fabrication.

### PROPHET

(Image(/site/resources/tools/prophet/prophet.jpg, 120, class=align-right) failed - File not found) PROPHET in aTCADlab was originally developed for semiconductor process simulation. Device simulation capabilities are currently under development. PROPHET solves sets of partial differential equations in one, two, or three spatial dimensions. All model coefficients and material parameters are contained in a database library which can be modified or added to by the user. Even the equations to be solved can be specified by the end user. It is supported by an extensive set of User Guide pages and a seminar on Nano-Scale Device Simulations Using PROPHET.

## Device Simulation

### Drift Diffusion Lab

(Image(/site/resources/tools/semi/excess_carrier_intrinsic_slab_bias.png, 120, class=align-right) failed - File not found)
(Image(/site/resources/tools/semi/excess_carrier_profile_light_left.png, 120, class=align-right) failed - File not found) (Image(/site/resources/tools/semi/excess_carrier_profile_light_top.png, 120, class=align-right) failed - File not found) The Drift Diffusion Lab in aTCADlab enables a user to understand the basic concepts of drift and difusion of carriers inside a semiconductor slab using different kinds of experiments. Experiments like shining light on the semiconductor, applying bias and both can be performed. This tool provides important information about carrier densities, transient and steady state currents, fermi-levels and electrostatic potentials. It is supported by two related homework assignments #1 and #2 in which Students are asked to explore the concepts of drift, diffusion, quasi Fermi levels, and the response to light.

Exercises:

- Conductivity - Theoretical Exercise

### PN Junction Lab

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(Image(/site/resources/tools/pntoy/pntoy2.gif, 120, class=align-right) failed - File not found)
(Image(/site/resources/tools/pntoy/pntoy1.gif, 120, class=align-right) failed - File not found)
(Image(/site/resources/tools/pntoy/pnjunction.gif, 120, class=align-right) failed - File not found)
PN-Junction Lab in aTCADlab: Everything you need to explore and teach the basic concepts of P-N junction devices. Edit the doping concentrations, change the materials, tweak minority carrier lifetimes, and modify the ambient temperature. Then, see the effects in the energy band diagram, carrier densities, net charge distribution, I/V characteristic, etc.

There is a significant set of associated resources available for this tool.

- a demo of this tool
- a Primer on Semiconductor Device Simulation.
- a Learning Module entitled PN Junction Theory and Modeling which walks students through the PN junction theory and let's them verify concepts through on-line simulation.
- Homework assignment on the depletion approximation
- Homework assignment on the depletion approximation

Exercises:

- PN Diode Exercise: Series Resistance
- Exercise: PIN Diode
- PN Diode Exercise: Graded Junction
- Basic operation of a PN diode - Theoretical exercise
- PN diode - Advanced theoretical exercises
- Schottky diode - Theoretical exercises

## Bipolar Junction Transistor Lab

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(Image(/site/resources/tools/bjt/2npn_output.gif, 120, class=align-right) failed - File not found)
The Bipolar Junction Lab in aTCADlab allows Bipolar Junction Transistor (BJT) simulation using a 2D mesh. It allows user to simulate npn or pnp type of device. Users can specify the Emitter, Base and Collector region depths and doping densities. Also the material and minority carrier lifetimes can be specified by the user. It is supported by a homework assignment in which Students are asked to find the emitter efficiency, the base transport factor, current gains, and the Early voltage. Also a qualitative discussion is requested.

Exercises:

- BJT - Simulation Exercise
- BJT - Theoretical Exercise
- BJT Operation Description

## MOScap

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(Image(/site/resources/tools/moscap/moscap.jpg, 120, class=align-right) failed - File not found)
The MOScap Tool in aTCADlab tool enables a semi-classical analysis of MOS Capacitors. Simulates the capacitance of bulk and dual gate capacitors for a variety of different device sizes, geometries, temperature and doping profiles.

Exercises:

- Exercise: CV curves for MOS capacitors
- MOSCAP - Theoretical Exercises 1
- MOSCAP - Theoretical Exercises 2
- MOSCAP - Theoretical Exercises 3
- MOS Capacitors: Theory and Modeling

## Schred

(Image(/images/tool/schred/schred.jpg, 120, class=align-right) failed - File not found) Schred Tool in aTCADlab calculates the envelope wavefunctions and the corresponding bound-state energies in a typical MOS (Metal-Oxide-Semiconductor) or SOS (Semiconductor-Oxide-Semiconductor) structure and a typical SOI structure by solving self-consistently the one-dimensional (1D) Poisson equation and the 1D Schrodinger equation.

Exercises:

- Schred: Exercise 1
- SCHRED: Exercise 2
- Schred: Exercise 3
- Quantum Size Effects and the Need for Schred
- Schred Tutorial Version 2.1

## MOSfet Lab

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(Image(/site/resources/tools/mosfet/mosfet.jpg, 120 ,class=align-right) failed - File not found)
The MOSfet Lab in aTCADlab tool enables a semi-classical analysis of current-voltage characteristics for bulk and SOI Field Effect Transistors (FETs) for a variety of different device sizes, geometries, temperature and doping profiles.

Exercises:

- MOSFET Exercise
- Exercise: Basic Operation of n-Channel SOI Device
- MOSFET - Theoretical Exercises
- MOSFET Operation Description

### PADRE

(Image(/site/resources/tools/padre/padre.jpg, 120, class=align-right) failed - File not found) PADRE in aTCADlab is a 2D/3D simulator for electronic devices, such as MOSFET transistors. It can simulate physical structures of arbitrary geometry—including heterostructures—with arbitrary doping profiles, which can be obtained using analytical functions or directly from multidimensional process simulators such as . A variety of supplemental documents are available that deal with the PADRE software and TCAD simulation:

- User Guide
- Abbreviated First Time User Guide
- FAQ
- A set of course notes on Computational Electronics with detailed explanations on bandstructure, pseudopotentials, numerical issues, and drift diffusion.
- Introduction to DD Modeling with PADRE
- Description and Semiclassical Simulation With PADRE
- A Primer on Semiconductor Device Simulation (Seminar)

Exercises:

- BJT Problems and PADRE Exercise
- Introduction to DD Modeling with PADRE
- MOS Capacitors: Description and Semiclassical Simulation With PADRE

## Circuit Simulation

### SPICE3f4

(Image(/site/resources/tools/spice3f4/spice3f42.jpg, 120, class=align-right) failed - File not found) SPICE3f4 in aTCADlab s a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analysis. It was developed at the University of California, Berkeley. Version 3F4 was released in 1993. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, transmission lines, and the four most common semiconductor devices: diodes, BJT's, JFET's, and MOSFET's. SPICE has built-in models for the semiconductor devices, and the user need specify only the pertinent model parameter values.

- Getting Started
- FAQ
- User's Manual

- EECS University of Berkeley Spice3 Website

## About aTCADlab Constituent Tools

The aTCADlab has been put together from individual disjoint tools to enable educators, students, and profesionals to have a one-stop-shop in TCAD tools education. It therefore benefits tremendously from the hard work that the contributors of the individual tool builders have put into their tools.

As a matter of credit, simulation runs that are performed in the aTCADlab tool are also credited to the individual tools, which help the ranking of the individual tools. We do also count the number of usages of the individual tools in the aTCADlab tool set, to measure the aTCADlab impact and possibly also improve the tool.

In the description above we do not refer to the individual tools since we want to guide the users to the composite aTCADlab tool. We cite the individual tools here explicitly so they are being given the appropriate credit and on their rspective tool pages are being linked to this aTCADlab topic page.

Process Lab:Oxidation, Process Lab: Oxidation Flux, Process Lab: Concentration-Dependent Diffusion, Process Lab: Defect-coupled diffusion, Prophet, Drift-Diffusion Lab, PN Junction Lab, BJT Lab, MOSCap, Schred, MOSFet, Padre, and Spice3f4.

## Other TCAD Tools

### TSuprem4

(Image(/site/resources/tools/tsuprem4/tsuprem2.png, 120, class=align-right) failed - File not found) TSuprem4 simulates the processing steps used in the manufacture of silicon integrated circuits and discrete devices. The types of processing steps modeled by the current version of the program include ion implantation, inert ambient drive-in, silicon and polysilicon oxidation and silicidation, epitaxial growth, and low temperature deposition and etching of various materials.

Because of the way TSUPREM-4 is licensed, it is available only to users on the West Lafayette campus of Purdue University. Note that you must use a network connection on campus, or else you will get an 'access denied' message.