Fall 2008

EE 612: Nanoscale Transistors
TTh 10:30 –11:45 AM, EE117

Instructor: Mark Lundstrom (lundstro@purdue.edu)
Office: EE 310
Office Hours: MWF: 5:00 - 6:00 PM
(Please let me know by e-mail that you are coming by or use e-mail to make an appointment for a different time.)

Course Assistant: Changwook Jeong (jeongc@purdue.edu)

Prerequisite: EE 606

Text:  
Fundamentals of Modern VLSI Devices,
Yuan Taur and Tak H. Ning, Cambridge Univ. Press
ISBN: 0 521 55056 4 (hardback) 0 521 55959 6 (paperback)

Advanced Semiconductor Fundamentals, 2nd Edition

Course Web Page: Handout materials and course announcements will be available from the course web page (http://cobweb.ecn.purdue.edu/~ee612/). PowerPoint plus audio lectures from Fall 2006 and for the current semester will also be available on the course website.

Grading:

Exam 1: 25%  (Thursday, October 2)
Exam 2 25%  (Thursday, November 13)
Homework: 25%
Final: 25%

Course Description: This course examines the device physics of advanced transistors and the process, device, circuit, and systems considerations that enter into the development of new integrated circuit technologies. The course consists of three parts. Part 1 treats silicon MOS and MOSFET fundamentals as well as second order effects such as gate leakage and quantum mechanical effects. Short channel effects, device scaling, and fabrication processes and reliability are the subject of Part 2. In Part 3, we discuss circuit and systems issues and then examine strained silicon, III-V HEMTs, and nanowire transistors. The use of computer simulation to examine device issues is an integral part of the course.

Academic Dishonesty: Cheating of any kind is unacceptable and may result in a grade of zero on the assignment, exam, or course – depending on the severity of the incident as determined by me. Discussions between students about assignments are encouraged, but showing your solution or program to another student is unacceptable.
**EE-612: Course Outline Fall 2008**

**Part 1: MOSFET Fundamentals**

(6 weeks)

- Course intro / Review of semiconductor fundamentals pp. 1-31
- 1D MOS electrostatics pp. 58-68
- MOS capacitors pp. 68-74, 82-90
- Polysilicon gates / QM effects pp. 74-78, 194-200
- MOSFET IV: Square law pp. 112-117
  - Bulk charge pp. 117-125
  - Velocity saturation pp. 149-158, 283-285
- Ballistic MOSFETs class notes
- Quasi-Ballistic MOSFETs class notes
- Subthreshold conduction pp. 125-129
- \( V_T \), body effect, capacitance pp. 129-131, 78-82, 200-202, 135-137, 244-247

Review and catch up
EXAM 1 (Thursday, October 2)

**Part 2: Short Channel MOSFETs and CMOS Processes**

(5.5 weeks)

- Effective mobility pp. 132-135
- 2D Electrostatics pp. 139-149
- FALL BREAK (Tuesday, October 14)
- MOSFET Scaling and the ITRS pp. 164-173
- Channel profile design pp. 173-202
- Parasitic S/D resistance / \( L_{eff} \) pp. 158-160, 240-244, 202-221
- Breakdown and Leakage pp. 90-97, 160-161, 99-100
- Gate resistance / Interconnects pp. 247-257
- CMOS processes pp. 414-417
- CMOS reliability pp. 97-106

Review and catch up
EXAM 2 (Thursday, November 13)
### Part 3: CMOS Circuits plus new Materials and Structures (3.5 weeks)

- **CMOS circuits: I**
- **CMOS circuits: II**
- **RF CMOS**
- **THANKSGIVING BREAK (November 27)**
- **Strained silicon**
- **SOI MOSFETs**
- **Heterostructures, Heterostructure FETs and BJTs**
- **Nanotube and semiconductor nanowire FETs**

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