SOLUTIONS: ECE 606 Homework Week 15
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1) The purpose of this exercise is to help you review the basic theory of the MOSFET, introduce you to some key device parameters, and give you a feel for the typical values of key device performance metrics for state-of-the-art MOSFETs.

Step 1: View the online presentation: “A Review of MOSFET Fundamentals,” by Mark Lundstrom. This online lecture is available at nanoHUB.org at https://www.nanohub.org/resources/5307 (Viewing this lecture is also a good way to study for Exam 6.)

Step 2: For the exercises below, you will need to run the simulation program, nano-CMOS, on nanoHUB.org. Be sure you have an account, then proceed with the exercises below.

Locate the simulation tool, nano-CMOS (https://nanohub.org/tools/nanocmos), and use it to examine the IV characteristics of “45nm” N-channel CMOS technology. Select “NMOS 45nm,” and use the default values. Push the “Simulate” button, and then answer the following questions.

You should clearly describe how you obtain each parameter. Note that you are able to change the minimum and maximum axes scales and to select either linear or logarithmic scales.

1a) Determine the on-current in µA/µm
1b) Determine the off-current in µA/µm

Solutions:
On current: \( I_D \) when \( V_{GS} = V_{DS} = V_{DD} \) (power supply voltage). On-current = 1301 µA/µm

Off-Current: \( I_D \) when \( V_{GS} = 0 \) and \( V_{DS} = V_{DD} \). By extrapolating to \( V_{GS} = 0.0 \) V, the off-current is about 0.1µA/µm. Off-current = 0.1 µA/µm

See figure below:
1c) Determine the subthreshold swing, $S$, in mV/decade

**Solution:**

This parameter quantifies how abruptly the transistor turns on with increasing gate voltage (it is the inverse of subthreshold slope). It is defined as the gate-voltage change needed to induce a drain-current change of one order of magnitude. We typically do this at high $V_D$, because high drain voltages may degrade the SS by 2D electrostatics, so this is a worst case.

**Subthreshold Swing \sim 100 \text{ mV/decade}**
1d) Estimate $V_{DSAT}$ for $V_{GS} = 1.0\text{V}$. (Do not simply “eyeball” the answer; develop a simple methodology so that another person who follows it would get the same answer.

**Solution:**

$V_{DSAT}$:

$V_{DSAT}$ is the value of Drain Voltage at which $I_DS$ saturates. $V_{DSAT}$ ↑ as $V_G$ ↑. Since $V_{DSAT}$ is a function of $V_G$, here $V_{DSAT}$ is taken for maximum $V_G$ i.e. $V_{GS} = V_{DD}$. To determine $V_{DSAT}$ from the $I_D$ - $V_D$ plot, tangents to the linear and saturation regions of the $I_D$ - $V_D$ plot are drawn, and their intersection gives the value of $V_{DSAT}$.

$V_{DSAT} \sim 0.28\text{ V}$ (Note that $V_{DSAT} < V_D - V_T$, where, from f) below, $V_T \sim 0.31\text{ V}$. $V_D - V_T = 1.0 - 0.31 = 0.69$. So the drain current saturates at a much lower voltage than the classic “pinch-off” theory says it should.
1e) Estimate the DIBL in mV/V

**Solution:**

When the source and drain depletion regions are a substantial fraction of the channel length, “short-channel effects” start to occur. DIBL is caused by lowering of the source-junction potential barrier. As the drain bias is increased, the conduction band edge, which reflects the electron energies in the drain, is pulled down and the drain channel depletion width expands. The net result is an increase in leakage current between the source and drain with increasing drain bias.

DIBL is calculated by taking the horizontal shift in the sub-threshold characteristics (in millivolts) divided by change in the $V_D$, on log $I_D$ - $V_{GS}$ plot. We select a region of the plot where the drain current is exponential with gate voltage (linear on the log $I_D$ plot) and where the low $V_D$ and high $V_D$ characteristics are parallel. In this case, we selected $I_D = 10$ uA/um.

$$\text{DIBL} \sim 120 \ (1.0 - 0.9) = 133 \text{ mV/V}$$
1f) Estimate $V_{TH}(\text{lin})$ and $V_{TH}(\text{sat})$ in V

**Solution:**

$V_{TH}(\text{lin})$:

This is the threshold voltage for $V_D << V_G$ (i.e. in the linear region of operation). It is obtained by fitting a line to the point of maximum slope, and then finding the intercept with the x-axis.

$V_{TH}(\text{Lin}) \sim 0.35 \text{ V}$

$V_{TH}(\text{sat})$:

This is the threshold voltage for high $V_D$ (the saturated region of operation). $V_{TH}(\text{sat}) \sim 0.31 \text{ V}$
1g) Estimate the output resistance, $R_0$, in Ω-µm for $V_G = V_{DD}$.

**Solution:**

This parameter reflects the non-saturating drain current with drain bias. It is calculated using the formula $R_0 = \Delta V_D / \Delta I_D$. $R_0 = \Delta V_D / \Delta I_D = 1/(1301-900 \text{ uA}) \sim 2500 \Omega\text{-um}$
1h) Estimate the channel resistance, $R_{CH}$ in $\Omega \cdot \mu m$

Solution:

Channel Resistance ($R_{CH}$):

At small drain biases, a MOSFET acts like a resistor (the linear portion of $I_D - V_D$ plot). The total resistance ($R_{TOT}$) is the sum of the source-drain series resistance and the channel resistance. It is calculated by taking point 1 on the linear portion of $I_D - V_D$ and point 2 is taken at the origin. $R_{TOT}$ is then calculated by using the formula $R_{TOT} = \frac{\Delta V_D}{\Delta I_D}$. For point 1, we use a very small drain voltage. In this case, $V_D = 0.05V$ was used and we find: $R_{TOT} = 259 \, \Omega \cdot \mu m$, $R_{CH} = 259 \, \Omega \cdot \mu m - R_{sd} (= 150 \, \Omega \cdot \mu m) = 109 \, \Omega \cdot \mu m$

![Graph of I_D vs. V_D](image)

1i) Estimate the transconductance, $g_m$, in mS/mm at the maximum gate (and drain) voltage.

Solution:

This parameter measures the magnitude of the drain current change when the gate voltage changes. It is calculated by using the points indicated on the plot below and using the formula:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = 1900 \, \text{mS/mm}$$
HW Week 15 continued

The units for transconductance are Siemans per meter, or milliSiemans per millimeter or microSiemans per micrometer. Device people tend to use mS/mm, but all three have the same numerical value.

\[
\Delta I_D = (1301 - 1111) \, \mu A/\mu m \\
\Delta I_D = 190 \, \mu A/\mu m \\
\Delta V_{GS} = 0.1 \, V \\
g_m = \frac{\Delta I_D}{\Delta V_{GS}} = 1900 \, \mu S/\mu m
\]

1) The “self-gain, \( A = g_m R_0 \)” is often used as a metric for analog applications (it is roughly the maximum small signal gain that could be achieved in an amplifier circuit with this transistor). Estimate the self-gain for this transistor.

**Solution:**

\[g_m = 1900 \, \mu S/\mu m\]
\[R_0 = 2500 \, \Omega - \mu m\]

\[A = g_m R_0 = 4.8\]

**Additional Exercise:** Repeat problem 1) for a p-channel MOSFET by selecting “PMOS 45nm,” and pushing the “Simulate” button. You should use the default values. Estimate all of the device parameters listed problem 1) for this PMOS transistor. Discuss the main difference that you see.
2) The purpose of the following three exercises below is to review MOS electrostatics using the numerical simulation program, MOSCap (https://nanohub.org/tools/moscap) on nanoHUB.org.

Use the same parameters we used for the 45 nm N-MOSFET in 1):

\[ N_A = 2.7 \times 10^{18} \, \text{cm}^{-3} \text{ for the bulk doping} \]
\[ x_0 = EOT = 1.1 \, \text{nm} \]
\[ Q_F = 0 \]
\[ T = 300 \, \text{K} \]
\[ V_{DD} = 1.0 \, \text{V} \]
Assume an n+ polysilicon gate with \( (E_F - E_C) = 0.0 \) and ignore poly depletion.

2a) Determine the following quantities by analytical calculations (assume \( V_G = 0 \, \text{V} \)). You should use the delta-depletion approximation for these calculations.

(The first thing that a prudent engineer does when using a new simulation program is to check the results to be sure that he or she using the program properly and that the program is producing correct results – at least for one problem similar to the problem of interest. Good engineers take responsibility to be sure that a simulation tool is producing correct results for their problem. In question 2b), we will run MOSCap and compare answers to the analytical results.)

Solutions:
We solved this problem in HW12 Q2, so we can just list the numbers.

(i) The flatband voltage, \( V_{FB} \)

\[ \phi_m = -1.06 \, \text{V} \]

(ii) The surface potential, \( \phi_S \)

\[ \phi_S = 0.74 \, \text{V} \]

(iii) The electric field in the oxide, \( E_{ox} \)

\[ E_{ox} = 2.3 \times 10^6 \, \text{V/cm} \]

(iv) The electric field in the silicon at the surface, \( E_{Si} \)
HW Week 15 continued

\[ E_S = 7.9 \times 10^5 \text{ V/cm} \]

(v) The depletion region depth, \( W_D \)
\[ W_D = 19.3 \text{ nm} \]

(vi) The charge in the silicon, \( Q_S \)
\[ Q_S = -8.34 \times 10^{-7} \text{ C/cm}^2 \]

(vii) The charge on the gate, \( Q_G \)
\[ Q_G = -Q_S = +8.34 \times 10^{-7} \text{ C/cm}^2 \]

(viii) The voltage drop across the oxide, \( \Delta \phi_{\text{ox}} \)
\[ \Delta \phi_{\text{ox}} = 0.23 \text{ V} \]

(ix) The threshold voltage for this MOS capacitor, \( V_T \)
\[ V_T = 0.25 \text{ V} \]

2b) Simulate the above MOS capacitor using MOSCap on the nanoHUB. Use the same p-type doping and gate oxide thickness as in problem (1), and a voltage range of 2V to -4V. You can answer the following questions by reading the data from the MOSCap plots or by downloading the data as text. From the results, deduce the following quantities:

**Solutions:**

Model: single gate  
Gate insulator thickness: 1.1nm  
Gate insulator nodes: 20  
Gate insulator dielectric constant: 3.9  
Semiconductor thickness: 30 nm  
Semiconductor layer nodes: 100  
Semiconductor doping type: p-type  
Gate electrode: n+ poly silicon  
Gate electrode workfunction: 0 eV  
Semiconductor doping: 2.7e18 cm\(^{-3}\)  
Fixed charge density in gate oxide: 0 cm\(^{-3}\)  
Ambient temperature: 300 K  
Initial Voltage: 2 V  
Final Voltage: -4 V  
Number of voltage steps: 100
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(i) The flatband voltage, $V_{FB}$ (HINT: Deduce this from the $V_g = 0$ results.)

The flat band voltage from is just minus the built in voltage of the MOS cap. We can find Vbi from the potential vs. position plot at $V_g = 0$. It is the potential at the top of the oxide minus the potential in the bulk of the semiconductor.

From the above plot: $V_{bi} = 0.566 - (-0.502) = 1.07$ V

$$\phi_{ms} = -V_{bi} = -1.07 \text{ V}.$$ 

(ii) The surface potential, $\phi_s$ (as defined in the text– be careful MOSCap does not use the same reference potential as our text. That is, $\phi$ is not 0 in the bulk.)

From the above plot: $\phi_s = 0.299 - (-0.502) = 0.80$ V

$$\phi_s = 0.80 \text{ V}$$

(ii) The electric field in the oxide, $E_{ox}$

See plot below

$$E_{ox} = 2.24 \times 10^6 \text{ V/cm}$$
(iii) The electric field in the silicon at the surface, $E_{Si}$
See plot below
$E_{Si} = 7.95 \times 10^5$ V/cm

(iv) The depletion region depth, $W_D$
We can "eyeball" this from the electric field vs. position plot, or we can get it as follows.

Charge in silicon: $Q_S = -\kappa_S \varepsilon_0 E_S = -8.3 \times 10^{-7}$ C/cm$^2$
Assume that is it all depletion charge: $Q_D = Q_S - 8.3 \times 10^{-7}$ C/cm$^2$

$Q_D = qN_A W_D$

$W_D = \frac{Q_D}{qN_A} = 19.2$ nm

$W_D = 19.2$ nm

(v) The charge in the silicon, $Q_S$

Since the semiconductor is depleted, is it just the depletion charge calculated above.

$Q_S = Q_D = -8.3 \times 10^{-7}$ C/cm$^2$

$Q_S = -8.3 \times 10^{-7}$ C/cm$^2$
(vi) The charge on the gate, $Q_G$

Charge on gate must balance the charge in the semiconductor.

\[ Q_G = -Q_S = +8.3 \times 10^{-7} \text{ C/cm}^2 \]

(vii) The voltage drop across the oxide, $\Delta \phi_{ox}$

From the potential plot in part (i), we find

\[ \Delta \phi_{ox} = 0.566 - 0.299 = 0.27 \text{ V} \]

\[ \Delta \phi_{ox} = 0.27 \text{ V} \]

(ix) The threshold voltage for this MOS capacitor, $V_T$

From the high frequency CV curve (not shown here), we see that inversion occurs at $V_G = V_T \approx 0.32 \text{ V}$ (The approximate voltage at which the capacitance levels off).

\[ V_T \approx 0.32 \text{ V} \]

Explain how you deduced these parameters, and compare them to the values in part 2a). Some of these values will not be given directly by MOSCap – you will have to deduce them from the results that are given.

<table>
<thead>
<tr>
<th>Result comparison:</th>
<th>Theory</th>
<th>MOSCap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flat band voltage</td>
<td>1.06V</td>
<td>-1.07V</td>
</tr>
<tr>
<td>Surface potential</td>
<td>-0.80V</td>
<td>0.80V</td>
</tr>
<tr>
<td>Electric field in the oxide</td>
<td>2.40e6 V/cm</td>
<td>2.41e6 V/cm</td>
</tr>
<tr>
<td>Electric field at the silicon surface</td>
<td>8.00e5 V/cm</td>
<td>7.91e5 V/cm</td>
</tr>
<tr>
<td>Depletion width</td>
<td>19.4 nm</td>
<td>19.3 nm</td>
</tr>
<tr>
<td>Net charge in silicon</td>
<td>-8.34e-6 C/cm2</td>
<td>-8.26e-7 C/cm2</td>
</tr>
<tr>
<td>Voltage drop across the oxide</td>
<td>0.26 V</td>
<td>0.27 V</td>
</tr>
<tr>
<td>Threshold voltage</td>
<td>0.23 V</td>
<td>0.14 V</td>
</tr>
</tbody>
</table>

Generally, the results are close, since we are in depletion, where it is easy to do hand calculations. MOSCap does not make the depletion approximation, and values of parameters like $n_i$ may be slightly different from what we assumed, which may explain small differences. Threshold voltages are significantly different, but that is a parameter that is not well-defined in the CV curve.